

Cypress Data Book

SRAMs

MODULES

EPROMs

FIFOs

DUAL PORTS

DATA COM

FCT LOGIC

CLOCK CHIPS

PC CHIPSETS

1995



Cypress Data Book

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How To Use This Book






Overall Organization

This book has been organized by product type, beginning with Product Information. The products are next, starting with SRAMs, then Modules, Non-Volatile Memories, FIFOs, Dual-Ports, Data Communications, Bus Interface Products, FCT Logic, Timing Technology Products, and PC Chipsets. A section containing military information is next, followed by Quality and Reliability aspects, then Thermal Data and Packages. Within each section, data sheets are arranged in order of part number.

Recommended Search Paths

<p>To search by:</p> <p><i>Product line</i></p> <p><i>Size</i></p> <p><i>Numeric part number</i></p> <p><i>Other manufacturer's part number</i></p> <p><i>Military part number</i></p>	<p>Use:</p> <p>Table of Contents or flip through the book using the tabs on the right-hand pages.</p> <p>The Product Selector Guide in section 1.</p> <p>Numeric Device Index following the Table of Contents. The book is also arranged in order of part number.</p> <p>The Cross Reference Guide in section 1.</p> <p>The Military Selector Guide in section 12.</p>
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Key to Waveform Diagrams

	=	Rising edge of signal will occur during this time.
	=	Falling edge of signal will occur during this time.
	=	Signal may transition during this time (don't care condition).
	=	Signal changes from high-impedance state to valid logic level during this time.
	=	Signal changes from valid logic level to high-impedance state during this time.

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Table of Contents

Static RAMs (Random Access Memory) (continued)

Page Number

Device	Description	Page Number
CY7C197	256K x 1 Static RAM	2-208
CY7C199	32K x 8 Static RAM	2-216
CY7C1001	256K x 4 Static RAM with Separate I/O	2-227
CY7C1002	256K x 4 Static RAM with Separate I/O	2-227
CY7C1006	256K x 4 Static RAM	2-234
CY7C1007	1M x 1 Static RAM	2-241
CY7C1009	128K x 8 Static RAM	2-247
CY7C1014	256K x 4 Static RAM	2-254
CY7C1016	256K x 4 Static RAM	2-255
CY7C1019	128K x 8 Static RAM	2-256
CY7C1021	64K x 16 Static RAM	2-257
CY7C1031	64K x 18 Synchronous Cache RAM	2-258
CY7C1032	64K x 18 Synchronous Cache RAM	2-258
CY7C1088	128K x 9 Static RAM	2-270
CY7C1331	64K x 18 Synchronous Cache 3.3V RAM	2-271
CY7C1332	64K x 18 Synchronous Cache 3.3V RAM	2-271
CY7C1335	32K x 32 Synchronous Cache RAM	2-283
CY7C1336	32K x 32 Synchronous Cache RAM	2-283
CY7C1399	32K x 8 3.3V Static RAM	2-286

Modules

Page Number

Custom Module Capabilities	3-1	
Device	Description	
CYM1420	128K x 8 Static RAM Module	3-5
CYM1441	256K x 8 Static RAM Module	3-11
CYM1464	512K x 8 Static RAM Module	3-16
CYM1465	512K x 8 SRAM Module	3-22
CYM1471	1024K x 8 SRAM Module	3-28
CYM1481	2048K x 8 SRAM Module	3-28
CYM1622	64K x 16 Static RAM Module	3-34
CYM1720	32K x 24 Static RAM Module	3-39
CYM1730	64K x 24 Static RAM Module	3-44
CYM1821	16K x 32 Static RAM Module	3-49
CYM1828	32K x 32 Static RAM Module	3-55
CYM1831	64K x 32 Static RAM Module	3-62
CYM1832	64K x 32 Static RAM Module	3-67
CYM1836	128K x 32 Static RAM Module	3-72
CYM1838	128K x 32 Static RAM Module	3-77
CYM1840	256K x 32 Static RAM Module	3-82
CYM1841	256K x 32 Static RAM Module	3-88
CYM1841A	256K x 32 Static RAM Module	3-88
CYM1846	512K x 32 Static RAM Module	3-97
CYM1851	1,024K x 32 Static RAM Module	3-102
CYM7232	DRAM Accelerator Module	3-107
CYM7264	DRAM Accelerator Module	3-107
CYM7420	82420 PCIsset-Compatible Level II Cache Module	3-108
CYM7421	82420 PCIsset-Compatible Level II Cache Module	3-108
CYM7424	128K Cache Module for the Intel™ 82420EX PCIsset	3-109
CYM7425	256K Cache Module for the Intel 82420EX PCIsset	3-109
CYM7427	82420 PCIsset-Compatible Level II Cache Module Family	3-114
CYM7428	82420 PCIsset-Compatible Level II Cache Module Family	3-114

Non-Volatile Memories (continued)		Page Number
Device	Description	
CY7C265	8K x 8 Registered PROM	4-121
CY7C266	8K x 8 Power-Switched and Reprogrammable PROM	4-129
CY7C269	8K x 8 Registered Diagnostic PROM	4-136
CY7C271	32K x 8 Power-Switched and Reprogrammable PROM	4-147
CY7C274	32K x 8 Power-Switched and Reprogrammable PROM	4-147
CY7C271A	32K x 8 Power-Switched and Reprogrammable PROM	4-148
CY7C276	16K x 16 Reprogrammable PROM	4-155
CY7C277	32K x 8 Reprogrammable Registered PROM	4-161
CY7C281A	1K x 8 PROM	4-168
CY7C282A	1K x 8 PROM	4-168
CY7C287	64K x 8 Reprogrammable Registered PROM	4-174
CY7C291A	2K x 8 Reprogrammable PROM	4-180
CY7C292A	2K x 8 Reprogrammable PROM	4-180
CY7C293A	2K x 8 Reprogrammable PROM	4-180
Non-Volatile Memory Programming Information		4-189

FIFOs		Page Number
Device	Description	
CY7C401	64 x 4 Cascadable FIFO	5-1
CY7C402	64 x 5 Cascadable FIFO	5-1
CY7C403	64 x 4 Cascadable FIFO	5-1
CY7C404	64 x 5 Cascadable FIFO	5-1
CY7C408A	64 x 8 Cascadable FIFO	5-12
CY7C409A	64 x 9 Cascadable FIFO	5-12
CY7C419	256 x 9 Cascadable FIFO	5-26
CY7C420	512 x 9 Cascadable FIFO	5-26
CY7C421	512 x 9 Cascadable FIFO	5-26
CY7C424	1K x 9 Cascadable FIFO	5-26
CY7C425	1K x 9 Cascadable FIFO	5-26
CY7C428	2K x 9 Cascadable FIFO	5-26
CY7C429	2K x 9 Cascadable FIFO	5-26
CY7C432	4K x 9 Cascadable FIFO	5-26
CY7C433	4K x 9 Cascadable FIFO	5-26
CY7C4421	64 x 9 Synchronous FIFO	5-48
CY7C4201	256 x 9 Synchronous FIFO	5-48
CY7C4211	512 x 9 Synchronous FIFO	5-48
CY7C4221	1K x 9 Synchronous FIFO	5-48
CY7C4231	2K x 9 Synchronous FIFO	5-48
CY7C4241	4K x 9 Synchronous FIFO	5-48
CY7C4251	8K x 9 Synchronous FIFO	5-48
CY7C4425	64 x 18 Synchronous FIFO	5-67
CY7C4205	256 x 18 Synchronous FIFO	5-67
CY7C4215	512 x 18 Synchronous FIFO	5-67
CY7C4225	1K x 18 Synchronous FIFO	5-67
CY7C4235	2K x 18 Synchronous FIFO	5-67
CY7C4245	4K x 18 Synchronous FIFO	5-67
CY7C439	Bidirectional 2K x 9 FIFO	5-86
CY7C441	Clocked 512 x 9 FIFO	5-99
CY7C443	Clocked 2K x 9 FIFO	5-99
CY7C451	512 x 9 Cascadable Clocked FIFO with Programmable Flags	5-115
CY7C453	2K x 9 Cascadable Clocked FIFO with Programmable Flags	5-115

Bus Interface Products		Page Number
Device	Description	
VIC64	VMEbus Interface Controller with D64 Functionality	8-1
VIC068A	VMEbus Interface Controller	8-7
VAC068A	VMEbus Address Controller	8-16
CY7C960	Slave VMEbus Interface Controller Family	8-22
CY7C961	Slave VMEbus Interface Controller Family	8-22
CY7C964	Bus Interface Logic Circuit	8-27

FCT Logic Products		Page Number
Parameter Measurement Information		9-1

Device	Description	
CY29FCT52T	8-Bit Registered Transceiver	9-6
CY29FCT520T	Multi-Level Pipeline Register	9-12
CY29FCT818T	Diagnostic Scan Register	9-17
CY54/74FCT138T	1-of-8 Decoder	9-23
CY54/74FCT157T	Quad 2-Input Multiplexer	9-27
CY54/74FCT158T	Quad 2-Input Multiplexer	9-27
CY54/74FCT163T	4-Bit Binary Counter	9-33
CY54/74FCT191T	4-Bit Up/Down Binary Counter	9-38
CY54/74FCT240T	8-Bit Buffer/Line Driver	9-44
CY54/74FCT244T	8-Bit Buffer/Line Driver	9-44
CY54/74FCT245T	8-Bit Transceiver	9-49
CY54/74FCT257T	Quad 2-Input Multiplexer	9-54
CY54/74FCT273T	8-Bit Register	9-59
CY54/74FCT373T	8-Bit Latch	9-64
CY54/74FCT573T	8-Bit Latch	9-64
CY54/74FCT374T	8-Bit Register	9-69
CY54/74FCT574T	8-Bit Register	9-69
CY54/74FCT377T	8-Bit Register	9-74
CY54/74FCT399T	Quad 2-Input Register	9-79
CY54/74FCT480T	Dual 8-Bit Parity Generator/Checker	9-84
CY54/74FCT540T	8-Bit Buffer/Line Driver	9-89
CY54/74FCT541T	8-Bit Buffer/Line Driver	9-89
CY54/74FCT543T	8-Bit Latched Registered Transceiver	9-94
CY54/74FCT646T	8-Bit Registered Transceiver	9-100
CY54/74FCT648T	8-Bit Registered Transceiver	9-100
CY54/74FCT652T	8-Bit Registered Transceiver	9-106
CY54/74FCT821T	8-Bit Bus Interface Register	9-112
CY54/74FCT823T	9-Bit Bus Interface Register	9-112
CY54/74FCT825T	10-Bit Bus Interface Register	9-112
CY54/74FCT827T	10-Bit Buffer	9-121
CY54/74FCT841T	10-Bit Latch	9-126
CY54/74FCT2240T	8-Bit Buffer/Line Driver	9-133
CY54/74FCT2244T	8-Bit Buffer/Line Driver	9-133
CY54/74FCT2245T	8-Bit Transceiver	9-138
CY54/74FCT2257T	Quad 2-Input Multiplexer	9-142
CY54/74FCT2373T	8-Bit Latch	9-146
CY54/74FCT2573T	8-Bit Latch	9-146
CY54/74FCT2374T	8-Bit Register	9-151
CY54/74FCT2574T	8-Bit Register	9-151
CY54/74FCT2541T	8-Bit Buffer/Line Driver	9-156
CY54/74FCT2543T	8-Bit Latched Transceiver	9-160



Table of Contents

Timing Technology Products (continued) Page Number

Device	Description	Page Number
ICD2042A	Dual VGA Clock Generator	10-51
ICD2051	Dual Programmable Clock Generator	10-56
ICD2053B	Programmable Clock Generator	10-64
ICD2061A	Dual Programmable Graphics Clock Generator	10-71
ICD2062B	Dual Programmable ECL/TTL Clock Generator	10-85
ICD2063	Programmable Graphics Clock Generator	10-100
ICD2093	“Super Buffer” Clock Generator	10-117
ICD6233	One-Time-Programmable Clock Oscillator	10-127
CY7B991	Programmable Skew Clock Buffer (PSCB)	10-130
CY7B992	Programmable Skew Clock Buffer (PSCB)	10-130
CY7B9910	Low Skew Clock Buffer	10-141
CY7B9920	Low Skew Clock Buffer	10-141

PC Chipsets Page Number

Device	Description	Page Number
CY82C597	386/486 Green Chipset	11-1
CY82C599	Intelligent PCI Bus Controller	11-61

Military Information Page Number

Military Overview	12-1
Military Product Selector Guide	12-2
Military Ordering Information	12-7

Quality and Reliability Page Number

Quality, Reliability, and Process Flows	13-1
Tape and Reel Specifications	13-16

Packages Page Number

Thermal Management and Component Reliability	14-1
Package Diagrams	14-11
Module Package Diagrams	14-92

Sales Representatives and Distributors

- Direct Sales Offices
- North American Sales Representatives
- International Sales Representatives
- Distributors



Numeric Device Index

Device Number	Description	Page Number
CY54/74FCT825T	10-Bit Bus Interface Register	9-112
CY54/74FCT827T	10-Bit Buffer	9-121
CY54/74FCT841T	10-Bit Latch	9-126
CY6264	8K x 8 Static RAM	2-1
CY74FCT162240T	16-Bit Buffer/Line Driver	9-184
CY74FCT162244T	16-Bit Buffer/Line Driver	9-188
CY74FCT162245T	16-Bit Transceiver	9-193
CY74FCT162373T	16-Bit Latch	9-199
CY74FCT162374T	16-Bit Register	9-203
CY74FCT16240T	16-Bit Buffer/Line Driver	9-184
CY74FCT16244T	16-Bit Buffer/Line Driver	9-188
CY74FCT16245T	16-Bit Transceiver	9-193
CY74FCT162500T	18-Bit Registered Transceiver	9-207
CY74FCT162501T	18-Bit Registered Transceiver	9-211
CY74FCT162543T	16-Bit Latched Transceiver	9-217
CY74FCT162646T	16-Bit Registered Transceiver	9-223
CY74FCT162652T	16-Bit Registered Transceiver	9-229
CY74FCT162823T	18-Bit Register	9-236
CY74FCT162827T	20-Bit Buffer	9-242
CY74FCT162841T	20-Bit Latch	9-247
CY74FCT162952T	16-Bit Registered Transceiver	9-252
CY74FCT162H244T	16-Bit Buffer/Line Driver	9-188
CY74FCT162H245T	16-Bit Transceiver	9-193
CY74FCT162H501T	18-Bit Registered Transceiver	9-211
CY74FCT162H952T	16-Bit Registered Transceiver	9-252
CY74FCT16373T	16-Bit Latch	9-199
CY74FCT16374T	16-Bit Register	9-203
CY74FCT16444T	16-Bit Buffer/Line Driver	9-188
CY74FCT16445T	16-Bit Transceiver	9-193
CY74FCT16500T	18-Bit Registered Transceiver	9-207
CY74FCT16501T	18-Bit Registered Transceiver	9-211
CY74FCT16543T	16-Bit Latched Transceiver	9-217
CY74FCT16646T	16-Bit Registered Transceiver	9-223
CY74FCT16652T	16-Bit Registered Transceiver	9-229
CY74FCT16823T	18-Bit Register	9-236
CY74FCT16827T	20-Bit Buffer	9-242
CY74FCT16841T	20-Bit Latch	9-247
CY74FCT16952T	16-Bit Registered Transceiver	9-252
CY7B134	4K x 8 Dual-Port Static RAM	6-74
CY7B1342	4K x 8 Dual-Port Static RAM with Semaphores	6-74
CY7B135	4K x 8 Dual-Port Static RAM	6-74
CY7B138	4K x 8 Dual-Port Static RAM with Sem, Int, Busy	6-87
CY7B139	4K x 9 Dual-Port Static RAM with Sem, Int, Busy	6-87
CY7B144	8K x 8 Dual-Port Static RAM with Sem, Int, Busy	6-103
CY7B145	8K x 9 Dual-Port Static RAM with Sem, Int, Busy	6-103
CY7B8392	Ethernet Coax Transceiver Interface	7-67
CY7B923	HOTLink Transmitter	7-8
CY7B933	HOTLink Receiver	7-8
CY7B951	SST SONET/SDH Serial Transceiver	7-35
CY7B972	100BASE-TX/10BASE-T Fast Ethernet Transceiver	7-66
CY7B991	Programmable Skew Clock Buffer (PSCB)	10-130
CY7B9910	Low Skew Clock Buffer	10-141
CY7B992	Programmable Skew Clock Buffer (PSCB)	10-130
CY7B9920	Low Skew Clock Buffer	10-141
CY7C006	16K x 8 Dual-Port Static RAM with Sem, Int, Busy	6-1
CY7C016	16K x 9 Dual-Port Static RAM with Sem, Int, Busy	6-1
CY7C024	4K x 16 Dual-Port Static RAM with Sem, Int, Busy	6-18



Numeric Device Index

Device Number	Description	Page Number
CY7C182	8K x 9 Static RAM	2-142
CY7C185	8K x 8 Static RAM	2-147
CY7C185A	8K x 8 Static RAM	2-155
CY7C187	64K x 1 Static RAM	2-163
CY7C187A	64K x 1 Static RAM	2-170
CY7C188	32K x 9 Static RAM	2-178
CY7C191	64K x 4 Static RAM with Separate I/O	2-185
CY7C192	64K x 4 Static RAM with Separate I/O	2-185
CY7C193	32K x 8 Synchronous SRAM	2-193
CY7C194	64K x 4 Static RAM	2-199
CY7C195	64K x 4 Static RAM	2-199
CY7C196	64K x 4 Static RAM	2-199
CY7C197	256K x 1 Static RAM	2-208
CY7C199	32K x 8 Static RAM	2-216
CY7C225A	512 x 8 Registered PROM	4-76
CY7C235A	1K x 8 Registered PROM	4-83
CY7C243	4K x 8 Reprogrammable PROM	4-90
CY7C244	4K x 8 Reprogrammable PROM	4-90
CY7C245A	2K x 8 Reprogrammable Registered PROM	4-97
CY7C251	16K x 8 Power-Switched and Reprogrammable PROM	4-105
CY7C254	16K x 8 Power-Switched and Reprogrammable PROM	4-105
CY7C261	8K x 8 Power-Switched and Reprogrammable PROM	4-112
CY7C263	8K x 8 Power-Switched and Reprogrammable PROM	4-112
CY7C264	8K x 8 Power-Switched and Reprogrammable PROM	4-112
CY7C265	8K x 8 Registered PROM	4-121
CY7C266	8K x 8 Power-Switched and Reprogrammable PROM	4-129
CY7C269	8K x 8 Registered Diagnostic PROM	4-136
CY7C271	32K x 8 Power-Switched and Reprogrammable PROM	4-147
CY7C271A	32K x 8 Power-Switched and Reprogrammable PROM	4-148
CY7C274	32K x 8 Power-Switched and Reprogrammable PROM	4-147
CY7C276	16K x 16 Reprogrammable PROM	4-155
CY7C277	32K x 8 Reprogrammable Registered PROM	4-161
CY7C281A	1K x 8 PROM	4-168
CY7C282A	1K x 8 PROM	4-168
CY7C287	64K x 8 Reprogrammable Registered PROM	4-174
CY7C291A	2K x 8 Reprogrammable PROM	4-180
CY7C292A	2K x 8 Reprogrammable PROM	4-180
CY7C293A	2K x 8 Reprogrammable PROM	4-180
CY7C401	64 x 4 Cascadable FIFO	5-1
CY7C402	64 x 5 Cascadable FIFO	5-1
CY7C403	64 x 4 Cascadable FIFO	5-1
CY7C404	64 x 5 Cascadable FIFO	5-1
CY7C408A	64 x 8 Cascadable FIFO	5-12
CY7C409A	64 x 9 Cascadable FIFO	5-12
CY7C419	256 x 9 Cascadable FIFO	5-26
CY7C420	512 x 9 Cascadable FIFO	5-26
CY7C4201	256 x 9 Synchronous FIFO	5-48
CY7C4205	256 x 18 Synchronous FIFO	5-67
CY7C421	512 x 9 Cascadable FIFO	5-26
CY7C4211	512 x 9 Synchronous FIFO	5-48
CY7C4215	512 x 18 Synchronous FIFO	5-67
CY7C4221	1K x 9 Synchronous FIFO	5-48
CY7C4225	1K x 18 Synchronous FIFO	5-67
CY7C4231	2K x 9 Synchronous FIFO	5-48
CY7C4235	2K x 18 Synchronous FIFO	5-67
CY7C424	1K x 9 Cascadable FIFO	5-26
CY7C4241	4K x 9 Synchronous FIFO	5-48



Numeric Device Index

Device Number	Description	Page Number
CYM7421	82420 PCIsset-Compatible Level II Cache Module	3-108
CYM7424	128K Cache Module for the Intel™ 82420EX PCIsset	3-109
CYM7425	256K Cache Module for the Intel 82420EX PCIsset	3-109
CYM7427	82420 PCIsset-Compatible Level II Cache Module Family	3-114
CYM7428	82420 PCIsset-Compatible Level II Cache Module Family	3-114
CYM7432	256K Pentium-Compatible Cache Module	3-115
CYM7450	128K Cache Module for VLSI VL82C483 Chipset	3-118
CYM7451	256K Cache Module for VLSI VL82C483 Chipset	3-118
CYM7490	i486™ Level II Cache Module	3-119
CYM7491	i486 Level II Cache Module	3-119
CYM7492	i486 Level II Cache Module	3-119
CYM74A430	Intel 82430FX PCIsset Level II Cache Module	3-125
CYM74A550	OPTi Viper Chipset Level II Cache Module	3-130
CYM74A551	OPTi Viper Chipset Level II Cache Module	3-130
CYM74A590	VLSI 82C590 Chipset Level II Cache Module	3-135
CYM74AP54	Intel 82430NX Chipset Level II Cache Module	3-120
CYM74S430	Intel 82430FX PCIsset Level II Cache Module	3-125
CYM74S431	Intel 82430FX PCIsset Level II Cache Module	3-125
CYM74S550	OPTi Viper Chipset Level II Cache Module	3-130
CYM74S551	OPTi Viper Chipset Level II Cache Module	3-130
CYM74S590	VLSI 82C590 Chipset Level II Cache Module	3-135
CYM74S591	VLSI 82C590 Chipset Level II Cache Module	3-135
CYM74SP54	Intel 82430NX Chipset Level II Cache Module	3-120
CYM74SP55	Intel 82430NX Chipset Level II Cache Module	3-120
CYM9230	82420 PCIsset-Compatible Level II Cache Module	3-140
CYM9231	82420 PCIsset-Compatible Level II Cache Module	3-140
CYM9236	128K Cache Module for the UMC491 Chipset	3-141
CYM9237	256K Cache Module for the UMC491 Chipset	3-141
CYM9244	128K Cache Module for the OPTi 802GP Chipset	3-142
CYM9245	256K Cache Module for the OPTi 802GP Chipset	3-142
CYM9246	128K Cache Module for the OPTi 802GP Chipset	3-142
CYM9247	256K Cache Module for the OPTi 802GP Chipset	3-142
ICD2023	PC Motherboard Clock Generator	10-19
ICD2025	Motherboard Clock Generator	10-27
ICD2027	PC Motherboard Clock Generator	10-33
ICD2028	PC Motherboard Clock Generator	10-39
ICD2042A	Dual VGA Clock Generator	10-51
ICD2051	Dual Programmable Clock Generator	10-56
ICD2053B	Programmable Clock Generator	10-64
ICD2061A	Dual Programmable Graphics Clock Generator	10-71
ICD2062B	Dual Programmable ECL/TTL Clock Generator	10-85
ICD2063	Programmable Graphics Clock Generator	10-100
ICD2093	“Super Buffer” Clock Generator	10-117
ICD6233	One-Time-Programmable Clock Oscillator	10-127
VAC068A	VMEbus Address Controller	8-16
VIC068A	VMEbus Interface Controller	8-7
VIC64	VMEbus Interface Controller with D64 Functionality	8-1



Section Contents

General Product Information	Page Number
Cypress Semiconductor Background	1-1
Ordering Information	1-4
Datasheets Available Upon Request	1-8
Cypress Semiconductor Bulletin Board System (BBS) Announcement	1-9
Application Notes	1-10
Product Selector Guide	1-12
Product Line Cross Reference	1-25



ing RoboClock, a programmable skew clock buffer that adjusts complex timing control signals for a broad range of systems. The division also offers a broad range of First-In, First-Out (FIFO) memories, used to communicate data between systems operating at different frequencies, and Dual-Port Memories, used to distribute data to two different systems simultaneously.

Computation Products Division

This division focuses on the high-volume, high-growth market surrounding the desktop computer. It is the second of Cypress's market-oriented divisions. The division includes timing technology products offered through Cypress's IC Designs Subsidiary in Kirkland, Washington, and a new line of PC chipsets. IC Designs products are used widely in personal computers and disk drives, and the product line provides Cypress with major inroads into these growing markets. IC Designs clock oscillators control the intricate timing of all aspects of a computer system, including signals for the computer's central processing unit (CPU), keyboard, disk drives, system bus, serial port, and real-time clock. They replace all of the metal can oscillators used in the system. This product line includes QuiXTAL™—a programmable metal can oscillator that replaces individual oscillators used to control timing signals in virtually every type of electronics equipment. Cypress's chipset offerings include products for 486-based personal computers, as well as PCI local bus controllers for graphics and multimedia desktop applications. Cypress has announced plans to introduce a low-power, 3.3 volt chipset for the Pentium P54C, as well as P54C bus controller.

Cypress Facilities

Cypress operates wafer fabrication facilities in California's Silicon Valley (San Jose), Round Rock (Austin), Texas, and Bloomington, Minnesota. The company's fourth wafer fab, located adjacent to the Bloomington, Minnesota facility, is scheduled to go on-line in mid-1995. There are additional Cypress Design Centers in Starkville, Mississippi, Colorado Springs, Colorado, and the United Kingdom, and a PLD software design group in Beaverton, Oregon. The facilities are designed to the most demanding technical and environmental specifications in the industry. At the Texas and Minnesota facilities, the entire wafer fabrication area is specified to be a Class 1 environment. This means that the ambient air has less than 1 particle of greater than 0.2 microns in diameter per cubic foot of air. Other environmental considerations are carefully insured: temperature is controlled to a ± 0.1 degree Fahrenheit tolerance; filtered air is completely exchanged more than 10 times each minute throughout the fab; and critical equipment is situated on isolated slabs to minimize vibration.

The company has also received ISO9000 registration, a standard model of quality assurance that is awarded to companies with exacting standards of quality management, production, and inspections.

Attention to assembly is equally critical. Cypress manufactures 100 percent of our wafers in the United States, at our front-end fabrication sites in California (San Jose), Minnesota (Bloomington), and Texas (Round Rock). Cypress Texas, our largest fab, and Cypress Minnesota, our newest fab, are both Class 1 facilities.

To improve our global competitiveness, we chose to move most of our back-end assembly, test, and mark operations to a facility in Thailand. Be assured that Cypress's total quality commitment extends to the new site—Cypress Bangkok.

The move to Bangkok consummated an intense search by Cypress for a world-class, environmentally sophisticated facility

that we could bring on line quickly. The Cypress search team scrutinized fifteen manufacturing facilities in five countries and chose a site managed by Alphatec Electronics Co., Ltd., a privately owned, entrepreneurial company promoted by the Thailand Board of Investment. Cypress Bangkok occupies almost 25,000 square feet—a significant portion of the manufacturing floor space available within the facility. The full facility at Bangkok occupies more than 85,000 square feet on a site that encompasses 25 acres—sufficient room for expansion to a number of buildings in a campus-like setting.

Manufacturing at the site since 1990 with a charter to specialize in IC packaging, the Alphatec facility has almost a century of person-years experience working for U.S. semiconductor suppliers. Thoroughly modern, MIL 883-certified, and with fully developed administrative, logistic, and manufacturing systems in place, the facility has earned an exceptional reputation for hermetic assembly and out-going quality.

Cypress San Jose maintains complete management control of Cypress Bangkok's assembly, test, mark, and ship operations within the facility, thus assuring complete continuity of San Jose's back-end operations and quality.

Cypress has added Tape Automated Bonding (TAB) to its package offering. TAB, a surface-mount packaging technology, provides the densest lead and package footprint available for fully tested die.

From Cypress's facility in Minnesota, a VME Bus Interface Products group has been in operation since the acquisition of VTC's fab in 1990. Cypress manufactures VIC and VAC VME devices on the 0.8 micron CMOS process.

The Cypress motto has always been "only the best—the best facilities, the best equipment, the best employees ... all striving to make the best CMOS and BiCMOS products."

Cypress Process Technology

In the last decade, there has been a tremendous need for high-performance semiconductor products manufactured with a balance of SPEED, RELIABILITY, and POWER. Cypress Semiconductor overcame the classically held perceptions that CMOS was a moderate-performance technology.

Cypress initially introduced a 1.2-micron "N" well technology with double-layer poly and a single-layer metal. The process employed lightly doped extensions of the heavily doped source and drain regions for both "N" and "P" channel transistors for significant improvement in gate delays. Further improvements in performance, through the use of substrate bias techniques, have added the benefit of eliminating the input and output latch-up characteristics associated with older CMOS technologies.

Cypress pushed process development to new limits in the areas of PROMs (Programmable Read Only Memory) and EPLDs (Erasable Programmable Logic Devices). Both PROMs and EPLDs have existed since the early 1970s in a bipolar process that employed various fuse technologies and was the only viable high-speed nonvolatile process available. Cypress PROMs and EPLDs use EPROM technology, which has been in use in MOS (Metal Oxide Silicon) since the early 1970s. EPROM technology has traditionally emphasized density while forsaking performance. Through improved technology, Cypress produced the first high-performance CMOS PROMs and EPLDs, replacing their bipolar counterparts.

To maintain our leadership position in CMOS technology, Cypress introduced a sub-micron technology in 1987. This 0.8 micron breakthrough made Cypress's CMOS one of the most

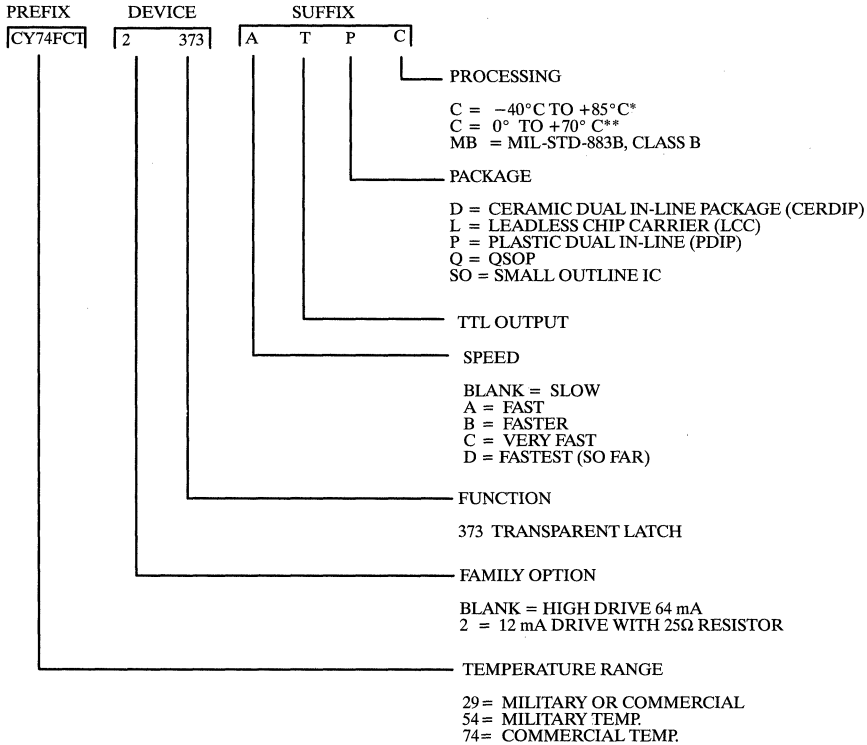


Ordering Information

In general, the valid ordering codes for all products (except modules and VMEbus products) follow the format below; e.g., CY7C128-45DMB, PALC16R8L-35PC.

RAM, PROM, FIFO, μ P, ECL

PREFIX	DEVICE	SUFFIX	FAMILY
CY	7C128	-45 D M B	CMOS SRAM PROM FIFO μ P
CY	7C245	L-35 P C	
CY	7C404	-25 D M B	
CY	7C9101	-30 P C	
C = CMOS			
			PROCESSING
			B = MIL-STD-883C FOR MILITARY PRODUCT
			= LEVEL 2 PROCESSING FOR COMMERCIAL PRODUCT
			T = SURFACE-MOUNTED DEVICES TO BE TAPE AND REELED
			R = LEVEL 2 PROCESSING ON TAPE AND REELED DEVICES
			TEMPERATURE RANGE
			C = COMMERCIAL (0°C TO +70°C)
			I = INDUSTRIAL (-40°C TO +85°C)
			M = MILITARY (-55°C TO +125°C)
			PACKAGE
			A = THIN QUAD PLSTIC FLATPACK (TOFP)
			B = PLASTIC PIN GRID ARRAY (PPGA)
			D = CERAMIC DUAL IN-LINE PACKAGE (CERDIP)/BRAZED DIP
			E = TAPE AUTOMATED BONDING (TAB)
			F = FLATPACK (SOLDER-SEALED FLAT PACKAGE)
			G = PIN GRID ARRAY (PGA)
			H = WINDOWED LEADED CHIP CARRIER
			J = PLASTIC LEADED CHIP CARRIER (PLCC)
			K = CERPACK (GLASS-SEALED FLAT PACKAGE)
			L = LEADLESS CHIP CARRIER (LCC)
			N = PLASTIC QUAD FLATPACK (PQFP)
			P = PLASTIC DUAL IN-LINE (PDIP)
			Q = WINDOWED LEADLESS CHIP CARRIER (LCC)
			R = WINDOWED PIN GRID ARRAY (PGA)
			S = SOIC (GULL WING)
			T = WINDOWED CERPACK
			U = CERAMIC QUAD FLATPACK (CQFP)
			V = SOIC (J LEAD)
			W = WINDOWED CERAMIC DUAL IN-LINE PACKAGE (CERDIP)
			X = DICE (WAFFLE PACK)
			Y = CERAMIC LEADED CHIP CARRIER
			SPEED (ns or MHz)
			L = LOW-POWER OPTION
			A, B, C = REVISION LEVEL

FCT Octal Products


* COMMERCIAL TEMPERATURE IS -40°C TO +85°C FOR "STANDARD", "A", AND "B" SPEED

** COMMERCIAL TEMPERATURE IS 0°C TO +70°C FOR "C" SPEED



Datasheets listed here are not in this catalog but can be obtained from a Cypress Sales Representative.

Static RAMs (Random Access Memory)

Device Number

CY2147
CY2148/CY21L48/CY2149/CY21L49
CY6116
CY6116A/CY6117A
CY7C122
CY7C128
CY7C147
CY7C167
CY7C168/CY7C169
CY7C170
CY7C171/CY7C172
CY7C183/CY7C184
CY7C186
CY7C189/CY7C190
CY7C198
CY74S189/CY27LS03/CY27S03/CY27S07
CY93L422A/CY93422/CY93L422

Description

4096 x 1 Static R/W RAM
1024 x 4 Static R/W RAM
2048 x 8 Static R/W RAM
2048 x 8 Static R/W RAM
256 x 4 Static R/W RAM Separate I/O
2048 x 8 Static R/W RAM
4096 x 1 Static RAM
16,384 x 1 Static R/W RAM
4096 x 4 Static RAM
4096 x 4 Static R/W RAM
4096 x 4 Static R/W RAM Separate I/O
2 x 4096 x 16 Cache RAM
8K x 8 Static RAM
16 x 4 Static R/W RAM
32K x 8 Static R/W RAM
16 x 4 Static R/W RAM
256 x 4 Static R/W RAM

FIFOs

Device Number

CY3341

Description

64 x 4 Serial Memory FIFO

Logic

Device Number

CY2901C
CY2909/11
CY2910
CY7C901
CY7C909/11
CY7C910

Description

CMOS 4-Bit Slice
CMOS Microprogram Sequencers
CMOS Microprogram Controller
CMOS 4-Bit Slice
CMOS Microprogram Sequencers
CMOS Microprogram Controller

Modules

Device Number

CYM1466
CYM1611
CYM1830

Description

512K x 8 Static RAM Module
16K x 16 Static RAM Module
64K x 32 Static RAM Module

Contact a Cypress representative or use the Cypress Bulletin Board System to get copies of the application notes listed here.

General Information

I/O Characteristics of Cypress Products
Power Characteristics of Cypress Products
Protection, Decoupling, and Filtering of Cypress CMOS Circuits
System Design Considerations when Using Cypress CMOS Circuits
Tips for High-Speed Logic Design
Using Decoupling Capacitors

Modules

CYM7232/7264 DRAM Accelerator:
Mixing 5-Volt and 3.3-Volt DRAMs
DRAM Accelerator: Set-Up for Basic Operation
DRAM Configuration and Diagnostics
DRAM Interfacing
Multichip Family of JEDEC ZIP/SIMM Modules
Packages in High-Density Module Designs

ECL and TTL BiCMOS

A New Generation of BiCMOS High-Speed TTL SRAMs
Access Time vs. Load Capacitance for High-Speed TTL SRAMs
BiCMOS TTL & ECL SRAMs Improve High-Performance Systems
BiCMOS TTL SRAMs Improve R3000 and R3000A Systems
Combining SRAMs Without an External Decoder
Memory and Support for Next-Generation ECL Systems
Noise Considerations in High-Speed Logic Systems
PLCC/CLCC Packaging for High-Speed Parts
Using ECL in Single +5V TTL Systems

SRAMs

Cypress RAM I/O Characteristics
Second-Level Cache and Main Memory Systems for the 80486
Understanding Dual-Port RAMs
Using Dual-Port RAMs Without Arbitration
Using Cypress SRAMs to Implement 386 Cache
Using the CY7C180/181 Cache Tag RAM

PROMs

Designing Custom ALUs and Multipliers with PROMs
Generating PROM Programming Files
Interfacing the CY7C276 High-Speed PROM to the AT&T, AD, Motorola, and TI DSPs
Pinout Compatibility Considerations of SRAMs and PROMs

PLDs

ABEL 4.0/4.1 and the CY7C330, CY7C331, and CY7C332
Abel-HDL vs. IEEE-1076 VHDL
Architectures and Technologies for FPGAs

Are Your PLDs Metastable?

Bus-Oriented Maskable Interrupt Controller
CMOS PAL Basics
CY7C331 Asynchronous Self-Timed VMEbus Requestor
CY7C344 as a Second-Level Cache Controller for the 80486
CY7C380 Family Quick Power Calculator
Describing State Machines with *Warp2* VHDL
Design Tips for Advanced Max Users
Designing a Multiprocessor Interrupt Distribution Unit with MAX
Designing with the CY7C35 and *Warp2* VHDL Compiler
Designing with FPGAs
DMA Control Using the CY7C342 MAX EPLD
The FLASH370 Family of CPLDs and Designing with *Warp2*
Implementing a Reframe Controller for the CY7B933 HOTLink Receiver in a CY7C371 CPLD
FIFO RAM Controller with Programmable Flags
Getting Started Converting .ABL Files to VHDL
Interfacing PROMs and RAMs to DSP Using Cypress MAX Products
PAL Design Example: A GCR Encoder/Decoder
pASIC380 Power vs. Operating Frequency
PLD-Based Data Path for SCSI-2
State Machine Design Considerations and Methodologies
T2 Framing Circuitry
Top-Down Design Methodology with VHDL
Using ABEL to Program the Cypress 22V10
Using CUPL with Cypress PLDs
Using Hierarchical VHDL Design
Using Log/IC to Program the CY7C330
Using Scan Mode on pASIC380 for In-Circuit Testing
Using the CY7C331 as a Waveform Generator
VHDL Techniques for Optimal Design Fitting
Describing State Machines with *Warp2*

Static RAMs

Size	Organization	Pins	Part Number	Speed (ns)	I _{CC} /I _{SB} (mA @ ns)	Packages
64	16x4—Inverting	16	CY7C189	t _{AA} = 15, 25	55 @ 25	D, P
64	16x4—Non-Inverting	16	CY7C190	t _{AA} = 15, 25	55 @ 25	L, P
64	16x4—Inverting	16	CY74S189	t _{AA} = 35	90 @ 35	D, P
64	16x4—Inverting	16	CY27S03A	t _{AA} = 25, 35	90 @ 25	D, P
64	16x4—Non-Inverting	16	CY27S07A	t _{AA} = 25, 35	90 @ 25	D, P
1K	256x4	22	CY7C122	t _{AA} = 15, 25, 35	60 @ 25	D, L, P, S
1K	256x4	24S	CY7C123	t _{AA} = 7, 9, 10, 12, 15	120 @ 7	L, P, V
1K	256x4	22	CY9122/91L22	t _{AA} = 25, 35, 45	120 @ 25	P
1K	256x4	22	CY93422A/93L422A	t _{AA} = 35, 45	80 @ 45	L, P
4K	4Kx1—CS Power-Down	18	CY7C147	t _{AA} = 25, 35, 45	80/10 @ 35	D, P
4K	4Kx1—CS Power-Down	18	CY2147/21L47	t _{AA} = 35, 45, 55	125/25 @ 35	D, P
4K	1Kx4—CS Power-Down	18	CY7C148	t _{AA} = 25, 35, 45	80/10 @ 35	D, P
4K	1Kx4—CS Power-Down	18	CY2148/21L48	t _{AA} = 35, 45, 55	120/20 @ 35	D, P
4K	1Kx4	18	CY7C149	t _{AA} = 25, 35, 45	80 @ 35	D, L, P
4K	1Kx4	18	CY2149/21L49	t _{AA} = 35, 45, 55	120 @ 35	D, P
4K	1Kx4—Separate I/O, Reset	24S	CY7C150	t _{AA} = 10, 12, 15, 25, 35	90 @ 12	D, P, S
16K	2Kx8—CS Power-Down	24	CY7C128A	t _{AA} = 15, 20, 25, 35, 45, 55	90/20 @ 55	D, L, P, V
16K	2Kx8—CS Power-Down	24	CY6116A	t _{AA} = 20, 25, 35, 45, 55	80/20 @ 55	D, L
16K	2Kx8—CS Power-Down	24	CY6117A	t _{AA} = 20, 25, 35, 45, 55	80/20 @ 55	L
16K	16Kx1—CS Power-Down	30	CY7C167A	t _{AA} = 15, 20, 25, 35, 45	50/15 @ 45	D, P, V
16K	4Kx4—CS Power-Down	20	CY7C168A	t _{AA} = 15, 20, 25, 35, 45	70/15 @ 45	D, P, V
16K	4Kx4	20	CY7C169A	t _{AA} = 15, 20, 25, 35, 45	70 @ 45	P
16K	4Kx4—Output Enable	22S	CY7C170A	t _{AA} = 15, 20, 25, 35, 45	90 @ 45	P, V
16K	4Kx4—Separate I/O	24S	CY7C171A	t _{AA} = 15, 20, 25, 35, 45	90 @ 45	D, L, P, V
16K	4Kx4—Separate I/O	24S	CY7C172A	t _{AA} = 15, 20, 25, 35, 45	90 @ 45	D, L, P
64K	8Kx8—CS Power-Down	28S	CY7C185	t _{AA} = 15, 20, 25, 35	120/20 @ 15	P, V
64K	8Kx8—CS Power-Down	28S	CY7C185A	t _{AA} = 15, 20, 25, 35, 45	125/40 @ 25	D, L
64K	8Kx8—CS Power-Down	28	CY7C186A	t _{AA} = 15, 20, 25, 35, 45	125/40 @ 25	D, L
64K	8Kx8—CS Power-Down	28	CY7C186	t _{AA} = 20, 25, 35	120/20 @ 15	P
64K	64Kx1—CS Power-Down	22S	CY7C187A	t _{AA} = 15, 20, 25, 35, 45	80/40 @ 25	D, L
64K	64Kx1—CS Power-Down	22S	CY7C187	t _{AA} = 15, 20, 25, 35	90/40 @ 15	P, V
64K	16Kx4—CS Power-Down	22S	CY7C164	t _{AA} = 15, 20, 25, 35	115/40 @ 15	P, V
64K	16Kx4—Output Enable	24S	CY7C166	t _{AA} = 15, 20, 25, 35	115/40 @ 15	P, V
64K	16Kx4—Separate I/O, Transparent Write	28S	CY7C161	t _{AA} = 15, 20, 25, 35	115/40 @ 15	P, V
64K	16Kx4—Separate I/O	28S	CY7C162	t _{AA} = 15, 20, 25, 35	115/40 @ 15	P, V
64K	16Kx4—Separate I/O, Transparent Write	28	CY7C161A	t _{AA} = 15, 20, 25, 35, 45	100/40 @ 20	D, L
64K	16Kx4—Separate I/O	28	CY7C162A	t _{AA} = 15, 20, 25, 35, 45	100/40 @ 20	D, L
64K	16Kx4—CS Power-Down	22	CY7C164A	t _{AA} = 15, 20, 25, 35, 45	100/40 @ 20	D, L
64K	16Kx4—Output Enable	24	CY7C166A	t _{AA} = 15, 20, 25, 35, 45	100/40 @ 20	D, L
72K	8Kx9	28	CY7C182	t _{AA} = 25, 35, 45, 55	140/35 @ 25	P, V, S
256K	32Kx8—CS Power-Down	28	CY7C198	t _{AA} = 25, 35, 45	160/35 @ 25	L, P
256K	32Kx8—CS Power-Down	28S	CY7C199	t _{AA} = 12, 15, 20, 25, 35, 45, 55	170/30 @ 25	D, L, P, V, Z
256K	32Kx8—CS Power-Down (3.3V)	28S	CY7C1399	t _{AA} = 15, 20, 25	60/25 @ 20	P, V
256K	64Kx4—CS Power-Down	24	CY7C194	t _{AA} = 12, 15, 20, 25, 35, 45	160/30 @ 25	D, L, P, V

Note: Please contact a Cypress Representative for product availability.

Dual-Port RAMs (continued)

Size	Organization	Pins	Part Number	Speed (ns)	I _{CC} /I _{SB} (mA @ ns)	Packages
64K	4K x 16—Dual-Port, w/Semaph, Busy, Int	84	CY7C024	t _{AA} = 15, 25, 35	200	J,A
64K	4K x 18—Dual-Port, w/Semaph, Busy, Int	84	CY7C0241	t _{AA} = 15, 25, 35	200	J,A
128K	8K x 16—Dual-Port w/Semaph, Busy, Int	84	CY7C025	t _{AA} = 15, 25, 35	200	J,A
128K	8K x 18—Dual-Port w/Semaph, Busy, Int	84	CY7C0251	t _{AA} = 15, 25, 35	200	J,A
128K	16K x 8—Dual-Port w/Semaph, Busy, Int	68	CY7C006	t _{AA} = 15, 25, 35	200	J,N
128K	16K x 9—Dual-Port w/Semaph, Busy, Int	68	CY7C016	t _{AA} = 15, 25, 35	200	J,N

SRAM Modules – Secondary Cache Subsystems

Size	Organization	Pins	Part Number	Speed (MHz)	I _{CC} /I _{SB} /I _{CCDR} (mA @ ns)	Packages
128K	PCIsSet Secondary Cache	112	CYM7420	f _{max} = 33 MHz	1100	PB
256K	PCIsSet Secondary Cache	112	CYM7421	f _{max} = 33 MHz	1200	PB
128K	PCIsSet Secondary Cache	112	CYM7424	f _{max} = 33 MHz	1000	PB
256K	PCIsSet Secondary Cache	112	CYM7425	f _{max} = 33 MHz	1600	PB
128K	i486 Secondary Cache	128	CYM7450	f _{max} = 33 MHz	900	PM
256K	i486 Secondary Cache	128	CYM7451	f _{max} = 33 MHz	1500	PM
128K	i486 Secondary Cache	112	CYM7427	f _{max} = 33 MHz		
256K	i486 Secondary Cache	112	CYM7428	f _{max} = 33 MHz		
256K	i486 Secondary Cache	128	CYM7491	f _{max} = 33 MHz	1300	PM
128K	i486 Secondary Cache	112	CYM9236	f _{max} = 33 MHz		
256K	i486 Secondary Cache	112	CYM9237	f _{max} = 33 MHz		
256K	Pentium Cache	160	CYM7432	f _{max} = 60 MHz	1300	PB
256K	P54C Cache (Intel™ Neptune)	160	CYM74AP54	f _{max} = 60, 66 MHz		
256K	P54C Cache (Intel Neptune)	160	CYM74SP54	f _{max} = 60, 66 MHz		
512K	P54C Cache (Intel Neptune)	160	CYM74SP55	f _{max} = 60, 66 MHz		
256K	P54C Cache (Intel Triton)	160	CYM74A430	50, 60, 66 MHz		
256K	P54C Cache (Intel Triton)	160	CYM74S430	50, 60, 66 MHz		
512K	P54C Cache (Intel Triton)	160	CYM74S431	50, 60, 66 MHz		
256K	P54C Cache (OPTi Viper)	160	CYM74A550	50, 60, 66 MHz		
256K	P54C Cache (OPTi Viper)	160	CYM74S550	50, 60, 66 MHz		
512K	P54C Cache (OPTi Viper)	160	CYM74S551	50, 60, 66 MHz		
256K	P54C Cache (VLSI 590)	160	CYM74A590	60, 66 MHz		
256K	P54C Cache (VLSI 590)	160	CYM74S590	60, 66 MHz		
512K	P54C Cache (VLSI 590)	160	CYM74S591	60, 66 MHz		

32-Bit Standard SRAM Module Family

Size	Organization	Pins	Part Number	Speed (ns)	I _{CC} /I _{SB} /I _{CCDR} (mA @ ns)	Packages
512K	16K x 32	64	CYM1821	t _{AA} = 12, 15 t _{AA} = 20, 25, 30, 35, 45	960 @ 12 720 @ 20	PM, PZ PM, PZ
2M	64K x 32	64	CYM1831	t _{AA} = 15, 20, 25, 30, 35, 45	720 @ 25	PM, PN, PZ
4M	128K x 32	64	CYM1836	t _{AA} = 20, 25, 30, 35, 45 t _{AA} = 15	480 @ 20 760 @ 15	PM, PZ
8M	256K x 32	64	CYM1841	t _{AA} = 25, 30, 35, 45, 55 t _{AA} = 20 t _{AA} = 15	960 @ 25 1120 @ 20 1600 @ 15	PM, PN, PZ
8M	256K x 32 (72-pin Superset)	72	CYM1841AP7	t _{AA} = 15, 20, 25, 30, 35, 45	960 @ 25 1120 @ 20 1600 @ 15	PM
16M	512K x 32 (72-pin Superset)	72	CYM1846	t _{AA} = 25, 30, 35	800	PM, PZ
32M	1M x 32 (64-pin Superset)	72	CYM1851	t _{AA} = 25, 30, 35	1250 @ 30	PM, PN, PZ

Note: Please contact a Cypress Representative for product availability.

PLDs (continued)

Size	Organization	Pins	Part Number	Speed (ns)	I _{CC} /I _{SB} (mA @ ns)	Packages
PLD24	20RA10—Asynchronous	24S	PLD20RA10	t _{PD} /S/CO = 15/10/15	80	D, H, J, L, P, Q, W
PLD28	7C330—State Machine	28S	CY7C330	f _{MAX} , t _{IS} , t _{CO} = 66 MHz/3ns/12ns	130@50 MHz	D, H, J, L, P, Q, W
PLD28	7C331—Asynchronous, Registered	28S	CY7C331	t _{PD} /S/CO = 20/12/20	120@25 ns	D, H, J, L, P, Q, W
PLD28	7C335—Universal Synchronous	28S	CY7C335	f _{MAX} /t _{IS} = 100 MHz/2ns, 83 MHz/2ns	140	D, H, J, L, P, Q, W

CPLDs

Size	Organization	Pins	Part Number	Speed (ns)	I _{CC} /I _{SB} (mA)	Packages
MAX28	7C344—32 Macrocell	28S	CY7C344/B	t _{PD} /S/CO = 15/9/10, 10/6/5	200/150	D, H, J, P, W
MAX44	7C343—64 Macrocell	44	CY7C343/B	t _{PD} /S/CO = 20/12/12, 12/8/6	135/125	H, J, R
MAX68	7C342—128 Macrocell	68	CY7C342/B	t _{PD} /S/CO = 25/15/14, 12/8/6	250/225	H, J, R
MAX84	7C341—192 Macrocell	84	CY7C341/B	t _{PD} /S/CO = 25/20/16, 15/10/7	380/360	H, J, R
MAX100	7C346—128 Macrocell	84, 100	CY7C346/B	t _{PD} /S/CO = 25/15/14, 15/10/7	250/225	H, J, N, R
FLASH370—44	7C371—32-Macrocell Flash CPLD	44	CY7C371	f _{MAX} /t _S /t _{CO} = 143MHz/6.5 ns/6.5 ns	150/TBD	J, Y, A
FLASH370—44	7C372—64-Macrocell Flash CPLD	44	CY7C372	f _{MAX} /t _S /t _{CO} = 100 MHz/6.5 ns/6.5 ns	180/TBD	J, Y
FLASH370—84	7C373—64-Macrocell Flash CPLD	84, 100	CY7C373	f _{MAX} /t _S /t _{CO} = 100 MHz/6.5 ns/6.5 ns	180/TBD	A, J, G, Y
FLASH370—84	7C374—128-Macrocell Flash CPLD	84, 100	CY7C374	f _{MAX} /t _S /t _{CO} = 100 MHz/6.5 ns/6.5 ns	300/TBD	A, J, G, Y
FLASH370—160	7C375—128-Macrocell Flash CPLD	160	CY7C375	f _{MAX} /t _S /t _{CO} = 100 MHz/6.5 ns/6.5 ns	300/TBD	A, G, U
FLASH370—160	7C376—192-Macrocell Flash CPLD	160	CY7C376	f _{MAX} /t _S /t _{CO} = 83 MHz/10 ns/10 ns	300/TBD	A, G
FLASH370—240	7C377—192-Macrocell Flash CPLD	240	CY7C377	f _{MAX} /t _S /t _{CO} = 83 MHz/10 ns/10 ns	300/TBD	BGA, N, G
FLASH370—160	7C378—256-Macrocell Flash CPLD	160	CY7C378	f _{MAX} /t _S /t _{CO} = 83 MHz/10 ns/10 ns	300/TBD	A, G
FLASH370—240	7C379—256-Macrocell Flash CPLD	240	CY7C379	f _{MAX} /t _S /t _{CO} = 83 MHz/10 ns/10 ns	300/TBD	BGA, N, G

FPGAs

Size	Organization	Pins	Part Number	Speed Grade	I _{CC} /I _{SB} (mA)	Packages
pASIC380—1K	CMOS 8x12, 1K Gates FPGA	44	CY7C381A	-X, -0, -1, -2	I _{SB} = 10	J
pASIC380—1K	CMOS 8x12, 1K Gates FPGA	68, 100	CY7C382A	-X, -0, -1, -2	I _{SB} = 10	A, G, J
pASIC3380—1K 3.3V	3.3V CMOS 8x12, 1K Gates FPGA	44	CY7C3381A	-0, -1	I _{SB} = 2	J
pASIC3380—1K 3.3V	3.3V CMOS 8x12, 1K Gates FPGA	68, 100	CY7C3382A	-0, -1	I _{SB} = 2	A, J
pASIC380—2K	CMOS 12x16, 2K Gates FPGA	68	CY7C383A	-X, -0, -1, -2	I _{SB} = 10	J
pASIC380—2K	CMOS 12x16, 2K Gates FPGA	84, 100	CY7C384A	-X, -0, -1, -2	I _{SB} = 10	A, G, J
pASIC3380—2K 3.3V	3.3V CMOS 12x16, 2K Gates FPGA	68	CY7C3383A	-0, -1	I _{SB} = 10	J
pASIC3380—2K 3.3V	3.3V CMOS 12x16, 2K Gates FPGA	84, 100	CY7C3384A	-0, -1	I _{SB} = 10	A, J
pASIC380—4K	CMOS 16x24, 4K Gates FPGA	84, 100	CY7C385A	-X, -0, -1, -2	I _{SB} = 10	A, J
pASIC380—4K	CMOS 16x24, 4K Gates FPGA	144, 160	CY7C386A	-X, -0, -1, -2	I _{SB} = 10	A, G, U
pASIC3380—4K 3.3V	3.3V CMOS 16x24, 4K Gates FPGA	84, 100	CY7C3385A	-0, -1	I _{SB} = 10	A, J

Note: Please contact a Cypress Representative for product availability.

EPROMs

Size	Organization	Pins	Part Number	Speed (ns)	I _{CC} /I _{SB} (mA @ ns)	Packages
64K	16Kx8—EPROM	24	CY27C64	t _{AA} = 70, 90, 120, 150, 200	100/15	D, J, P, W
128K	16Kx8—EPROM	28	CY27C128	t _{AA} = 45, 55, 70, 90, 120, 150, 200	45/15	D, J, P, W
256K	32Kx8—EPROM	28	CY27C256	t _{AA} = 45, 55, 70, 90, 120, 150, 200	45/15	D, J, P, W, Z (32-Pin)
256K	32Kx8—EPROM	28S	CY27C256T	t _{AA} = 45, 55, 70, 90, 120, 150, 200	45/15	W, Z (28-Pin)
256K	32Kx8—EPROM	28	CY27H256	t _{AA} = 25, 30, 35, 45, 55	50/15	D, J, P, W
512K	64Kx8—EPROM	28	CY27C512	t _{AA} = 70, 90, 120, 150, 200	40/15	D, J, L, P, Q, W, Z
512K	64Kx8—EPROM	28	CY27H512	t _{AA} = 25, 30, 35, 45, 55, 70	50/15	D, H, J, L, P, Q, W, Z
1M	128Kx8—EPROM	32	CY27C010	t _{AA} = 70, 90, 120, 150, 200	40/15	D, H, J, L, P, Q, W, Z
1M	128Kx8—EPROM	32	CY27H010	t _{AA} = 25, 30, 35, 45, 55	50/15	D, H, J, L, P, Q, W, Z

FIFOs

Organization	Pins	Part Number	Speed (ns)	I _{CC} /I _{SB} (mA @ ns)	Packages
64x4	16	CY3341	1.2, 2MHz	45	D, P
64x4	16	CY7C401	5, 10, 15, 25 MHz	75	D, L, P
64x4—w/OE	16	CY7C403	10, 15, 25 MHz	75	D, L, P
64x5	18	CY7C402	5, 10, 15, 25 MHz	75	D, L, P
64x5—w/OE	18	CY7C404	10, 15, 25 MHz	75	D, L, P
64x8—w/OE and Almost Flags	28S	CY7C408A	15, 25, 35 MHz	120	D, L, P, V
64x9—w/Almost Flags	28S	CY7C409A	15, 25, 35 MHz	120	D, L, P, V
256x9—w/Half Full Flag	28	CY7C419	10, 15, 20, 25, 30, 40, 65	120	D, L, P, V
512x9—w/Half Full Flag	28	CY7C420	20, 25, 30, 40, 65	142/30	D, P
512x9—w/Half Full Flag	28S	CY7C421	10, 15, 20, 25, 30, 40, 65	142/30	D, J, L, P, V
512x9—Clocked	28S	CY7C441	14, 20, 30*	140/30	D, J, L, P, V
512x9—Clocked w/Prog. Flags	32	CY7C451	14, 20, 30*	140/30	D, J, L
512x18—Clocked w/Prog. Flags	52	CY7C455	14, 20, 30*	160/40	J, L, N
1Kx9—w/Half Full Flag	28	CY7C424	20, 25, 30, 40, 65	142/30	D, P
1Kx9—w/Half Full Flag	28S	CY7C425	10, 15, 20, 25, 30, 40, 65	142/30	D, J, L, P, V
1Kx18—Clocked w/Prog. Flags	52	CY7C456	14, 20, 30*	160/40	J, L, N
2Kx9—w/Half Full Flag	28	CY7C428	20, 25, 30, 40, 65	142/30	D, P
2Kx9—w/Half Full Flag	28S	CY7C429	10, 15, 20, 25, 30, 40, 65	142/30	D, J, L, P, V
2Kx9—Bidirectional	28S	CY7C439	25, 30, 40, 65	147/40	D, J, L, P
2Kx9—Clocked	28S	CY7C443	14, 20, 30*	140/30	D, J, L, P, V
2Kx9—Clocked w/Prog. Flags	32	CY7C453	14, 20, 30*	140/30	D, J, L
2Kx18—Clocked w/Prog. Flags	52	CY7C457	14, 20, 30*	160/40	J, L, N
4Kx9—w/Half Full Flag	28	CY7C432	25, 30, 40, 65	140/25	D, P
4Kx9—w/Half Full Flag	28S	CY7C433	10, 15, 25, 30, 40, 65	140/25	D, J, L, P, V
8Kx9—w/Half Full Flag	28	CY7C460	15, 25, 40	160	D, J, L, P
8Kx9—w/Prog. Flags	28	CY7C470	15, 25, 40	160	D, J, L, P
16Kx9—w/Half Full Flag	28	CY7C462	15, 25, 40	160	D, J, L, P
16Kx9—w/Prog. Flags	28	CY7C472	15, 25, 40	160	D, J, L, P
32Kx9—w/Half Full Flag	28	CY7C464	15, 25, 40	160	D, J, L, P
32Kx9—w/Prog. Flags	28	CY7C474	15, 25, 40	160	D, J, L, P
64Kx9—Module	28	CYM4208	25, 30, 40	640/100	HD
128Kx9—Module	28	CYM4209	25, 30, 40	640/100	HD
64x9	32	CY7C4421	10, 15, 25, 35	50	J, A

Note: Please contact a Cypress Representative for product availability.

Communication Products

Description	Pins	Part Number	Speed (MHz)	ICC (mA)	Packages
HOTLink Transmitter	28	CY7B923	160–330	70	J, L, S
HOTLink Receiver	28	CY7B933	160–330	130	J, L, S
Serial SONET Transceiver	24	CY7B951	51 & 155	50	S
10-Base 2/S Ethernet Coax Transceiver	16	CY7B8392	10	80	P, J
Fast Ethernet 100 Base-T4 Transceiver	80	CY7C971	10 & 100	—	N
HOTLink Evaluation Card	—	CY9266	160–330	—	C, T, F*
Integrated ATM Transceiver	100	CY7B955	51 & 155	—	N

* Interface: C—Coax; T—twisted pair; F—fiber

Timing Technology Products

Application	Part #	# of PLLs	# of Outputs	Features	Package
Motherboard Frequency Synthesizers	ICD2023	2	7	All PC clocks, 10–80 MHz, 5V	20S
	ICD2025	2	3	PC CPU & System clocks, 1.843–100MHz, 5V	16S
	ICD2027	2	6	All PC clocks, power-down, 0.76–100 MHz, 5V	20S
	ICD2028	3	8	All PC clocks, user-configurable, 0.35–100 MHz, 5V/3.3V	20S
	ICD2093	2	12	Super-Buffer: 8 skew-controlled CPU clocks, 5V	24S
	CY2254	2	14	Pentium Triton chipset compatible: 4 CPU/6 PCI buffered clocks, 3.3V	28S
	CY2255	2	14	OPTi Viper chipset compatible: 1 early/5 CPU/6 PCI buffered clocks, 3.3V	28S
	CY2257	2	14	Ali Aladdin chipset compatible: 1 early/5 CPU/6 PCI buffered clocks, 3.3V	28S
PC Graphics Frequency Synthesizers	CY2291	3	8	All PC clocks, factory EPROM programmable, 5V/3.3V	20S
	ICD2042A	2	3	PC video/memory clocks, addressable, 5V	16S
	ICD2061A	2	2	PC video/memory clocks, user-programmable, 5V	16S
	ICD2062B	2	6	PECL video clock for workstations, 0.5–165 MHz, 5V	20S
	ICD2063	2	2	PC video/memory clocks, user-programmable, 5V/3.3V	16S
General Purpose Programmable Products	ICD2051	2	5	User-programmable dual PLL, 0.3–120 MHz, 5V	16S
	ICD2053B	1	1	User-programmable single PLL, 0.4–100 MHz, 5V	8S
QuiXTAL Embedded Crystal Products	ICD6233	1	1	Metal can oscillator package, field programmable	—
Programmable Skew Clock Buffer (TTL Output)	CY7B991	1	8	3–80 MHz, Programmable Skew (700 ps increments)	J, L
Programmable Skew Clock Buffer (CMOS Output)	CY7B992	1	8	3–80 MHz, Programmable Skew (700 ps increments)	J, L

PC Chipsets

Description	Pins	Part Number	Package
Single-chip solution for 486-based systems with Green features. Supports SMI/CPU interface/cache control/DRAM control/ISA Bus control/VESA control	160	CY82C597	N
Intelligent PCI Bus Bridge Chip. Connects ISA Bus to the PCI Bus.	160	CY82C599	N

Note: Please contact a Cypress Representative for product availability.

FCT2-T Octal Logic Products with Resistor ($V_{CC}=5$ Volts)

Part Number	Organization	Pins	Propagation Delays (ns)								Packages	
			C		B		A		Standard			
			Com'l	Mil	Com'l	Mil	Com'l	Mil	Com'l	Mil		
CY54/74FCT2240T	8-Bit Inverting Buffer/Line Driver with \overline{OE} and 25 Ω Resistor	20	4.3					4.8	5.1	8.0	9.0	D, L, P, Q, SO
CY54/74FCT2244T	8-Bit Buffer/Line Driver with \overline{OE} and 25 Ω Resistor	20	4.1					4.8	5.1	6.5	7.0	D, L, P, Q, SO
CY54/74FCT2245T	8-Bit Transceiver with \overline{OE} and 25 Ω Resistor	20	4.1					4.6	4.9	7.0	7.5	D, L, P, Q, SO
CY54/74FCT2257T	Quad 2-input Multiplexers with \overline{OE} and 25 Ω Resistor	16	4.3					5.0	5.8	6.0	7.0	D, L, P, Q, SO
CY54/74FCT2373T	8-Bit Latch with \overline{OE} and 25 Ω Resistor	20	4.7	5.1				5.2	5.6	8.0	8.5	D, L, P, Q, SO
CY54/74FCT2374T	8-Bit Register with \overline{OE} and 25 Ω Resistor	20	5.2	6.0				6.5	7.2	10.0	11.0	D, L, P, Q, SO
CY54/74FCT2541T	8-Bit Buffer/Line Driver with \overline{OE} , Flow-Through Pinout and 25 Ω Resistor	20	4.1	4.6				4.8	5.1	8.0	9.0	D, L, P, Q, SO
CY54/74FCT2543T	8-Bit Latched Transceiver with \overline{OE} and 25 Ω Resistor	24	5.5	6.1				6.5	7.5	8.5	10.0	D, L, P, Q, SO
CY54/74FCT2573T	8-Bit Latch with \overline{OE} , Flow-Through Pinout and 25 Ω Resistor	20	4.7	5.1				5.2	5.6	8.0	8.5	D, L, P, Q, SO
CY54/74FCT2574T	8-Bit Register with \overline{OE} , Flow-Through Pinout and 25 Ω Resistor	20	5.2	6.0				6.5	7.2	10.0	11.0	D, L, P, Q, SO
CY54/74FCT2646T	8-Bit Registered Transceiver with \overline{OE} and 25 Ω Resistor	24	5.4	6.0				6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT2648T	8-Bit Inverting Registered Transceiver with \overline{OE} and 25 Ω Resistor	24	5.4	6.0				6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT2652T	8-Bit Registered Transceiver with \overline{OE} and 25 Ω Resistor	24	5.4	6.0				6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT2827T	10-Bit Buffer with \overline{OE} and 25 Ω Resistor	24	4.4	5.0	5.0	6.5	8.0	9.0				D, L, P, Q, SO

FCT16 16-Bit High Drive Logic Products ($V_{CC}=5$ Volts)

Part Number	Organization	Pins	Propagation Delays (ns)				Package
			C	B	A	Standard	
			Com'l	Com'l	Com'l	Com'l	
CY74FCT16240T	16-Bit Inverting Buffer/Line Driver with \overline{OE}	48	4.3		4.8	8.0	PA, PV
CY74FCT16244T	16-Bit Buffer/Line Driver with \overline{OE}	48	4.1		4.8	6.5	PA, PV
CY74FCT16245T	16-Bit Transceiver with \overline{OE}	48	4.1		4.6	7.0	PA, PV
CY74FCT16373T	16-Bit Latch with \overline{OE}	48	4.2		5.2	8.0	PA, PV
CY74FCT16374T	16-Bit Register with \overline{OE}	48	5.2		6.5	10.0	PA, PV
CY74FCT16444T	16-Bit 244 with Single \overline{OE}	48	4.1		4.8	6.5	PA, PV
CY74FCT16445T	16-Bit 245 with Single \overline{OE} and DIR	48	4.1		4.6	7.0	PA, PV
CY74FCT16500T	18-Bit Universal Bus Transceiver	56	4.6		5.1		PA, PV
CY74FCT16501T	18-Bit Universal Bus Transceiver	56	4.6		5.1		PA, PV
CY74FCT16543T	16-Bit Latched Transceiver with \overline{OE}	56	5.3		6.5	8.5	PA, PV
CY74FCT16646T	16-Bit Registered Transceiver with \overline{OE}	56	5.4		6.3	9.0	PA, PV
CY74FCT16652T	16-Bit Registered Transceiver with \overline{OE}	56	5.4		6.3	9.0	PA, PV
CY74FCT16823T	18-Bit Register with \overline{OE}	56	6.0	7.5	10.0		PA, PV
CY74FCT16827T	20-Bit Buffer with \overline{OE}	56	4.4	5.0	8.0		PA, PV
CY74FCT16841T	20-Bit Latch with \overline{OE}	56	5.5	6.5	9.0		PA, PV
CY74FCT16952T	16-Bit Registered Transceiver	56	6.3	7.5	10.0		PA, PV

Note: Please contact a Cypress Representative for product availability.



Product Selector Guide

FCT2 Octal Logic Products with Resistor ($V_{CC}=5$ Volts)

Part Number	Organization	Pins	Propagation Delays (ns)								Packages	
			C		B		A		Standard			
			Com'l	Mil	Com'l	Mil	Com'l	Mil	Com'l	Mil		
CY54/74FCT2240T	8-Bit Inverting Buffer/Line Driver with \overline{OE} and 25 Ω Resistor	20	4.3					4.8	5.1	8.0	9.0	D, L, P, Q, SO
CY54/74FCT2244T	8-Bit Buffer/Line Driver with \overline{OE} and 25 Ω Resistor	20	4.1					4.8	5.1	6.5	7.0	D, L, P, Q, SO
CY54/74FCT2245T	8-Bit Transceiver with \overline{OE} and 25 Ω Resistor	20	4.1					4.6	4.9	7.0	7.5	D, L, P, Q, SO
CY54/74FCT2257T	Quad 2-input Multiplexers with \overline{OE} and 25 Ω Resistor	16	4.3					5.0	5.8	6.0	7.0	D, L, P, Q, SO
CY54/74FCT2373T	8-Bit Latch with \overline{OE} and 25 Ω Resistor	20	4.7	5.1				5.2	5.6	8.0	8.5	D, L, P, Q, SO
CY54/74FCT2374T	8-Bit Register with \overline{OE} and 25 Ω Resistor	20	5.2	6.0				6.5	7.2	10.0	11.0	D, L, P, Q, SO
CY54/74FCT2541T	8-Bit Buffer/Line Driver with \overline{OE} , Flow-Through Pinout and 25 Ω Resistor	20	4.1	4.6				4.8	5.1	8.0	9.0	D, L, P, Q, SO
CY54/74FCT2543T	8-Bit Latched Transceiver with \overline{OE} and 25 Ω Resistor	24	5.5	6.1				6.5	7.5	8.5	10.0	D, L, P, Q, SO
CY54/74FCT2573T	8-Bit Latch with \overline{OE} , Flow-Through Pinout and 25 Ω Resistor	20	4.7	5.1				5.2	5.6	8.0	8.5	D, L, P, Q, SO
CY54/74FCT2574T	8-Bit Register with \overline{OE} , Flow-Through Pinout and 25 Ω Resistor	20	5.2	6.0				6.5	7.2	10.0	11.0	D, L, P, Q, SO
CY54/74FCT2646T	8-Bit Registered Transceiver with \overline{OE} and 25 Ω Resistor	24	5.4	6.0				6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT2648T	8-Bit Inverting Registered Transceiver with \overline{OE} and 25 Ω Resistor	24	5.4	6.0				6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT2652T	8-Bit Registered Transceiver with \overline{OE} and 25 Ω Resistor	24	5.4	6.0				6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT2827T	10-Bit Buffer with \overline{OE} and 25 Ω Resistor	24	4.4	5.0	5.0	6.5	8.0	9.0				D, L, P, Q, SO

Notes:

The above specifications are for the commercial temperature range of 0°C to 70°C. Military temperature range (-55°C to +125°C) product processed to MIL-STD-883 Revision C is also available for most products. Speed and power selections may vary from those above. Contact your local sales office for more information.

Commercial grade product is available in plastic, CERDIP, or LCC. Military grade product is available in CERDIP, LCC, or PGA.

Power supplies for most product lines are $V_{CC} = 5V \pm 10\%$.

22S, 24S, 28S stands for 300 mil, 22-pin, 24-pin, 28-pin, respectively. 28.4 stands for 28-pin 400 mil, 24.4 stands for 24-pin 400 mil.

PLCC, SOJ, and SOIC packages are available on some products.

F, K, and T packages are special order only.

Please contact a Cypress representative for product availability.

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Package Code:

B = Plastic Pin Grid Array
 D = CerDIP
 E = Tape Automated Bond (TAB)
 F = Flatpack
 G = Pin Grid Array (PGA)
 H = Windowed Hermetic LCC
 J = PLCC
 K = Cerpack
 L = Leadless Chip Carrier (LCC)
 N = Plastic Quad Flatpack
 P = Plastic

Q = Windowed LCC
 Q = QSOP
 R = Windowed PGA
 S = SOIC
 T = Windowed Cerpack
 U = Ceramic Quad Flatpack
 V = SOJ
 W = Windowed Cerdip
 X = DICE
 Y = Ceramic LCC
 Z = TSOP

HD = Hermetic DIP (Module)
 HG = Ceramic PGA (Module)
 PA = TSSOP
 PD = Plastic DIP (Module)
 PM = Plastic SIMM
 PN = Plastic Angled SIMM
 PS = Plastic SIP
 PV = SSOP
 PZ = Plastic ZIP
 SO = SOIC

Document #: 38-00237-E

Note: Please contact a Cypress Representative for product availability.



Product Line Cross Reference

ALTERA	CYPRESS
5032PC-2	7C344-20PC
5032PC-15	7C344-15PC
5032PC-17	Call Factory
5032PC-20	7C344-20PC
5032PC-25	7C344-25PC
5064JC	7C343-35HC
5064JC-1	7C343-25HC
5064JC-2	7C343-30HC
5064JI	7C343-35HI
5064JM	7C343-35HMB
5064LC	7C343-35JC
5064LC-1	7C343-25JC
5064LC-2	7C343-30JC
5128AGC-12	7C342B-12RC
5128AGC-15	7C342B-15RC
5128AGC-20	7C342B-20RC
5128AJC-12	7C342B-12HC
5128AJC-15	7C342B-15HC
5128AJC-20	7C342B-20HC
5128ALC-12	7C342B-12JC
5128ALC-15	7C342B-15JC
5128ALC-20	7C342B-20JC
5128GC	7C342-35RC
5128GC-1	7C342-25RC
5128GC-2	7C342-30RC
5128GM	7C342-35RMB
5128JC	7C342-35HC
5128JC-1	7C342-25HC
5128JC-2	7C342-30HC
5128JI	7C342-35HI
5128JI-2	7C342-30HI
5128JM	7C342-35HMB
5128LC	7C342-35JC
5128LC-1	7C342-25JC
5128LC-2	7C342-30JC
5128LI	7C342-35JI
5128LI-2	7C342-30JI
5130GC	7C346-35RC
5130GC-1	7C346-25RC
5130GC-2	7C346-30RC
5130GM	7C346-35RMB
5130JC	7C346-35HC
5130JC-1	7C346-25HC
5130JC-2	7C346-30HC
5130JM	7C346-35HMB
5130LC	7C346-35JC
5130LC-1	7C346-25JC
5130LC-2	7C346-30JC
5130LI	7C346-35JI
5130LI-2	7C346-30JI
5130QC	7C346-35NC
5130QC-1	7C346-25NC
5130QC-2	7C346-30NC
5130QI	7C346-35NI
5192AGC-15	7C341B-15RC
5192AGC-20	7C341B-20RC
5192AJC-15	7C341B-15HC
5192AJC-20	7C341B-20HC
5192ALC-1	7C341B-15JC
5192ALC-2	7C341B-20JC
5192GC	7C341-35RC
5192GC-1	7C341-25RC

ALTERA	CYPRESS
5192GC-2	7C341-30RC
5192JC	7C341-35HC
5192JC-1	7C341-25HC
5192JC-2	7C341-30HC
5192JI	7C341-35HI
5192LC	7C341-35JC
5192LC-1	7C341-25JC
5192LC-2	7C341-30JC

ALTERA	CYPRESS
PREFIX: Am	PREFIX: CY
PREFIX: SN	PREFIX: CY
SUFFIX: B	SUFFIX: B
SUFFIX: D	SUFFIX: W
SUFFIX: E	SUFFIX: Z
SUFFIX: F	SUFFIX: F
SUFFIX: J	SUFFIX: J
SUFFIX: L	SUFFIX: L
SUFFIX: P	SUFFIX: P
27C64-55C	7C266-55C
27C64-70C	27C64-70C
27C64-90C	27C64-90C
27C64-120C	27C64-120C
27C64-150C	27C64-150C
27C64-200C	27C64-200C
27C010-90C	27C010-90C
27C010-120C	27C010-120C
27C010-150C	27C010-150C
27C010-200C	27C010-200C
27C128-45C	27C128-45C
27C128-55C	27C128-55C
27C128-70C	27C128-70C
27C128-90C	27C128-90C+
27C128-120C	27C128-120C+
27C128-150C	27C128-150C+
27C128-200C	27C128-200C+
27C256-55C	27C256-55C
27C256-70C	27C256-70C+
27C256-90C	27C256-90C+
27C256-120C	27C256-120C+
27C256-150C	27C256-150C+
27C256-200C	27C256-200C+
27C512-75C	27H512-70C
27C512-90C	27H512-90C
27C512-120C	27H512-120C
27C512-150C	27H512-150C
27C512-200C	27H512-200C
27H010-45	27H010-45
27H010-55	27H010-55
27H010-70	27C010-70
27H010-90	27C010-90
27H256-35C	27H256-35C
27H256-45C	27C256-45C
27H256-45M	27C256-45M
27H256-55C	27C256-55C
27H256-55M	27C256-55M
27H256-70C	27C256-70C
27LS291M	7C291A-35M
27PS191AC	7C292A-50C
27PS191AM	7C292A-50M+
27PS191C	7C292A-50C
27PS191M	7C292A-50M+
27PS291AC	7C293A-50C

AMD	CYPRESS
27PS291AM	7C293A-50M+
27PS291C	7C293A-50C
27PS291M	7C293A-50M+
27S181AC	7C282A-30C
27S181AM	7C282A-45M
27S181C	7C282A-45C
27S181M	7C282A-45M
27S191AC	7C292A-35C
27S191AM	7C292A-50M
27S191C	7C292A-50C
27S191M	7C292A-50M
27S191SAC	7C292A-25C
27S191SAM	7C292A-30M
27S25AC	7C225A-30C
27S25AM	7C225A-35M
27S25C	7C225A-40C
27S25M	7C225A-40M
27S25SAC	7C225A-25C
27S25SAM	7C225A-30M
27S43AC	7C244-45C
27S43C	7C244-55C
27S281AC	7C281A-30C
27S281AM	7C281A-45M
27S281C	7C281A-45C
27S281M	7C281A-45M
27S291AC	7C291A-35C
27S291AM	7C291A-50M
27S291C	7C291A-50C
27S291M	7C291A-50M
27S291SAC	7C291A-25C
27S291SAM	7C291A-30M
27S35AC	7C235A-30C
27S35AM	7C235A-40M
27S35C	7C235A-40C
27S35M	7C235A-40M
27S45AC	7C245A-35C
27S45AM	7C245A-45M
27S45C	7C245A-45C
27S45M	7C245A-45M
27S45SAC	7C245A-25C
27S45SAM	7C245A-25M-
27S49A	7C264-40C
27S49AM	7C264-55M
27S49C	7C264-55C
27S49M	7C264-55M
27S49SAC	7C264-25C
27S49SAM	7C264-25M
2841AC	3341C
2841AM	3341M
2841C	3341C
2841M	3341M
7201-25	7C420-25
7201-25R	7C421-25
7201-35	7C420-30
7201-35R	7C421-30
7201-50	7C420-40
7201-50R	7C421-40
7201-65	7C420-65
7201-65R	7C421-65
7201-80	7C420-80
7201-80R	7C421-80
7202A-15	7C425A-15

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

- + = meets all performance specs but may not meet I_{CC} or I_{SB}
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Product Line Cross Reference

ANALOG DEV	CYPRESS
PREFIX: ADSP	PREFIX: CY
SUFFIX: 883B	SUFFIX: B
SUFFIX: D	SUFFIX: D
SUFFIX: E	SUFFIX: L
SUFFIX: F	SUFFIX: F
SUFFIX: G	SUFFIX: G

ATMEL	CYPRESS
PREFIX: AT	PREFIX: CY
SUFFIX: D	SUFFIX: W
SUFFIX: K	SUFFIX: H
SUFFIX: L	SUFFIX: Q
SUFFIX: J	SUFFIX: J
SUFFIX: P	SUFFIX: P
SUFFIX: T	SUFFIX: Z
22V10	PALC22V10
22V10-15	PALC22V10B
27C010-45C	27H010-45C
27C010-55C	27H010-55C
27C010-70C	27C010-50C
27C010-90C	27C010-90C
27C010-120C	27C010-120C
27C010-150C	27C010-150C
27C010-200C	27C010-200C
27C512-70C	27H512-70C
27C512-90C	27C512-90C
27C512-120C	27C512-120C
27C512-150C	27C512-150C
27C512-200C	27C512-200C
27C256R-70C	27C256-70C
27C256R-90C	27C256-90C+
27C256R-120C	27C256-120C+
27C256R-150C	27C256-150C+
27C256R-200C	27C256-200C+
27HC256R-35C	27C256-35C
27HC256R-45C	27C256-45C
27HC256R-55C	27C256-55C
27HC256R-70C	27C256-70C
27HC256R-70M	27C256-70M
27HC641-35C	7C264-35C
27HC641-45C	7C264-45C
27HC641-45M	7C264-45M
27HC641-55C	7C264-55C
27HC641-55M	7C264-55M
27HC641-70C	7C264-70C
27HC642-35C	7C261-35C
27HC642-45C	7C261-45C
27HC642-45M	7C261-45M
27HC642-55C	7C261-55C
27HC642-55M	7C261-55M
27HC642-70C	7C261-55C

AUSTIN SEMICONDUCTOR	CYPRESS
PREFIX: MT	PREFIX: CY
5C1608-25M	7C128A-25M
5C1608-30M	7C128A-25M
5C1608-35M	7C128A-35M
5C2561-25M	7C197-25MB
5C2561-35M	7C197-35MB
5C2561-45M	7C197-45MB
5C2564-25M	7C194-25MB
5C2564-35M	7C194-35MB

AUSTIN SEMICONDUCTOR	CYPRESS
5C2564-45M	7C194-45MB
5C2568-25M	7C199-25MB
5C2568-35M	7C199-35MB
5C2568-45B	7C199-45MB
5C2568CW-25M	7C198-25MB
5C2568CW-35M	7C198-35MB
5C2568CW-45B	7C198-45MB
5C2568W-25M	7C198-25MB
5C2568W-35M	7C198-35MB
5C2568W-45B	7C198-45MB
5C6401-20M	7C187A-20MB
5C6401-25M	7C187A-25MB
5C6401-30M	7C187A-25MB
5C6401-35M	7C187A-35MB
5C6404-20M	7C164A-20MB
5C6404-25M	7C164A-25MB
5C6404-30M	7C164A-25MB
5C6404-35M	7C164A-35MB
5C6408-20M	7C185A-20MB
5C6408-25M	7C185A-25M
5C6408-30M	7C185A-25MB
5C6408-35M	7C185A-35MB

CATALYST	CYPRESS
PREFIX: CAT	PREFIX: CY
27HC256-55L	27C256-55C+
27HC256-70L	27C256-70C+
27HC256-90L	27C256-70C+
27HC256-120L	27C256-120C+
27HC256/LI-55	27C256-55C/I
27HC256/LI-70	27C256-70C/I

DALLAS	CYPRESS
PREFIX: DS	PREFIX: CY
2009	7C421-25C
2010	7C425-25C
2011	7C429-25C

DENSEPAK	CYPRESS
PREFIX: DPS	PREFIX: CYM
6432-45C	1830HD-45C
6432-55C	1830HD-55C

EDI	CYPRESS
PREFIX: ED	PREFIX: CYM
8464C-45	7C194-45
8F32256C	1841PZ
8F3264C	1831PZ
8F8512CXXBC	1465PC-XXC
8F8512LPXXB6C	1465LPD-XXC
8F8512PXXXB6C	1465LPD-XXC
8M3264CXXC6B	M1830HD-XXMB
8M3264CXXC6C	M1830HD-XXC
8M32256CXXC6B	M1840HD-XXMB
8M32256CXXC6B	M1840HD-XXC
8M8512CXXM6C	1464PD-XXC

FUJITSU	CYPRESS
PREFIX: MB	PREFIX: CY
PREFIX: MBM	PREFIX: CY
SUFFIX: F	SUFFIX: F
SUFFIX: M	SUFFIX: P
SUFFIX: Z	SUFFIX: D

FUJITSU	CYPRESS
2147H-35	2147-35C
2147H-45	2147-45C
2149-45	2149-45C
27C128-170C	27C128-150C+
27C128-200C	27C128-200C+
27C128-250C	27C128-200C+
27C256A-150C	27C256-150C+
27C256A-170C	27C256-150C+
27C256A-200C	27C256-200C+
7132E	7C282A-45C
7132E-SK	7C281A-45C
7132E-W	7C282A-45M
7132H	7C282A-45C
7132H-SK	7C281A-45C
7132L-70	7C281A-45C
7132Y	7C282A-30C
7132Y-SK	7C281A-30C
7138E-55	7C291/2A-50C
7138E-W	7C291/2A-50M
7138H-45	7C291/2A-35C
7138Y-35	7C291/2A-35C
7144E	7C264-55C
7144E-W	7C264-55M
7144H	7C264-55C
71A38-25	7C291/2A-25C
71A38-35	7C291/2A-35C
71C44-35	7C264-35C
71C44-45	7C264-45C
71C46-45	7C254-45C
7226RA/S-25	7C225A-25C
7232RA-25	7C235A-25C
7238RA-20	7C245A-18C
7238RA-20-W	7C245A-18M
7238RA-25	7C245A-25C
7238RA-25-W	7C245A-25M
8128-10	7C128A-55C
8128-15	7C128A-55C
8167-70W	7C167A-45M
8167A-55	7C167A-45C
8167A-70	7C167A-45C
8168-55	7C168A-45C
8171-55	7C187-45C
8171-70	7C187-45C
81C67-35	7C167A-35C
81C67-45	7C167A-45C
81C67-55W	7C167A-45M
81C68-45	7C168A-45C
81C68-55W	7C168A-45M+
81C71-45	7C187-45C
81C71-55	7C187-45C
81C74-25	7C164-25C
81C74-35	7C164-35C+
81C74-45	7C164-45C
81C75-25	7C166-25C
81C75-35	7C166-35C
81C78-45	7C186-45C
81C78-55	7C186-55C
81C81A-35	7C197-35
81C81A-45	7C197-45
81C84A-35	7C194-35
81C84A-45	7C194-45
81C86-70	7C192-45C+

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

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- * = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}
- = functionally equivalent
- † = SOIC only
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Product Line Cross Reference

IDT	CYPRESS	IDT	CYPRESS	IDT	CYPRESS
6198SA20B	7C166-A20MB	71281SA35B	7C191-35MB	71321LA55	7C136-55C
6198SA25	7C166-25C	71281SA45	7C191-45C	71321LA55B	7C136-55MB
6198SA25B	7C166-A25MB	71281SA45B	7C191-45MB	71321LA70	7C136-55C
6198SA30B	7C166A-25MB	71282SA25	7C192-25C	71321LA70B	7C136-55MB
61B298S12	7C195-12C	71282SA25B	7C192-25MB	71321LA90	7C136-55C
61B298S15	7C195-15C	71282SA35	7C192-35C	71321LA90B	7C136-55MB
61B298S20	7C195-20C	71282SA35B	7C192-35MB	71321SA25	7C136-25C
61B298S15B	7C195-15MB	71282SA45	7C192-45C	71321SA30	7C136-30C
61B298S20B	7C195-20MB	7130LA25	7C130-25C	71321SA35	7C136-35C
7005S35	7B144-25C	7130LA25J	7C131-25JC	71321SA35B	7C136-35MB
7005S35	7B144-35C	7130LA30	7C130-30C	71321SA45	7C136-45C
7005S45B	7B144-35MB	7130LA30J	7C131-30JC	71321SA45B	7C136-45MB
7006S25	7006S25C	7130LA35	7C130-35C	71321SA55	7C136-55C
7006S35	7006S35C	7130LA35B	7C130-35MB	71321SA55B	7C136-55MB
7015S25	7C145-25C	7130LA35J	7C131-35JC	71321SA70	7C136-55C
7015S35	7C145-35C	7130LA35LB	7C130-35LMB	71321SA70B	7C136-55MB
7016S25	7C016-25C	7130LA45	7C130-45C	71321SA90	7C136-55C
7016S35	7C016-35C	7130LA45B	7C131-45MB	71321SA90B	7C136-55MB
7024S25	7C024-25C	7130LA45J	7C131-45JC	713256-20	7C1399-20C
7024S35	7C024-35C	7130LA45LB	7C130-45LMB	713256-25	7C1399-25C
7025S25	7C025-25C	7130LA55	7C130-55C	7132LA25	7C132-25C
7025S35	7C025-35C	7130LA55B	7C131-55MB	7132LA30	7C132-30C
7133S25	7C133-25C	7130LA55J	7C131-55JC	7132LA35	7C132-35C
7133S35	7C133-35C	7130LA55L52B	7C130-55LMB	7132LA35B	7C132-35MB
7143S25	7C143-25C	7130LA70	7C130-55C	7132LA45	7C132-45C
7143S35	7C143-35C	7130LA70B	7C131-55MB	7132LA45B	7C132-45MB
71V256-15	7C1399-15C	7130LA70J	7C131-55JC	7132LA55	7C132-55C*
71V256-20	7C1399-20C	7130LA70LB	7C130-55LMB	7132LA55B	7C132-55MB
71V256-25	7C1399-25C	7130LA90LB	7C131-55LMB	7132LA70	7C132-55C*
71024-15	7C109A-15C	7130SA25	7C130-25C	7132LA70B	7C132-55M*
71024-20	7C109A-20C	7130SA25J	7C131-25JC	7132LA90	7C132-55C*
71024-20	7C109-20C	7130SA30	7C130-25C	7132LA90B	7C132-55M*
71024-25	7C109-25C	7130SA30J	7C131-30JC	7132LA100	7C132-55C*
71028-15	7C106A-15C	7130SA35	7C130-35C	7132LA100B	7C132-55M*
71028-20	7C106A-20C	7130SA35B	7C130-35MB	7132LA120B	7C132-55M*
71028-25	7C106A-25C	7130SA35J	7C131-35JC	7132SA25	7C132-25C
71256SA15	7C199-15C	7130SA35LB	7C131-35LMB	7132SA30	7C132-30C
71256SA20	7C199-20C	7130SA45	7C130-45C	7132SA35	7C132-35C
71256SA20B	7C199-20MB	7130SA45B	7C130-45MB	7132SA35B	7C132-35MB
71256SA25	7C198-25C	7130SA45J	7C131-45JC	7132SA45	7C132-45C
71256SA30	7C198-25C	7130SA45LB	7C131-45LMB	7132SA45B	7C132-45MB
71256SA30B	7C198-25MB	7130SA55	7C130-55C	7132SA55	7C132-55C+
71256SA35	7C198-35C	7130SA55B	7C130-55MB	7132SA55B	7C132-55MB
71256SA35B	7C198-35MB	7130SA55J	7C131-55JC	7132SA70	7C132-55C+
71256SA45	7C198-45C	7130SA55LB	7C131-55LMB	7132SA70B	7C132-55M+
71256SA45B	7C198-45MB	7130SA70	7C130-55C	7132SA90	7C132-55C+
71257SA25	7C197-25C	7130SA70B	7C130-55MB	7132SA90B	7C132-55M+
71257SA25B	7C197-25MB	7130SA70J	7C131-55JC	7132SA100	7C132-55C+
71257SA35	7C197-35C	7130SA70LB	7C131-55LMB	7132SA100B	7C132-55M+
71257SA35B	7C197-35MB	7130SA90	7C130-55C	7132SA120B	7C132-55M+
71257SA45	7C197-45C	7130SA90B	7C130-55MB	71342S35	7C1342-25C
71257SA45B	7C197-45MB	7130SA90J	7C131-55JC	71342S35	7C1342-35C
71257SA55	7C197-45C	7130SA90LB	7C131-55LMB	71342S45B	7C1342-35MB
71258SA25	7C194-25C	7130SA100	7C130-55C	7134S35	7B134-25C
71258SA25B	7C194-25MB	7130SA100B	7C130-55MB	7134S35	7B134-35C
71258SA35	7C194-35C	7130SA100LB	7C131-55LMB	7134S35J52	7B135-25JC
71258SA35B	7C194-35MB	71321LA25	7C136-25C	7134S35J52	7B135-35JC
71258SA45	7C194-45C	71321LA30	7C136-30C	7134S35L52	7B135-25LC
71258SA45B	7C194-45MB	71321LA35	7C136-35C	7134S35L52	7B135-35LC
71281SA25	7C191-25C	71321LA35B	7C136-35MB	7134SA45B	7B134-35MB
71281SA25B	7C191-25MB	71321LA45	7C136-45C	7134S45L52B	7B135-35LMB
71281SA35	7C191-35C	71321LA45B	7C136-45MB	7140LA25	7C140-25C

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Product Line Cross Reference

IDT	CYPRESS
7200SA50T	7C419-50
7200SA65T	7C419-65
7200SA80T	7C419-65
7201LA15	7C421-15
7201LA20	7C420-20C
7201LA20T	7C421-20C
7201LA25	7C420-25C
7201LA25T	7C421-25C
7201LA30B	7C420-30MB
7201LA30TB	7C421-30MB
7201LA35	7C420-30C+
7201LA35T	7C421-30C
7201LA40B	7C420-40MB+
7201LA40TB	7C421-40MB
7201LA50	7C420-40C+
7201LA50B	7C420-40MB+
7201LA50T	7C421-40C
7201LA50TB	7C421-40MB
7201LA65	7C420-65C+
7201LA65B	7C420-65MB+
7201LA65T	7C421-65C
7201LA65TB	7C421-65MB
7201LA80	7C420-65C+
7201LA80B	7C420-65MB+
7201LA120	7C420-65C+
7201LA120B	7C420-65MB+
7201SA15	7C421-15
7201SA20	7C420-20C
7201SA20T	7C421-20C
7201SA25	7C420-25C
7201SA25T	7C421-25C
7201SA30B	7C420-30MB
7201SA30TB	7C421-30MB
7201SA35	7C420-30C
7201SA35T	7C421-30C
7201SA40B	7C420-40MB
7201SA40TB	7C421-40MB
7201SA50	7C420-40C
7201SA50B	7C420-40MB
7201SA50T	7C421-40C
7201SA50TB	7C421-40MB
7201SA65	7C420-65C
7201SA65B	7C420-65MB
7201SA65T	7C421-65C
7201SA65TB	7C421-65MB
7201SA80	7C420-65C
7201SA80B	7C420-65MB
7201SA120	7C420-65C
7201SA120B	7C420-65MB
7202LA15	7C425-15
7202LA20	7C424-20C
7202LA20T	7C425-20C
7202LA25	7C424-25C
7202LA25T	7C425-25C
7202LA30B	7C424-30MB
7202LA30TB	7C425-30MB
7202LA35	7C424-30C+
7202LA35T	7C425-30C
7202LA40B	7C424-40MB+
7202LA40TB	7C425-40MB
7202LA50	7C424-40C+
7202LA50B	7C424-40MB+

IDT	CYPRESS
7202LA50T	7C425-40C
7202LA50TB	7C425-40MB
7202LA65	7C424-65C+
7202LA65B	7C424-65MB+
7202LA65T	7C425-65C
7202LA65TB	7C425-65MB
7202LA80	7C424-65C+
7202LA80B	7C424-65MB+
7202LA120	7C424-65C+
7202LA120B	7C424-65MB+
7202SA15	7C425-15
7202SA20	7C424-20C
7202SA20T	7C425-20C
7202SA25	7C424-25C
7202SA25T	7C425-25C
7202SA30B	7C424-30MB
7202SA30TB	7C425-30MB
7202SA35	7C424-30C
7202SA35T	7C425-30C
7202SA40B	7C424-40MB
7202SA40TB	7C425-40MB
7202SA50	7C424-40C
7202SA50B	7C424-40MB
7202SA50T	7C425-40C
7202SA50TB	7C425-40MB
7202SA65	7C424-65C
7202SA65B	7C424-65MB
7202SA65T	7C425-65C
7202SA65TB	7C425-65MB
7202SA80	7C424-65C
7202SA80B	7C424-65MB
7202SA120	7C424-65C
7202SA120B	7C424-65MB
7203L20	7C428-20C
7203L20T	7C429-20C
7203L25	7C428-25C
7203L25B	7C428-25MB
7203L25T	7C429-25C
7203L25TB	7C429-25MB
7203L30	7C428-30C
7203L30T	7C429-30C
7203L35B	7C428-30MB
7203L35TB	7C429-30MB
7203L40	7C428-40C
7203L40T	7C429-40C
7203L55B	7C428-40MB
7203L55TB	7C429-40MB
7203L65	7C428-65C
7203L65B	7C428-65MB
7203L65T	7C429-65C
7203L65TB	7C429-65MB
7203L80	7C428-80C
7203L80B	7C428-80MB
7203L80T	7C429-80C
7203L80TB	7C429-80MB
7203S20	7C428-20C
7203S20T	7C429-20C
7203S25	7C428-25C
7203S25B	7C428-25MB
7203S25T	7C429-25C
7203S25TB	7C429-25MB
7203S30	7C428-30C

IDT	CYPRESS
7203S30T	7C429-30C
7203S35B	7C428-30MB
7203S35TB	7C429-30MB
7203S40	7C428-40C
7203S40T	7C429-40C
7203S55B	7C428-40MB
7203S55TB	7C429-40MB
7203S65	7C428-65C
7203S65B	7C428-65MB
7203S65T	7C429-65C
7203S65TB	7C429-65MB
7203S80	7C428-80C
7203S80B	7C428-80MB
7203S80T	7C429-80C
7203S80TB	7C429-80MB
7204S25	7C432-25C
7204S25T	7C433-25C
7204S30	7C432-30C
7204S30T	7C433-30C
7204S35B	7C432-30MB
7204S35TB	7C433-30MB
7204S40	7C432-40C
7204S40T	7C433-40C
7204S55B	7C432-40MB
7204S55TB	7C433-40MB
7204S65	7C432-65C
7204S65B	7C432-65MB
7204S65T	7C433-65C
7204S65TB	7C433-65MB
7204S80B	7C432-65MB
7204S80TB	7C433-65MB
7205L20	7C460-15C
7205L25	7C460-25C
7205L30B	7C460-15MB
7205L30B	7C460-25MB
7205L35	7C460-25C
7205L50	7C460-40C
7205L50B	7C460-40MB
7206-15	7C462-15
7206-20	7C462-20
7206-25	7C462-25
7220L15	7C4201-15
7220L25	7C4201-25
7220L35	7C4201-35
7220SLB15	7C4205-15
7220SLB25	7C4205-25
7220SLB35	7C4205-35
7221L15	7C4211-15
7221L25	7C4211-25
7221L35	7C4211-35
7221SLB15	7C4215-15
7221SLB25	7C4215-25
7221SLB35	7C4215-35
7222L15	7C4221-15
7222L25	7C4221-25
7222L35	7C4221-35
7222SLB15	7C4225-15
7222SLB25	7C4225-25
7222SLB35	7C4225-35
7223L15	7C4231-15
7223L25	7C4231-25
7223L35	7C4231-35

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Product Line Cross Reference

MACRONIX	CYPRESS
27C256-55C	27C256-55C
27C256-70C	27C256-70C
27C256-90C	27C256-90C
27C256-120C	27C256-120C
27C256-150C	27C256-150C
27C256-200C	27C256-200C
27C512-45C	27H512-45C
27C512-55C	27H512-55C
27C512-70C	27H512-70C
27C512-90C	27C512-90C
27C512-120C	27C512-120C
27C512-150C	27C512-150C
27C512-200C	27C512-200C

MICROCHIP	CYPRESS
SUFFIX: J	SUFFIX: W
SUFFIX: P	SUFFIX: P
SUFFIX: L	SUFFIX: J
27C64-12	27C64-120C
27C64-15	27C64-150C
27C64-17	27C64-150C
27C64-20	27C64-200C
27C64-25	27C64-200C
27C128-12	CY27C128-120C+
27C128-15	CY27C128-150C+
27C128-17	CY27C128-150C+
27C128-20	CY27C128-200C+
27C128-25	CY27C128-200C+
27C256-10	CY27C256-90C+
27C256-12	CY27C256-120C+
27C256-15	CY27C256-150C+
27C256-20	CY27C256-200C+
27C512-10	27C512-90C
27C512-12	27C512-120C
27C512-15	27C512-150C
27C512-20	27C512-200C
27C512-90	27C512-90C
27HC256-55	CY27C256-55C
27HC256-70	CY27C256-70C
27HC256-90	CY27C256-90C

MICRON**	CYPRESS
PREFIX: MT	PREFIX: CY
58LC64K18B2	7C1331
5C1001-15C	7C107A-15C
5C1001-20C	7C107A-20C
5C1001-25C	7C107A-25C
5C1008-20C	7C109-20C
5C1008-25C	7C109-25C
5C1008-12C	7C109A-12C
5C1008-15C	7C109A-15C
5C1008-20C	7C109A-20C
5C1601-15	7C167A-15C
5C1601-20C	7C167A-20C
5C1601-25C	7C167A-25C
5C1601-30	7C167A-25C
5C1601-35C	7C167A-35C
5C1604-15	7C168A-15C
5C1604-20C	7C168A-20C
5C1604-25C	7C168A-25C
5C1604-30	7C168A-25C
5C1604-35C	7C168A-35C
5C1605-15	7C170A-15C

MICRON**	CYPRESS
5C1605-20C	7C170A-20C
5C1605-25C	7C170A-25C
5C1605-30	7C170A-25C
5C1605-35C	7C170A-35C
5C1608-15	7C128A-15C
5C1608-20C	7C128A-20C
5C1608-25C	7C128A-25C
5C1608-35C	7C128A-35C
5C2561-12	7C197-12
5C2561-15	7C197-15
5C2561-20	7C197-20
5C2561-25	7C197-25C
5C2561-30	7C197-25C
5C2561-35	7C197-35C
5C2561-45	7C197-45C
5C2564-12	7C194-12
5C2564-15	7C194-15
5C2564-20	7C194-20
5C2564-25	7C194-25C
5C2564-30	7C194-25C
5C2564-35	7C194-35C
5C2564-45	7C194-45C
5C2565-12	7C195-12
5C2565-15	7C195-15
5C2565-20	7C195-20
5C2565-25	7C195-25C
5C2565-30	7C195-25C
5C2565-35	7C195-35C
5C2565-45	7C195-45C
5C2568-12	7C199-12
5C2568-15	7C199-15
5C2568-20	7C199-20
5C2568-25	7C199-25C
5C2568-30	7C199-25C
5C2568-35	7C199-35C
5C2568-45	7C199-45C
5C2889-20C	7C188-20C
5C2889-25C	7C188-25C
5C6404-15	7C164-15C
5C6404-20	7C164-20C
5C6404-25	7C164-25C
5C6404-30	7C164-25C
5C6404-35	7C164-35C
5C6405-15	7C166-15C
5C6405-20C	7C166-20C
5C6405-25C	7C166-25C
5C6405-30	7C166-25C
5C6405-35C	7C166-35C
5C6408-15	7C185-15C
5C6408-20C	7C185-20C
5C6408-25C	7C185-25C
5C6408-30	7C185-25C
5C6408-35C	7C185-35C
5LC2568-15	7C1399-15
5LC2568-20C	7C1399-20C
5LC2568-25C	7C1399-25C
58LC64K18-9	7C1031-8.5
58LC64K18-10	7C1031-10
85C1664-30C	1620HD-30C
85C8128-25	M1420PD-25C
85C8128-35	M1420PD-35C
85C8128-45C	1423PD-45C

MICRON**	CYPRESS
8S1632Z	M1821PZ
8S1632M	M1821PM
8S6432Z	M1831PZ
8S6432M	M1831PM
8S2563Z	M1841PZ
8S2563M	M1841PM
4S12832Z	M1836PZ
4S12832M	M1836PM

MITSUBISHI	CYPRESS
PREFIX: M5L	PREFIX: CY
PREFIX: M5M	PREFIX: CY
SUFFIX: AP	SUFFIX: L
SUFFIX: FP	SUFFIX: F
SUFFIX: K	SUFFIX: D
SUFFIX: P	SUFFIX: P
21C67P-35	7C167A-35C
21C67P-45	7C167A-45C
21C67P-55	7C167A-45C
21C68P-35	7C168A-35C
21C68P-45	7C168A-45C
21C68P-55	7C168A-45C
27C256-85	27C256-70C+
27C256-100	27C256-90C+
27C256-120	27C256-120C+
27C256-150	27C256-150C+
27C256-170	27C256-150C+
5165L-70	7C186-55C+
5165L-100	7C186-55C+
5165L-120	7C186-55C+
5165P-70	7C186-55C+
5165P-100	7C186-55C+
5165P-120	7C186-55C+
5178P-45	7C186-45C+
5178P-55	7C186-55C+
5187P-25	7C187-25C
5187P-35	7C187-35C
5187P-45	7C187-45C
5187P-55	7C187-45C
5188P-25	7C164-25C
5188P-35	7C164-35C
5188P-45	7C164-45C
5188P-55	7C164-45C
5257J-35	7C197-35C
5257J-45	7C197-45C
5257P-35	7C197-35C
5257P-45	7C197-45C
5258J-45	7C194-45C
5258P-35	7C194-35C
5258P-45	7C194-45C
52B79P/J	7C188

MMI/AMD	CYPRESS
SUFFIX: 883B	SUFFIX: B
SUFFIX: F	SUFFIX: F
SUFFIX: J	SUFFIX: D
SUFFIX: L	SUFFIX: L
SUFFIX: N	SUFFIX: P
SUFFIX: SHRP	SUFFIX: B
PAL12L10C	PLDC20G10-35C
PAL12L10M	PLDC20G10-40M
PAL14L8C	PLDC20G10-35C
PAL14L8M	PLD20G10-40M

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Product Line Cross Reference

NATIONAL	CYPRESS
27C010-120C	27C010-120C
27C010-150C	27C010-150C
27C010-200C	27C010-200C
27C64-100C	27C64-90C
27C64-120C	27C64-120C
27C64-150C	27C64-150C
27C64-200C	27C64-200C
27C128-12C	27C128-120C+
27C128-15C	27C128-150C+
27C128-20C	27C128-200C+
27C256-100	27C256-90C+
27C256-120	27C256-120C+
27C256-150	27C256-150C+
27C256-200	27C256-200C+
27C512-120C	27C512-120C
27C512-150C	27C512-150C
27C512-200C	27C512-200C
27P010-70C	27C010-70C
27P010-90C	27C010-90C
27P010-100C	27C010-90C
77LS181	7C282A-45M
77S181	7C282A-45M
77S181A	7C282A-45M
77S281	7C281A-45M
77S281A	7C281A-45M
77S401	7C401-10M
77S401A	7C401-10M
77S402	7C402-10M
77S402A	7C402-10M
77SR181	7C235A-40M
77SR476	7C225A-40M-
77SR476B	7C225A-40M-
85S07A	7C128-45C+
87LS181	7C282A-45C
87S181	7C282A-45C
87S281	7C281A-45C
87S281A	7C281A-45C
87S401	7C401-10C
87S401A	7C401-15C
87S402	7C402-10C
87S402A	7C402-15C
87SR181	7C235-40C
87SR476	7C225A-40C
87SR476B	7C225A-30C
93L422A	7C122-C
C27C53-55	27C256-55C
C27C53-70	27C256-70C
GAL22V10-15C	PALC22V10D-15C
GAL22V10-20I	PALC22V10D-15I
GAL22V10-20M	PALC22V10D-15M
GAL22V10-25C	PALC22V10D-25C
GAL22V10-30I	PALC22V10D-25I
GAL22V10-30M	PALC22V10D-25M
NMF512X9-15	7C421A-15
NMF512X9-25	7C421-25
NMF2048X9-20	7C429-20
NMF4096X9A-25	7C433-25
PAL164A2M	PALC16R4-40M
PAL16L8A2C	PALC16L8-35C
PAL16L8A2M	PALC16L8-40M
PAL16L8AC	PALC16L8-25C
PAL16L8AM	PALC16L8-30M

NATIONAL	CYPRESS
PAL16L8B2C	PALC16L8-25C
PAL16L8B2M	PALC16L8-30M
PAL16L8B4C	PALC16L8L-35C
PAL16L8B4M	PALC16L8-40M
PAL16L8BM	PALC16L8-20M
PAL16L8C	PALC16L8-35C
PAL16L8M	PALC16L8-40M
PAL16R4A2C	PALC16R4-35C
PAL16R4AC	PALC16R4-25C
PAL16R4AM	PALC16R4-30M
PAL16R4B2C	PALC16R4-25C
PAL16R4B2M	PALC16R4-30M
PAL16R4B4C	PALC16R4L-35C
PAL16R4B4M	PALC16R4-40M
PAL16R4BM	PALC16R4-20M
PAL16R4C	PALC16R4-35C
PAL16R4M	PALC16R4-40M
PAL16R6A2C	PALC16R6-35C
PAL16R6A2M	PALC16R6-40M
PAL16R6AC	PALC16R6-25C
PAL16R6AM	PALC16R6-30M
PAL16R6B2C	PALC16R6-25C
PAL16R6B2M	PALC16R6-30M
PAL16R6B4C	PALC16R6L-35C
PAL16R6B4M	PALC16R6-40M
PAL16R6BM	PALC16R6-20M
PAL16R6C	PALC16R6-35C
PAL16R6M	PALC16R6-40M
PAL16R8A2C	PALC16R8-35C
PAL16R8A2M	PALC16R8-40M
PAL16R8AC	PALC16R8-25C
PAL16R8AM	PALC16R8-30M
PAL16R8B2C	PALC16R8-25C
PAL16R8B2M	PALC16R8-30M
PAL16R8B4C	PALC16R8L-35C
PAL16R8B4M	PALC16R8-40M
PAL16R8BM	PALC16R8-20M
PAL16R8C	PALC16R8-35C
PAL16R8M	PALC16R8-40M
PAL20L2C	PLDC20G10-35C
PAL20L8AC	PLDC20G10-25C
PAL20L8AM	PLDC20G10-30M
PAL20L8BC	PLDC20G10-25C
PAL20L8BM	PLDC20G10-30M
PAL20L8C	PLDC20G10-35C
PAL20L8M	PLDC20G10-40M
PAL20L10B2C	PLDC20G10-25C
PAL20L10B2M	PLDC20G10-30M
PAL20L10C	PLDC20G10-35C
PAL20L10M	PLDC20G10-40M
PAL20R4AC	PLDC20G10-25C
PAL20R4AM	PLDC20G10-30M
PAL20R4BC	PLDC20G10-25C
PAL20R4BM	PLDC20G10-30M
PAL20R4C	PLDC20G10-35C
PAL20R4M	PLDC20G10-40M
PAL20R6AC	PLDC20G10-25C
PAL20R6AM	PLDC20G10-30M
PAL20R6BC	PLDC20G10-25C
PAL20R6BM	PLDC20G10-30M
PAL20R6C	PLDC20G10-35C
PAL20R6M	PLDC20G10-40M

NATIONAL	CYPRESS
PAL20R8AC	PLDC20G10-25C
PAL20R8AM	PLDC20G10-30M
PAL20R8BC	PLDC20G10-25C
PAL20R8BM	PLDC20G10-30M
PAL20R8C	PLDC20G10-35C
PAL20R8M	PLDC20G10-40M

NEC	CYPRESS
PREFIX: uPD	PREFIX: CY
SUFFIX: C	SUFFIX: P
SUFFIX: D	SUFFIX: D
SUFFIX: K	SUFFIX: L
SUFFIX: L	SUFFIX: F
2147A	7C147-C
2149	2149-C
2149	7C149-C
2167-2	7C167A-C
27HC65-25	7C263/4-25C
27HC65-35	7C263/4-35C
27HC65-45	7C263/4-45C
4311-45	7C167A-45C
4311-55	7C167A-45C
43254C-35	7C194-35
43254C-45	7C194-45
4361	7C187-C
4362	7C164-C
4363	7C166-C
43259-20	7C188-20
43259-25	7C188-25
431001-20	7C107A-20C
431001-25	7C107A-25C
431004-20	7C106A-20C
431004-25	7C106A-25C
431008-15	7C109A-15
431008-20	7C109A-20
431008-20	7C109-20

OKI	CYPRESS
PREFIX: MSM	PREFIX: CY
27128A-12C	27C128-120C+
27128A-15C	27C128-150C+
27128A-20C	27C128-200C+
27256-100	27C256-90C+
27256-120	27C256-120C+
27256-150	27C256-150C+
27256-200	27C256-200C+
27256H-55	27C256-55C
27256H-70	27C256-70C

PARADIGM	CYPRESS
PREFIX: PDM	PREFIX: CY
41251L	7C191-C
41251LB	7C191-MB*
41251S	7C191-C
41251SB	7C191-MB
41252L	7C192-C
41252LB	7C192-MB*
41252S	7C192-C
41252SB	7C192-MB
41256L	7C199/8-C*
41256LB	7C199/8-MB*
41256S	7C199/8-C
41256SB	7C199/8-MB

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Product Line Cross Reference

SAMSUNG	CYPRESS
PREFIX: KM	PREFIX: CY
18V87-8	7C1031-8.5
61257A-25	7C197-25C
61257A-35	7C197-35C
61257A-45	7C197-45C
64257A-25	7C194-25C
64257A-35	7C194-35C
64257A-45	7C194-45C
64258B-15	7C194-15C
64258B-20	7C194-20C
64259B-15	7C196-15C
64259B-20	7C196-20C
641001-20	7C106A-20C
681001-20	7C109A-20C
681002-15	7C1009-15C
681002-20	7C1009-20C
68257-12	7C199-12C
68257-15	7C199-15C
718B514-8	7C178-8.5
75C01A-15	7C421-15
75C01A-20	7C421-20C
75C01A-25	7C421-25C
75C01A-35	7C421-30C
75C01A-50	7C421-40C
75C01A-80	7C421-65C
75C01AP-20	7C420-20C
75C01AP-25	7C420-25C
75C01AP-35	7C420-35C
75C01AP-50	7C420-50C
75C01AP-80	7C420-80C
75C02A-15	7C425-15
75C02A-20	7C425-20C
75C02A-25	7C425-25C
75C02A-35	7C425-30C
75C02A-50	7C425-40C
75C02A-80	7C425-65C
75C02AP-20	7C424-20C
75C02AP-25	7C424-25C
75C02AP-35	7C424-30C
75C02AP-50	7C424-40C
75C02AP-80	7C424-65C
75C03A-15	7C429-15C
75C03A-20	7C429-20C
75C03A-25	7C429-25C
75C03A-35	7C429-30C
75C03A-50	7C429-40C
75C03A-80	7C429-65C
75C03AP-20	7C428-20C
75C03AP-25	7C428-25C
75C03AP-35	7C428-30C
75C03AP-50	7C428-40C
75C03AP-80	7C428-65C
75C102A-20	7C425-20C
75C102A-25	7C425-25C
75C102A-35	7C425-25C
75C102A-80	7C425-65C
SGS-THOMSON	CYPRESS
PREFIX: M	PREFIX: CY
SUFFIX: F1	SUFFIX: W
SUFFIX: B1	SUFFIX: P
SUFFIX: C1	SUFFIX: J
SUFFIX: N1	SUFFIX: Z

SGS-THOMSON	CYPRESS
27256-150	27C256-150C
27256-170	27C256-150C
27256-200	27C256-200C
27C64A-12	27C64-120C
27C64A-15	27C64-150C
27C64A-20	27C64-200C
27C64A-25	27C64-200C
27C64A-30	27C64-200C
27C128A-12	27C128-120C+
27C128A-15	27C128-150C+
27C128A-20	27C128-200C+
27C256B-80	27C256-70C+
27C256B-90	27C256-90C+
27C256B-100	27C256-90C+
27C256B-120	27C256-120C+
27C512-10	27C512-90C
27C512-12	27C512-120C
27C512-15	27C512-150C
27C512-20	27C512-200C
27C512-25	27C512-200C
27C512-80	27H512-70C
27C512-90	27C512-90C
27C1001-60X	27H010-55C
27C1001-70	27C010-70C
27C1001-90	27C010-90C
27C1001-120	27C010-120C
27C1001-150	27C010-150C
27C1001-200	27C010-200C
SHARP	CYPRESS
PREFIX: LH	PREFIX: CY
52251-35	7C197-35C
52251-45	7C197-45C
52252-35	7C194-35C
52252-45	7C194-45C
52254D-25	7C199-25C
52254D-35	7C199-35C
52254D-45	7C199-45C
52259	7C188
5481-15	7C408A-15C
5481-25	7C408A-25C
5481-35	7C408A-35C
5491-15	7C409A-15C
5491-25	7C409A-25C
5491-35	7C409A-35C
5496-20	7C420-20C
5496-35	7C420-30C
5496-50	7C420-40C
5496D-15	7C421A-15
5496D-20	7C421-20C
5496D-35	7C421-30C
5496D-50	7C421-40C
5497-20	7C424-20C
5497-35	7C424-30C
5497-50	7C424-40C
5497D-15	7C425A-15
5497D-20	7C425-20C
5497D-35	7C425-30C
5497D-50	7C425-40C

SONY	CYPRESS
PREFIX: CXX	PREFIX: CY
51256P-35	7C197-35
51256P-45	7C197-45
55464-20	7C194-20C
55464-25	7C194-25C
58258A-15	7C199-15C
58258A-20	7C199-20C
58258A-25	7C199-25C
59288-20C	7C188-20C
59288-25C	7C188-25C
TI	CYPRESS
PREFIX: JBP	PREFIX: CY
PREFIX: PAL	SUFFIX: P
PREFIX: SM	PREFIX: CY
PREFIX: SMJ	PREFIX: CY
PREFIX: SN	PREFIX: CY
PREFIX: TBP	PREFIX: CY
PREFIX: TIB	PREFIX: CY
PREFIX: TMS	PREFIX: CY
SUFFIX: FM	SUFFIX: J
SUFFIX: J	SUFFIX: W
SUFFIX: N	SUFFIX: P
SUFFIX: DD	SUFFIX: Z
SUFFIX: N	SUFFIX: P
22V10AC	PALC22V10-25C
22V10AM	PALC22V10-30M
27C010-120	27C010-120C
27C010-150	27C010-150C
27C010-200	27C010-200C
27C128-12	27C128-120
27C512-100	27C512-90C
27C512-120	27C512-120C
27C512-150	27C512-150C
27C512-200	27C512-200C
27C/PC128-15	27C128-150
27C/PC128-200	27C128-200
27C256-10	27C256-90C+
27C256-12	27C256-120C+
27C256-15	27C256-150C+
27C256-17	27C256-150C+
27C256-20	27C256-200C+
27PC010-120	27PC010-120C
27PC010-150	27PC010-150C
27PC010-200	27PC010-200C
27PC256-10	27C256-90C+
27PC256-12	27C256-120C+
27PC256-15	27C256-150C+
27PC256-17	27C256-150C+
27PC256-20	27C256-200C+
27PC512-100	27PC512-90C
27PC512-120	27PC512-120C
27PC512-150	27PC512-150C
27PC512-200	27PC512-200C
PAL16L8-5C	PAL16L8-5C
PAL16L8-7C	PAL16L8-7C
PAL16L8-7M	PAL16L8-7M
PAL16L8-10C	PAL16L8-7C
PAL16L8-10M	PAL16L8-10M
PAL16L8-12M	PAL16L8-10M
PAL16L8-15C	PAL16L8-7C
PAL16L8-15M	PAL16L8-10M
PAL16L8-20M	PALC16L8-20M

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

- + = meets all performance specs but may not meet I_{CC} or I_{SB}
- * = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}
- = functionally equivalent
- † = SOIC only
- ‡ = 32-pin LCC crosses to the 7C198M
- ** = See Austin Semiconductor for military products



Product Line Cross Reference

WSI	CYPRESS
57C64F-55	7C266-55C
57C51C-45	7C251/4-45C
57C51C-45M	7C251/4-45M
57C51C-55	7C251/4-55C
57C51C-55M	7C251/4-55M
57C51C-70	7C251/4-55M
57C51C-70M	7C251/4-55M
57C71C-35	7C271A-35C
57C71C-45	7C271A-45C
57C71C-55	7C271A-55C
57C71C-55M	7C271A-55M
57C71C-70	7C271A-55M
57C71C-70M	7C271A-55M
57C128F-55C	27C128-55C+
57C128F-70C	27C128-70C+
57C128FB-45	27C128-45C
57C128FB-55	27C128-55C
57C128FB-70	27C128-70C
57C191B-35	7C292A-35C
57C191B-35M	7C292A-35M
57C191B-45	7C292A-35C
57C191B-45M	7C292A-35M
57C191B-50M	7C292A-50M
57C191B-55	7C292A-50C
57C191B-55M	7C292A-50M
57C191C-25	7C292A-25C
57C191C-35	7C292A-35C
57C191C-45	7C292A-35C
57C191C-45M	7C292A-35M
57C191C-55	7C292A-50C
57C191C-55M	7C292A-50M
57C256F-35	27H256-35C
57C256F-45	27C256-45C+
57C256F-55	27C256-55C+
57C256F-55M	27C256-55M
57C256F-70	27C256-70C+
57C256F-70M	27C256-70M
57C256F-90	27C256-90C+
57C291B-35	7C291A-35C
57C291B-35M	7C291A-35M
57C291B-45	7C291A-35C
57C291B-45M	7C291A-35M
57C291B-50M	7C291A-50M
57C291B-55	7C291A-50C
57C291B-55M	7C291A-50M
57C291C-25	7C291A-25C
57C291C-35	7C291A-35C
57C291C-45	7C291A-35C
57C291C-45M	7C291A-35M
57C291C-55	7C291A-50C
57C291C-55M	7C291A-50M

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

- + = meets all performance specs but may not meet I_{CC} or I_{SB}
- * = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}
- = functionally equivalent
- † = SOIC only
- ‡ = 32-pin LCC crosses to the 7C198M
- ** = See Austin Semiconductor for military products



Product Line Cross Reference

FCT Commercial Cross Reference (continued)

CYPRESS		TI
CY74FCT52C		74ABT2952A
CY74FCT2240A		SN74ABT2240
CY74FCT2244A		SN74ABT2244
CY74FCT2245A		SN74ABT2245
CY74FCT240A		SN74ABT240
CY74FCT244A		SN74ABT244
CY74FCT245A		SN74ABT245
CY74FCT273A		SN74ABT273
CY74FCT373A		SN74ABT373
CY74FCT374A		SN74ABT374
CY74FCT377A		SN74ABT377
CY74FCT540A		SN74ABT540
CY74FCT541A		SN74ABT541
CY74FCT543A		SN74ABT543
CY74FCT573A		SN74ABT573
CY74FCT574A		SN74ABT574
CY74FCT646A		SN74ABT646
CY74FCT646C		SN74ABT646A
CY74FCT652A		SN74ABT652
CY74FCT652C		SN74ABT652A
CY74FCT821C		SN74ABT821
CY74FCT827C		SN74ABT827
CY74FCT841C		SN74ABT841
CYBUS3384		SN74CBT3384
Package		Code
Plastic DIP	P	N
SOIC	SO	DW



Product Line Cross Reference

Commercial Cross Reference

CYPRESS		IDT		PERICOM	
CY74FCT16240	Std, A, C	IDT174FCT16240	Std, A, C, E	PI74FCT16240	Std, A, C, D
CY74FCT16244	Std, A, C	IDT174FCT16244	Std, A, C, E	PI74FCT16244	Std, A, C, D
CY74FCT16245	Std, A, C	IDT174FCT16245	Std, A, C, E	PI74FCT16245	Std, A, C, D
CY74FCT16373	Std, A, C	IDT174FCT16373	Std, A, C, E	PI74FCT16373	Std, A, C, D
CY74FCT16374	Std, A, C	IDT174FCT16374	Std, A, C, E	PI74FCT16374	Std, A, C, D
CY74FCT16444	Std, A, C				
CY74FCT16445	Std, A, C				
CY74FCT16500	A, C	IDT174FCT16500	A, C, E	PI74FCT16500	A, C, D
CY74FCT16501	A, C	IDT174FCT16501	A, C, E	PI74FCT16501	A, C, D
CY74FCT16543	Std, A, C	IDT174FCT16543	Std, A, C, E	PI74FCT16543	Std, A, C, D
CY74FCT16646	Std, A, C	IDT174FCT16646	Std, A, C, E	PI74FCT16646	Std, A, C, D
CY74FCT16652	Std, A, C	IDT174FCT16652	Std, A, C, E	PI74FCT16652	Std, A, C, D
CY74FCT16823	A, B, C	IDT174FCT16823	A, B, C, E	PI74FCT16823	A, B, C
CY74FCT16827	A, B, C	IDT174FCT16827	A, B, C, E	PI74FCT16827	A, B, C
CY74FCT16841	A, B, C	IDT174FCT16841	A, B, C, E	PI74FCT16841	A, B, C
CY74FCT16952	A, B, C	IDT174FCT16952	A, B, C, E	PI74FCT16952	A, B, C, D
CY74FCT162240	Std, A, C	IDT174FCT162240	Std, A, C, E	PI74FCT162240	Std, A, C, D
CY74FCT162244	Std, A, C	IDT174FCT162244	Std, A, C, E	PI74FCT162244	Std, A, C, D
CY74FCT162245	Std, A, C	IDT174FCT162245	Std, A, C, E	PI74FCT162245	Std, A, C, D
CY74FCT162373	Std, A, C	IDT174FCT162373	Std, A, C, E	PI74FCT162373	Std, A, C, D
CY74FCT162374	Std, A, C	IDT174FCT162374	Std, A, C, E	PI74FCT162374	Std, A, C, D
CY74FCT162444	Std, A, C				
CY74FCT162445	Std, A, C				
CY74FCT162500	A, C	IDT174FCT162500	A, C, E	PI74FCT162500	A, C, D
CY74FCT162501	A, C	IDT174FCT162501	A, C, E	PI74FCT162501	A, C, D
CY74FCT162543	Std, A, C	IDT174FCT162543	Std, A, C, E	PI74FCT162543	Std, A, C, D
CY74FCT162646	Std, A, C	IDT174FCT162646	Std, A, C, E	PI74FCT162646	Std, A, C, D
CY74FCT162652	Std, A, C	IDT174FCT162652	Std, A, C, E	PI74FCT162652	Std, A, C, D
CY74FCT162823	A, B, C	IDT174FCT162823	A, B, C, E	PI74FCT16H823	A, B, C
CY74FCT162827	A, B, C	IDT174FCT162827	A, B, C, E	PI74FCT162827	A, B, C
CY74FCT162841	A, B, C	IDT174FCT162841	A, B, C, E	PI74FCT162841	A, B, C
CY74FCT162952	A, B, C	IDT174FCT162952	A, B, C, E	PI74FCT162952	A, B, C, D
CY74FCT162H952	A, B, C	IDT174FCT162H952	A, B, C, E		
CY74FCT162H501	A, C	IDT174FCT162H501	A, C, E		
CY74FCT162H244	Std, A, C	IDT174FCT162H244	Std, A, C, E		
CY74FCT162H245	Std, A, C	IDT174FCT162H245	Std, A, C, E		
CY74FCT162H373	Std, A, C	IDT174FCT162H373	Std, A, C, E		
Package	Code	Package	Code	Package	Code
SSOP	PV	SSOP	PV	SSOP	PV
TSSOP	PA	TSSOP	PA	TSSOP	PA

CYPRESS		TEXAS INSTRUMENTS		PHILLIPS	
CY74FCT16240CT		SN74ABT16240		74ABT16244	
CY74FCT16244CT		SN74ABT16244A		74ABT16245	
CY74FCT16245CT		SN74ABT16245		74ABT16373	
CY74FCT16373CT		SN74ABT16373A		74ABT16374	
CY74FCT16374CT		SN74ABT16374A			
CY74FCT16500CT		SN74ABT16500B			
CY74FCT16543CT		SN74ABT16543B		74ABT16543	
CY74FCT162240CT		SN74ABT162240			
CY74FCT162244CT		SN74ABT162244			
CY74FCT162245CT		SN74ABT162245			
CY74FCT162373					
CY74FCT162374					
CY74FCT162500CT		SN74ABT162500			
Package	Code	Package	Code	Package	Code
SSOP	PV	SSOP	DL	SSOP	PV
TSSOP	PA	TSSOP	DDG	TSSOP	PA

Static RAMs (Random Access Memory)
Page Number

Device	Description	Page Number
CY6264	8K x 8 Static RAM	2-1
CY7C101A	256K x 4 Static RAM with Separate I/O	2-7
CY7C102A	256K x 4 Static RAM with Separate I/O	2-7
CY7C106A	256K x 4 Static RAM	2-15
CY7C107A	1M x 1 Static RAM	2-23
CY7C109	128K x 8 Static RAM	2-30
CY7C109A	128K x 8 Static RAM	2-36
CY7C123	256 x 4 Static RAM	2-44
CY7C128A	2K x 8 Static RAM	2-50
CY7C148	1K x 4 Static RAM	2-57
CY7C149	1K x 4 Static RAM	2-57
CY7C150	1K x 4 Static RAM	2-64
CY7C161	16K x 4 Static RAM with Separate I/O	2-72
CY7C162	16K x 4 Static RAM with Separate I/O	2-72
CY7C161A	16K x 4 Static RAM with Separate I/O	2-80
CY7C162A	16K x 4 Static RAM with Separate I/O	2-80
CY7C164	16K x 4 Static RAM	2-88
CY7C166	16K x 4 Static RAM	2-88
CY7C164A	16K x 4 Static RAM	2-95
CY7C166A	16K x 4 Static RAM	2-95
CY7C167A	16K x 1 Static RAM	2-103
CY7C168A	4K x 4 Static RAM	2-110
CY7C169A	4K x 4 Static RAM	2-110
CY7C170A	4K x 4 Static RAM	2-117
CY7C171A	4K x 4 Static RAM with Separate I/O	2-122
CY7C172A	4K x 4 Static RAM with Separate I/O	2-122
CY7C178	32K x 18 Synchronous Cache RAM	2-130
CY7C179	32K x 18 Synchronous Cache RAM	2-130
CY7C182	8K x 9 Static RAM	2-142
CY7C185	8K x 8 Static RAM	2-147
CY7C185A	8K x 8 Static RAM	2-155
CY7C187	64K x 1 Static RAM	2-163
CY7C187A	64K x 1 Static RAM	2-170
CY7C188	32K x 9 Static RAM	2-178
CY7C191	64K x 4 Static RAM with Separate I/O	2-185
CY7C192	64K x 4 Static RAM with Separate I/O	2-185
CY7C193	32K x 8 Synchronous SRAM	2-193
CY7C194	64K x 4 Static RAM	2-199
CY7C195	64K x 4 Static RAM	2-199
CY7C196	64K x 4 Static RAM	2-199
CY7C197	256K x 1 Static RAM	2-208
CY7C199	32K x 8 Static RAM	2-216
CY7C1001	256K x 4 Static RAM with Separate I/O	2-227
CY7C1002	256K x 4 Static RAM with Separate I/O	2-227
CY7C1006	256K x 4 Static RAM	2-234
CY7C1007	1M x 1 Static RAM	2-241
CY7C1009	128K x 8 Static RAM	2-247
CY7C1014	256K x 4 Static RAM	2-254
CY7C1016	256K x 4 Static RAM	2-255
CY7C1019	128K x 8 Static RAM	2-256
CY7C1021	64K x 16 Static RAM	2-257

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ^[1]	-0.5V to +7.0V
DC Input Voltage ^[1]	-0.5V to +7.0V

Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	6264-55		6264-70		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[1]		-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[2]	V _{CC} = Max., V _{OUT} = GND		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		100		100	mA
I _{SB1}	Automatic \overline{CE}_1 Power-Down Current	Max. V _{CC} , $\overline{CE}_1 \geq V_{IH}$, Min. Duty Cycle = 100%		20		20	mA
I _{SB2}	Automatic \overline{CE}_1 Power-Down Current	Max. V _{CC} , $\overline{CE}_1 \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		15		15	mA

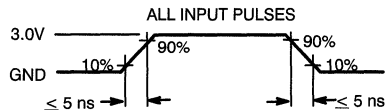
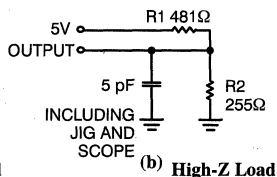
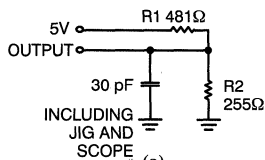
Shaded area contains advanced information.

Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	7	pF
C _{OUT}	Output Capacitance		7	pF

Notes:

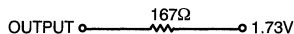
- Minimum voltage is equal to -3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

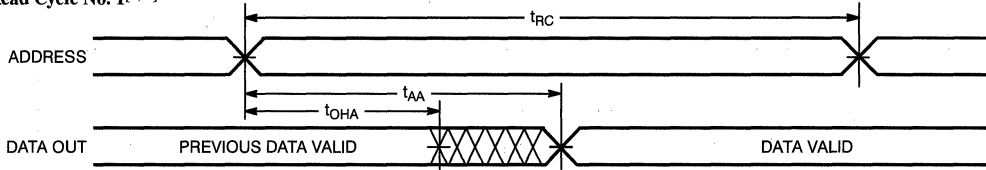
AC Test Loads and Waveforms


CY6264-3

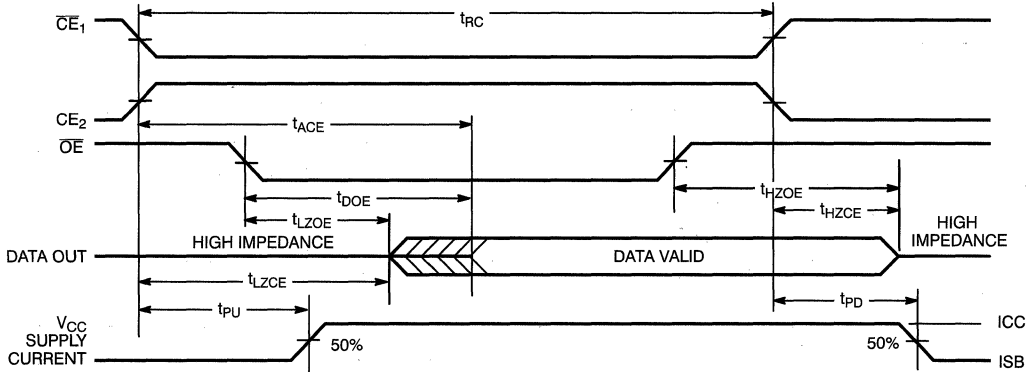
CY6264-4

Equivalent to: THÉVENIN EQUIVALENT

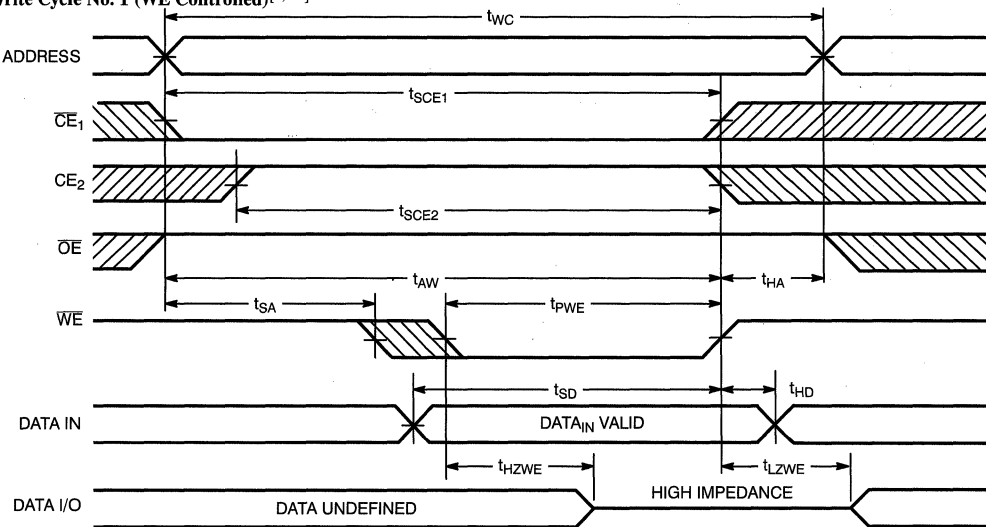


Switching Waveforms
Read Cycle No. 1^[8, 9]


CY6264-5

Read Cycle No. 2^[10, 11]


CY6264-6

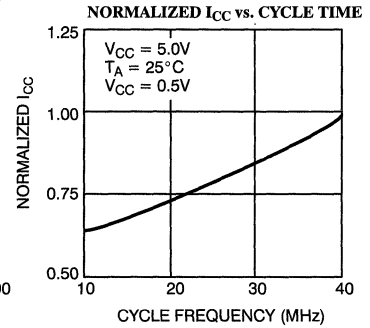
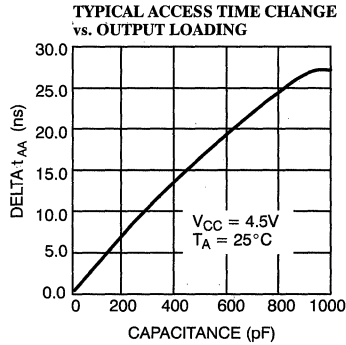
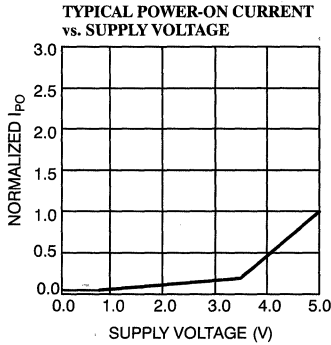
Write Cycle No. 1 (WE Controlled)^[9, 11]


CY6264-7

Notes:

8. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$. $CE_2 = V_{IH}$.
 9. Address valid prior to or coincident with \overline{CE} transition LOW.

10. \overline{WE} is HIGH for read cycle.
 11. Data I/O is High Z if $\overline{OE} = V_{IH}$, $\overline{CE}_1 = V_{IH}$, or $\overline{WE} = V_{IL}$.

Typical DC and AC Characteristics (continued)

Truth Table

\overline{CE}_1	CE_2	\overline{WE}	\overline{OE}	Input/Output	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Address Designators

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24
A3	X2	25

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY6264-55SC	S23	28-Lead 330-Mil SOIC	Commercial
70	CY6264-70SC	S23	28-Lead 330-Mil SOIC	Commercial

Shaded area contains advanced information.

Document #: 38-00425



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with
 Power Applied -55°C to +125°C
 Supply Voltage on V_{CC} Relative to GND^[1] . . . -0.5V to +7.0V
 DC Voltage Applied to Outputs
 in High Z State^[1] -0.5V to V_{CC} +0.5V
 DC Input Voltage^[1] -0.5V to V_{CC} +0.5V
 Current into Outputs (LOW) 20 mA
 Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military ^[2]	-55°C to +125°C	5V ± 10%

Notes:

1. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range^[3]

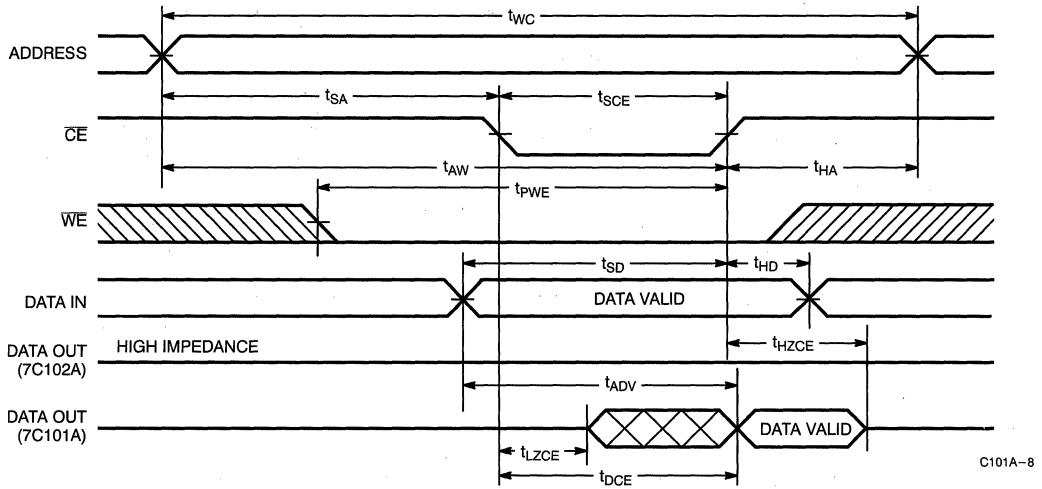
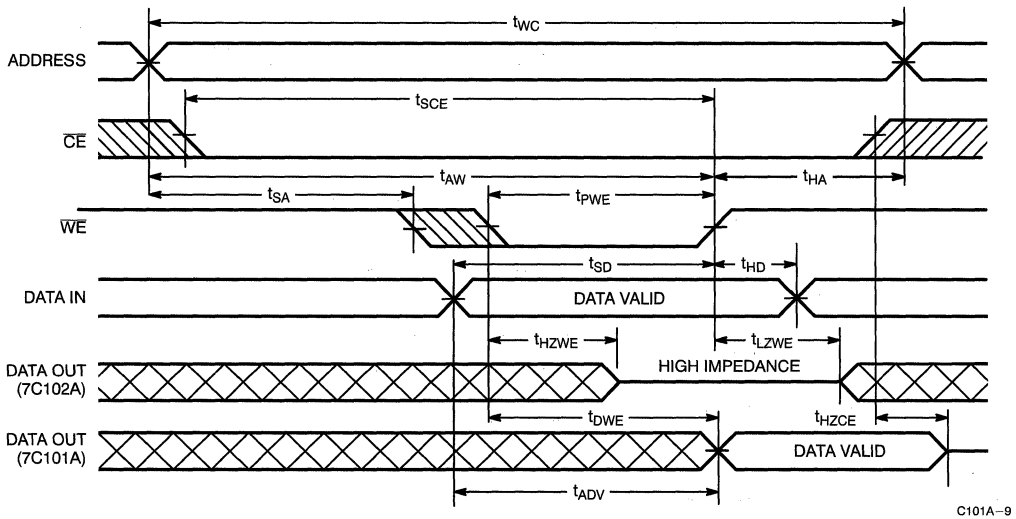
Parameter	Description	Test Conditions	7C101A-12 7C102A-12		7C101A-15 7C102A-15		7C101A-20 7C102A-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _{PX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	-1	+1	µA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	µA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com ¹	165		155		140	mA
			Mil			165		150	
I _{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Com ¹	50		40		30	mA
			Mil			40		30	
I _{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0	Com ¹	2		2		2	mA
			Mil			2		2	

Switching Characteristics Over the Operating Range^[3, 6]

Parameter	Description	7C101A-12 7C102A-12		7C101A-15 7C102A-15		7C101A-20 7C102A-20		7C101A-25 7C102A-25		7C101A-35 7C102A-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	12		15		20		25		35		ns
t _{AA}	Address to Data Valid		12		15		20		25		35	ns
t _{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t _{ACE}	\overline{CE} LOW to Data Valid		12		15		20		25		35	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[7]	3		3		3		3		3		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[7, 8]		6		7		8		10		10	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		12		15		20		25		35	ns
WRITE CYCLE^[9]												
t _{WC}	Write Cycle Time	12		15		20		25		35		ns
t _{SCE}	\overline{CE} LOW to Write End	10		12		15		20		25		ns
t _{AW}	Address Set-Up to Write End	10		12		15		20		25		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	10		12		15		20		25		ns
t _{SD}	Data Set-Up to Write End	7		8		10		15		20		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[7]	3		3		3		3		3		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[7, 8]		6		7		8		10		10	ns
t _{DWE}	\overline{WE} LOW to Data Valid (7C101A)		12		15		20		25		35	ns
t _{DCE}	\overline{CE} LOW to Data Valid (7C101A)		12		15		20		25		35	ns
t _{ADV}	Data Valid to Output Valid (7C101A)		12		15		20		25		35	ns

Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{CE} Controlled)^[9, 14]

Write Cycle No. 2 (\overline{WE} Controlled)^[9]

Note:

14. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state (7C102A only).



MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{Ix}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11
t _{DWE} ^[16]	7, 8, 9, 10, 11
t _{ADV} ^[16]	7, 8, 9, 10, 11

Note:

16. 7C101A only.

Document #: 38-00231-A

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Ambient Temperature with
 Power Applied -55°C to $+125^{\circ}\text{C}$
 Supply Voltage on V_{CC} Relative to GND^[1] . -0.5V to $+7.0\text{V}$
 DC Voltage Applied to Outputs
 in High Z State^[1] -0.5V to $V_{CC} + 0.5\text{V}$
 DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5\text{V}$
 Current into Outputs (LOW) 20 mA

Static Discharge Voltage $>2001\text{V}$
 (per MIL-STD-883, Method 3015)

Latch-Up Current $>200\text{ mA}$

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 10\%$
Military	-55°C to $+125^{\circ}\text{C}$	$5\text{V} \pm 10\%$

Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	7C106A-12		7C106A-15		7C106A-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0\text{ mA}$	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0\text{ mA}$		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-1	+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	-5	+5	-5	+5	-5	+5	μA
I_{OS}	Output Short Circuit Current ^[4]	$V_{CC} = \text{Max.}, V_{OUT} = GND$		-300		-300		-300	mA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0\text{ mA}, f = f_{MAX} = 1/\text{trc}$	Com'l	165		155		140	mA
			Mil			165		150	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	Com'l	50		40		30	mA
			Mil			40		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3\text{V}$, $V_{IN} \geq V_{CC} - 0.3\text{V}$ or $V_{IN} \leq 0.3\text{V}, f = 0$	Com'l	2		2		2	mA
			Mil			2		2	

Notes:

- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

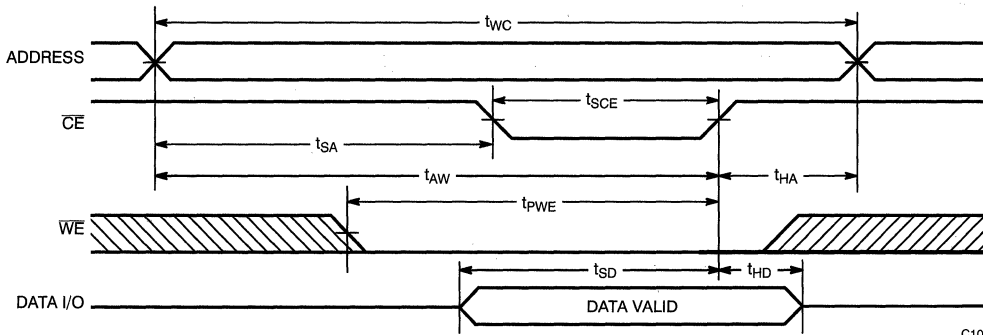
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Switching Characteristics Over the Operating Range^[3, 6]

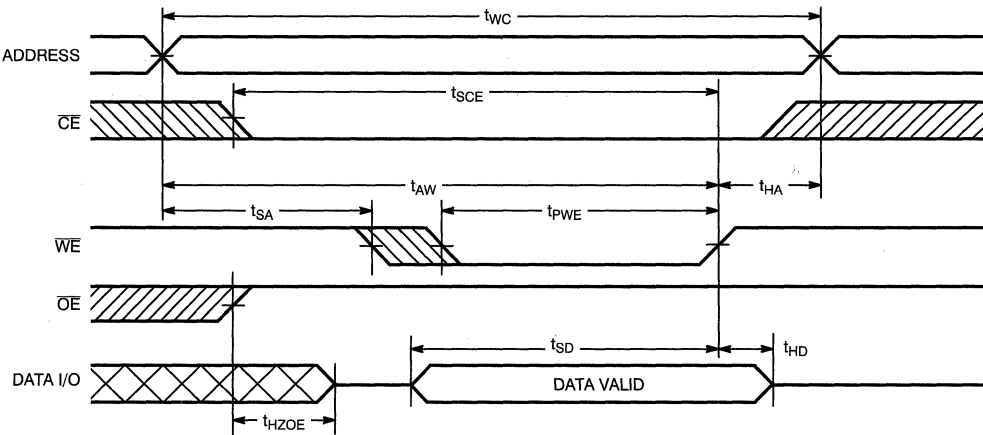
Parameter	Description	7C106A-12		7C106A-15		7C106A-20		7C106A-25		7C106A-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	12		15		20		25		35		ns
t _{AA}	Address to Data Valid		12		15		20		25		35	ns
t _{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t _{ACE}	\overline{CE} LOW to Data Valid		12		15		20		25		35	ns
t _{DOE}	\overline{OE} LOW to Data Valid		6		7		8		10		10	ns
t _{LZOE}	\overline{OE} LOW to Low Z	0		0		0		0		0		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[7, 8]		6		7		8		10		10	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[8]	3		3		3		3		3		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[7, 8]		6		7		8		10		10	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		12		15		20		25		35	ns
WRITE CYCLE^[9,10]												
t _{WC}	Write Cycle Time	12		15		20		25		35		ns
t _{SCE}	\overline{CE} LOW to Write End	10		12		15		20		25		ns
t _{AW}	Address Set-Up to Write End	10		12		15		20		25		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	10		12		15		20		25		ns
t _{SD}	Data Set-Up to Write End	7		8		10		15		20		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[8]	2		3		3		3		3		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[7, 8]		6		7		8		10		10	ns

Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{CE} Controlled)^[15, 16]


C106A-8

Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[15,16]


C106A-9

Notes:

15. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state. 16. Data I/O is high impedance if $\overline{OE} = V_{IH}$.



MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

Document #: 38-00230-A



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with
 Power Applied -55°C to +125°C
 Supply Voltage on V_{CC} Relative to GND^[1] . -0.5V to +7.0V
 DC Voltage Applied to Outputs
 in High Z State^[1] -0.5V to V_{CC} +0.5V
 DC Input Voltage^[1] -0.5V to V_{CC} +0.5V
 Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

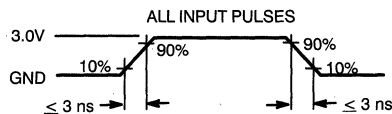
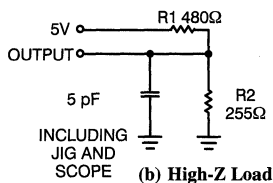
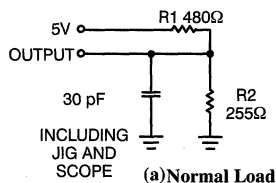
Range	Ambient Temperature ^[2]	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	7C107A-12		7C107A-15		7C107A-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} +0.3	2.2	V _{CC} +0.3	2.2	V _{CC} +0.3	V
V _{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	-1	+1	µA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	µA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0mA, f = f _{MAX} = 1/t _{RC}	Com'l	150		135		125	mA
			Mil			145		135	
I _{SB1}	Automatic \overline{CE} Power-Down Current - TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Com'l	50		40		30	mA
			Mil			40		30	
I _{SB2}	Automatic \overline{CE} Power-Down Current - CMOS Inputs	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f=0	Com'l	2		2		2	mA
			Mil			2		2	

Notes:

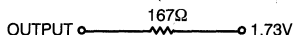
- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.

AC Test Loads and Waveforms


107A-3

107A-4

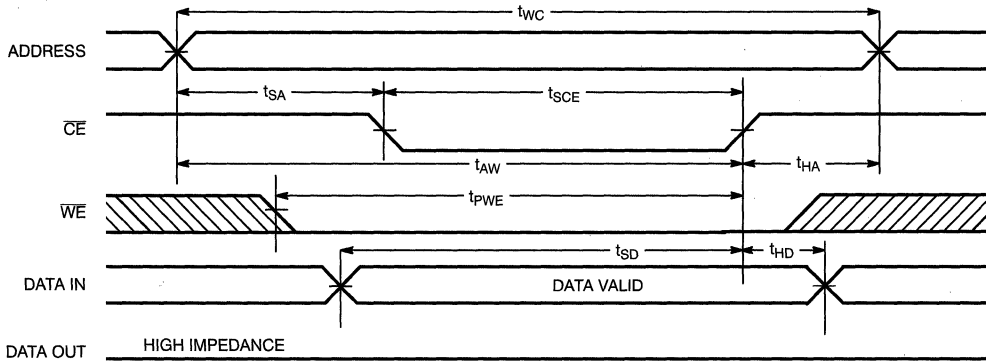
Equivalent to: THÉVENIN EQUIVALENT


Switching Characteristics^[3, 6] Over the Operating Range

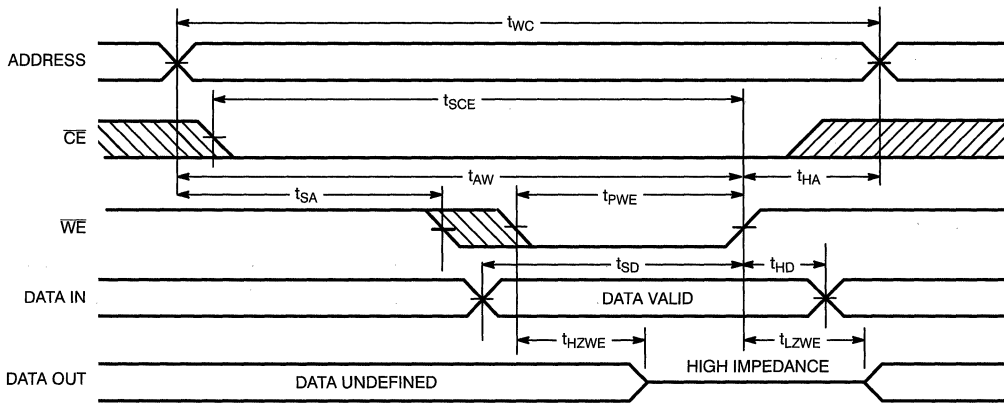
Parameter	Description	7C107A-12		7C107A-15		7C107A-20		7C107A-25		7C107A-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	\overline{CE} LOW to Data Valid		12		15		20		25		35	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[7]	3		3		3		3		3		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[7, 8]		6		7		8		10		10	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		12		15		20		25		35	ns
WRITE CYCLE^[9]												
t_{WC}	Write Cycle Time	12		15		20		25		35		ns
t_{SCE}	\overline{CE} LOW to Write End	10		12		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	10		12		15		20		25		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[7]	3		3		3		3		3		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[7, 8]		6		7		8		10		10	ns

Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZCE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{CE} Controlled)^[14]


107A-8

Write Cycle No. 2 (\overline{WE} Controlled)^[14]


107A-9

Truth Table

\overline{CE}	\overline{WE}	D _{OUT}	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	High Z	Write	Active (I_{CC})

Note:

 14. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.



128K x 8 Static RAM

Features

- High speed
— $t_{AA} = 20$ ns
- CMOS for optimum speed/power
- Low active power
— 770 mW
- Low standby power
— 165 mW
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} options

Functional Description

The CY7C109 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}_1), an active HIGH chip enable (CE_2), an active LOW output enable (\overline{OE}), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

Writing to the device is accomplished by taking chip enable one (\overline{CE}_1) and write enable (\overline{WE}) inputs LOW and chip enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written

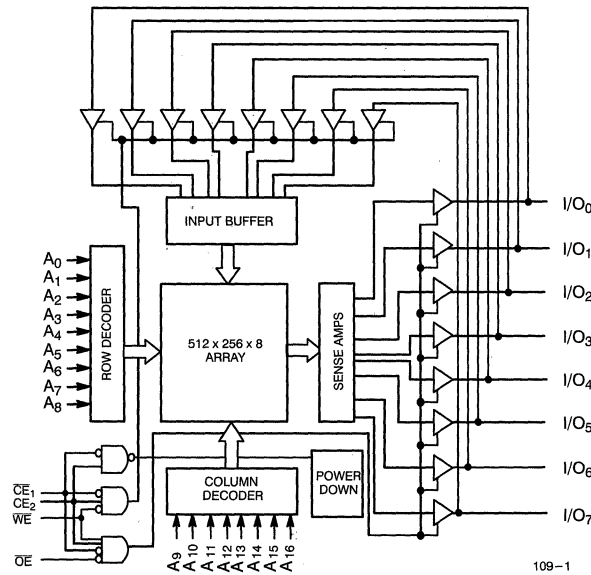
into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable one (\overline{CE}_1) and output enable (\overline{OE}) LOW while forcing write enable (\overline{WE}) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH or CE_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW).

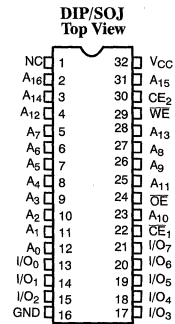
The CY7C109 is available in standard 400-mil-wide DIPs and SOJs.

Logic Block Diagram



109-1

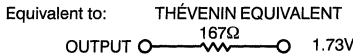
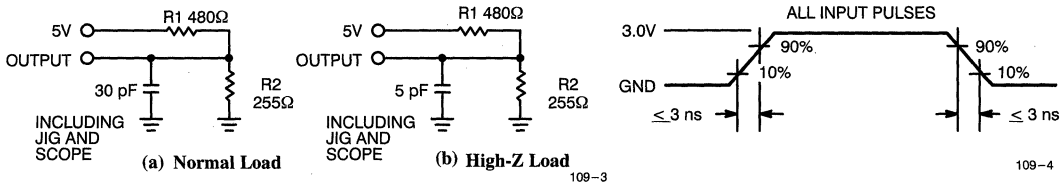
Pin Configurations



109-2

Selection Guide

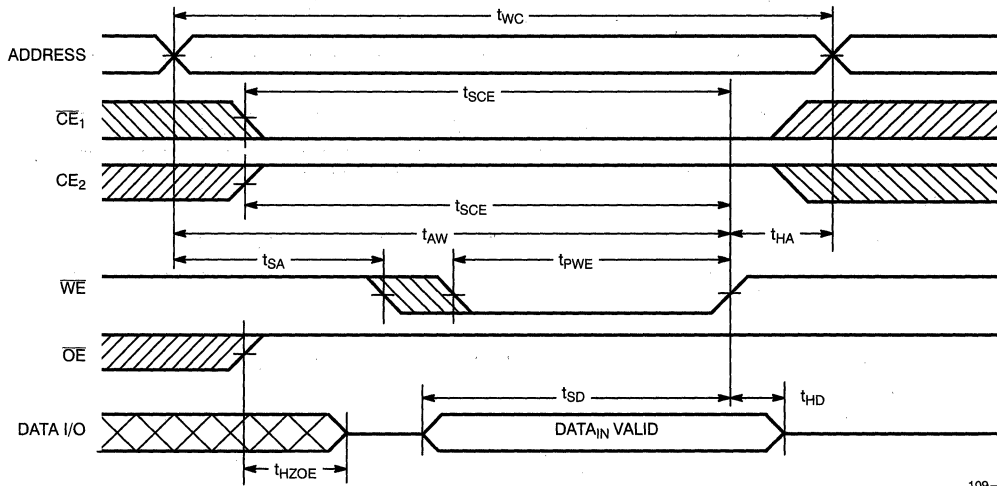
		7C109-20	7C109-25	7C109-35
Maximum Access Time (ns)		20	25	35
Maximum Operating Current (mA)	Commercial	140	135	125
Maximum Standby Current (mA)	Commercial	30	30	25

AC Test Loads and Waveforms

Switching Characteristics^[3, 6] Over the Operating Range

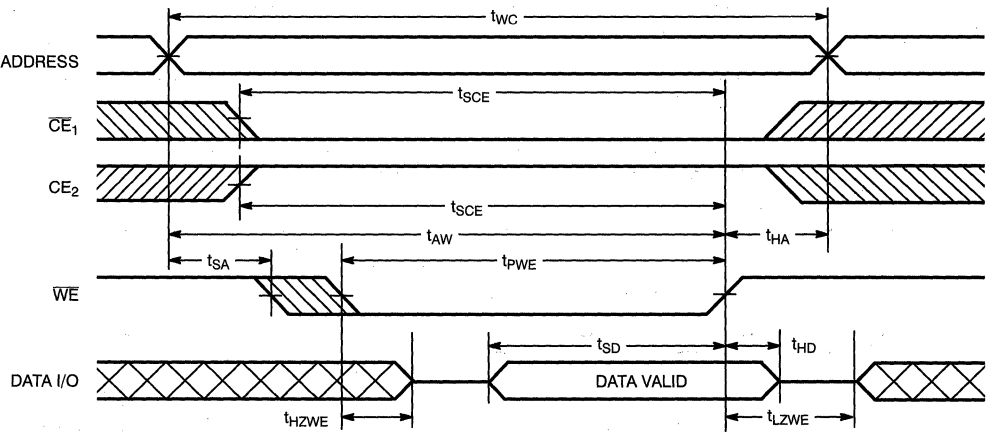
Parameter	Description	7C109-20		7C109-25		7C109-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20		25		35		ns
t_{AA}	Address to Data Valid		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		5		5		ns
t_{ACE}	\overline{CE}_1 LOW to Data Valid, CE_2 HIGH to Data Valid		20		25		35	ns
t_{DOE}	\overline{OE} LOW to Data Valid		8		10		15	ns
t_{LZOE}	\overline{OE} LOW to Low Z	0		0		0		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[7, 8]		8		10		15	ns
t_{LZCE}	\overline{CE}_1 LOW to Low Z, CE_2 HIGH to Low Z ^[8]	3		5		5		ns
t_{HZCE}	\overline{CE}_1 HIGH to High Z, CE_2 LOW to High Z ^[7, 8]		8		10		15	ns
t_{PU}	\overline{CE}_1 LOW to Power-Up, CE_2 HIGH to Power-Up	0		0		0		ns
t_{PD}	\overline{CE}_1 HIGH to Power-Down, CE_2 LOW to Power-Down		20		25		35	ns
WRITE CYCLE^[9, 10]								
t_{WC}	Write Cycle Time	20		25		35		ns
t_{SCE}	\overline{CE}_1 LOW to Write End, CE_2 HIGH to Write End	15		20		25		ns
t_{AW}	Address Set-Up to Write End	15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	15		20		25		ns
t_{SD}	Data Set-Up to Write End	10		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[8]	3		5		5		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[7, 8]		8		10		15	ns

Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW. \overline{CE}_1 and \overline{WE} must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms (continued)
Write Cycle No. 2 (WE Controlled, OE HIGH During Write)^[14, 15]


109-8

Write Cycle No. 3 (WE Controlled, OE LOW)^[10, 15]


109-9



128K x 8 Static RAM

Features

- High speed
— $t_{AA} = 12$ ns
- CMOS for optimum speed/power
- Low active power
— 1020 mW
- Low standby power
— 250 mW
- 2.0V data retention (optional)
— 100 μ W
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} options

Functional Description

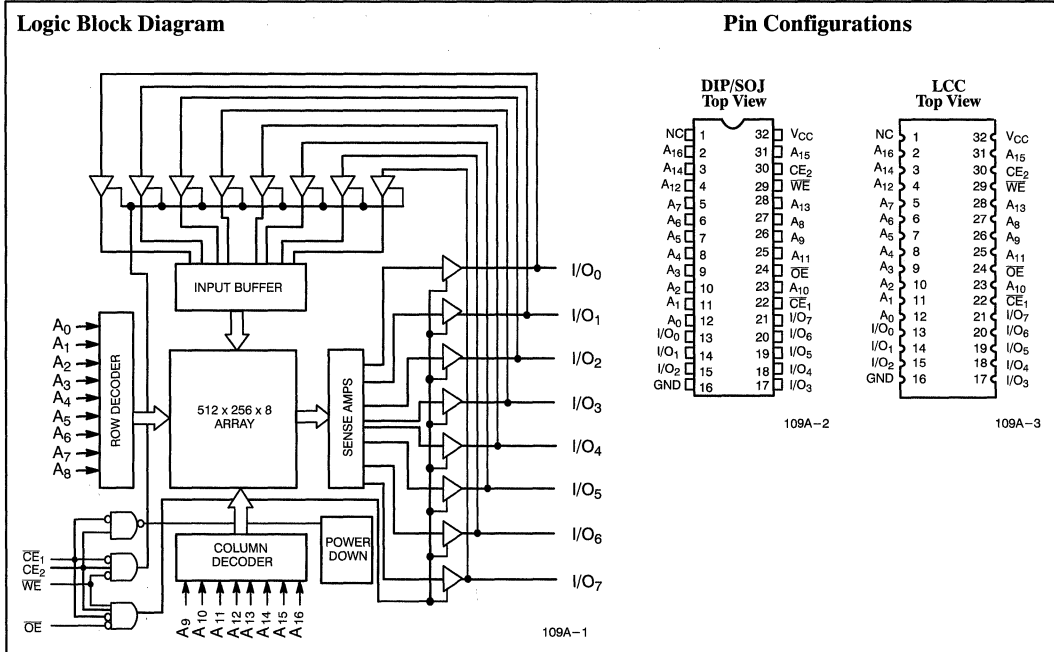
The CY7C109A is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}_1), an active HIGH chip enable (CE_2), an active LOW output enable (\overline{OE}), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

Writing to the device is accomplished by taking chip enable one (\overline{CE}_1) and write enable (\overline{WE}) inputs LOW and chip enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable one (\overline{CE}_1) and output enable (\overline{OE}) LOW while forcing write enable (\overline{WE}) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH or CE_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW).

The CY7C109A is available in standard 400-mil-wide DIPs and SOJs and a leadless chip carrier.



Selection Guide

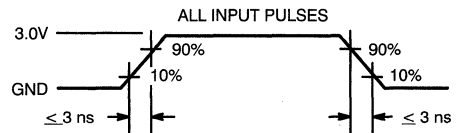
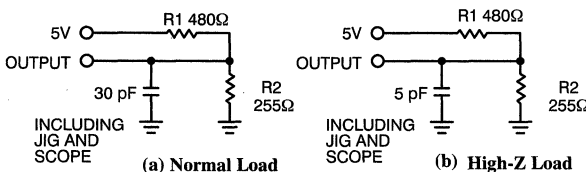
		7C109A-12	7C109A-15	7C109A-20	7C109A-25	7C109A-35
Maximum Access Time (ns)		12	15	20	25	35
Maximum Operating Current (mA)	Commercial	185	170	155	145	140
	Military		180	170	160	150
Maximum Standby Current (mA)	Commercial	45	40	30	30	25
	Military		40	30	30	25

Electrical Characteristics Over the Operating Range^[3] (continued)

Parameter	Description	Test Conditions	7C109A-25		7C109A-35		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/trc	Com'1	145	140		mA
			Mil	160	150		
I _{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V _{CC} , CE ₁ ≥ V _{IH} or CE ₂ ≤ V _{IL} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Com'1	30	25		mA
			Mil	30	25		
I _{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V _{CC} , CE ₁ ≥ V _{CC} - 0.3V, or CE ₂ ≤ 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0	Com'1	2	2		mA
			Mil	2	2		

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN} : Addresses	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	7	pF
C _{IN} : Controls			10	pF
C _{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms


109A-4

109A-5

Equivalent to: THÉVENIN EQUIVALENT

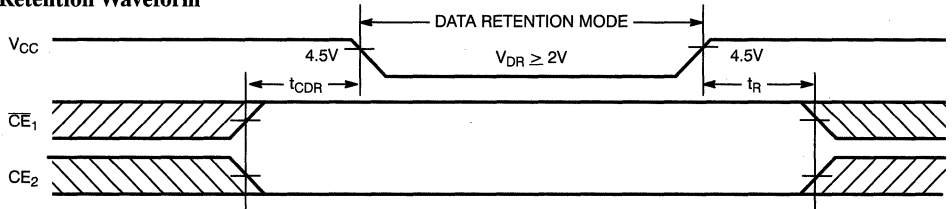
OUTPUT — 167Ω — 1.73V

Notes:

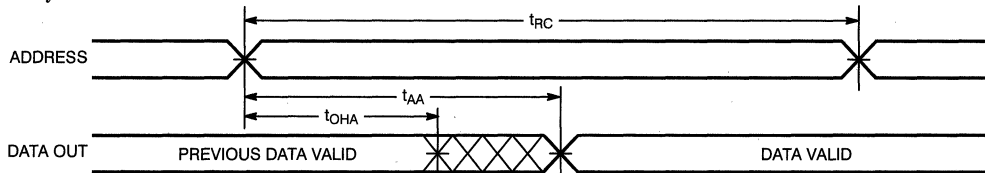
- See the last page of this specification for Group A subgroup testing information.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

Data Retention Characteristics Over the Operating Range (L Version Only)

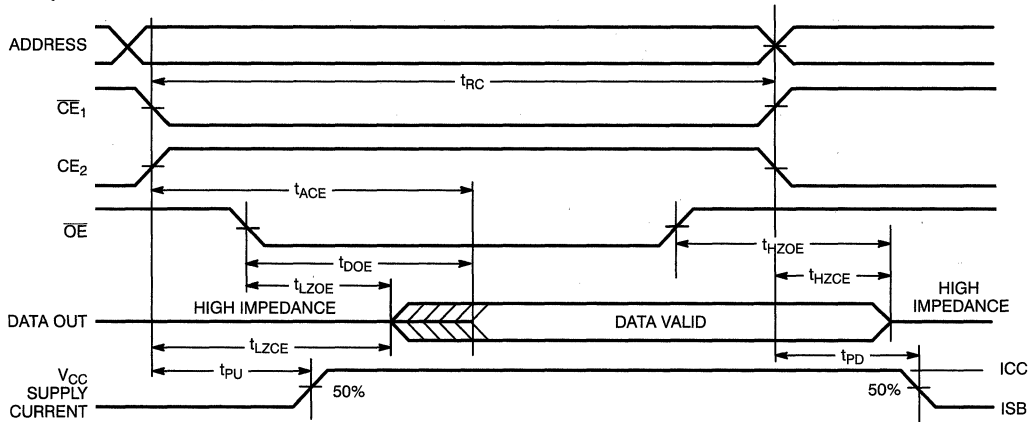
Parameter	Description	Conditions ^[11]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Retention Data		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $CE_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$		50		70	μA
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		0		ns
$t_R^{[5]}$	Operation Recovery Time		t_{RC}		t_{RC}		ns

Data Retention Waveform


109A-6

Switching Waveforms
Read Cycle No. 1^[12, 13]


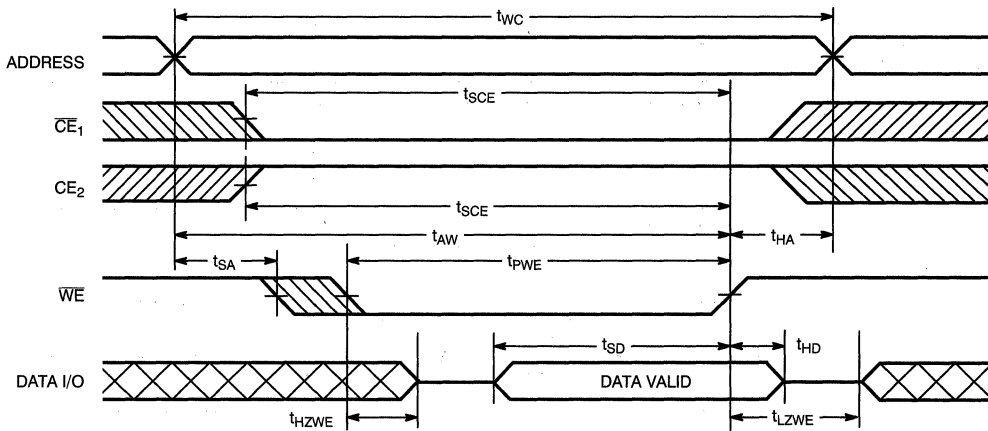
109A-7

Read Cycle No. 2 (\overline{OE} Controlled)^[13, 14]


109A-8

Notes:

11. No input may exceed $V_{CC} + 0.5V$.
12. Device is continuously selected. \overline{OE} , $CE_1 = V_{IL}$, $CE_2 = V_{IH}$.
13. \overline{WE} is HIGH for read cycle.
14. Address valid prior to or coincident with \overline{CE}_1 transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)
Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[10, 16]


109A-11

Truth Table

CE ₁	CE ₂	OE	WE	Input/Output	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I _{SB})
X	L	X	X	High Z	Power-Down	Standby (I _{SB})
L	H	L	H	Data Out	Read	Active (I _{CC})
L	H	X	L	Data In	Write	Active (I _{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I _{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C109A-12PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A-12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C109A-15PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A-15VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C109A-15DMB	D44	32-Lead (400-Mil) CerDIP	Military
	CY7C109A-15LMB	L75	32-Pin Leadless Chip Carrier	
20	CY7C109A-20PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A-20VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C109A-20DMB	D44	32-Lead (400-Mil) CerDIP	Military
	CY7C109A-20LMB	L75	32-Pin Leadless Chip Carrier	

Contact factory for "L" version availability.



256 x 4 Static RAM

Features

- 256 x 4 static RAM for control store in high-speed computers
- CMOS for optimum speed/power
- High speed
 - 7 ns (commercial)
 - 10 ns (military)
- Low power
 - 660 mW (commercial)
 - 825 mW (military)
- Separate inputs and outputs
- 5-volt power supply ±10% tolerance both commercial and military
- TTL-compatible inputs and outputs
- 24 pins
- 300-mil package

Functional Description

The CY7C123 is a high-performance CMOS static RAM organized as 256 words by 4 bits. Easy memory expansion is provided by an active LOW chip select one (\overline{CS}_1) input, an active HIGH chip select two (CS_2) input, and three-state outputs.

Writing to the device is accomplished when the chip select one (\overline{CS}_1) and write enable (\overline{WE}) inputs are both LOW and the chip select two input is HIGH. Data on the four data inputs (D_0 through D_3) is written into the memory location specified on the address pins (A_0 through A_7). The outputs are preconditioned so that the write data is present at the outputs when the write cycle is complete. This preconditioning

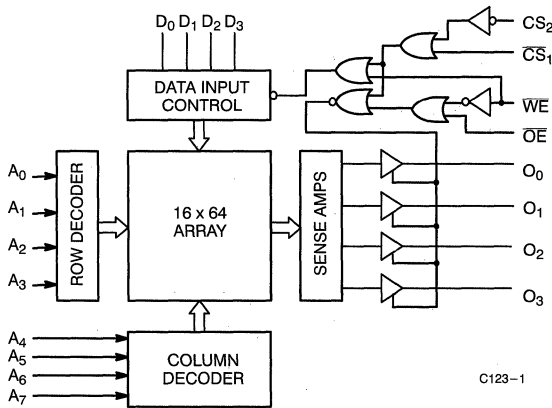
operation ensures minimum write recovery times by eliminating the "write recovery glitch."

Reading the device is accomplished by taking the chip select one (\overline{CS}_1) and output enable (\overline{OE}) inputs LOW, while the write enable (\overline{WE}) and chip select two (CS_2) inputs remain HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four output pins (O_0 through O_3).

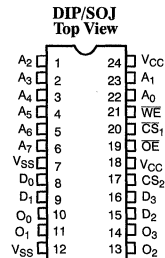
The output pins remain in high-impedance state when chip select one (\overline{CS}_1) or output enable (\overline{OE}) is HIGH, or write enable (\overline{WE}) or chip select two (CS_2) is LOW.

A die coat is used to insure alpha immunity.

Logic Block Diagram



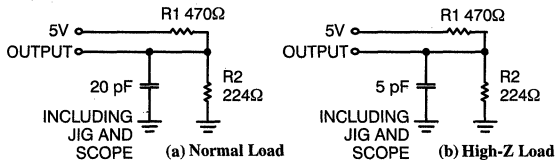
Pin Configuration



C123-2

Selection Guide

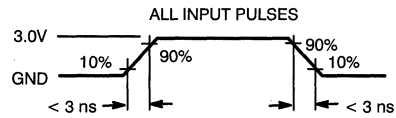
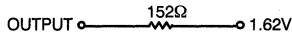
		7C123-7	7C123-9	7C123-10	7C123-12	7C123-15
Maximum Access Time (ns)	Commercial	7	9		12	
	Military			10	12	15
Maximum Operating Current (mA)	Commercial	120	120		120	
	Military			150	150	150

AC Test Loads and Waveforms


C123-3

C123-4

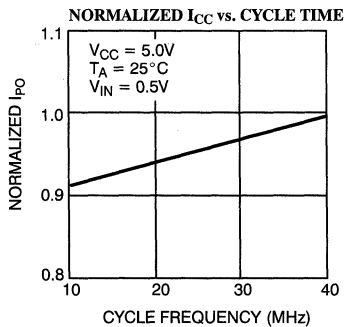
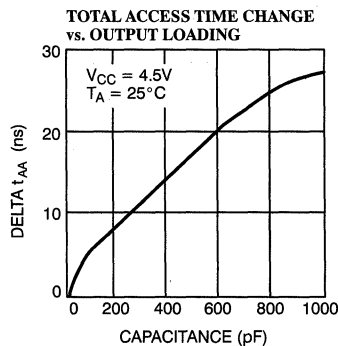
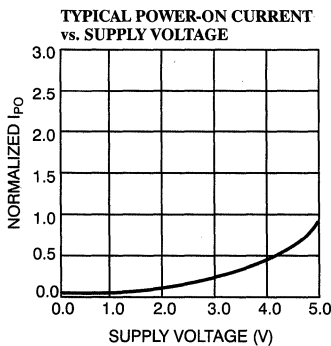
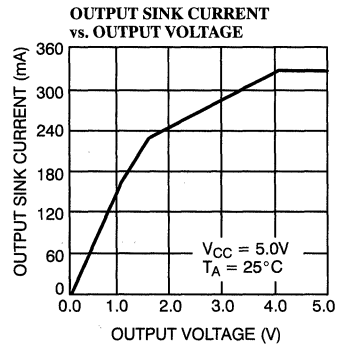
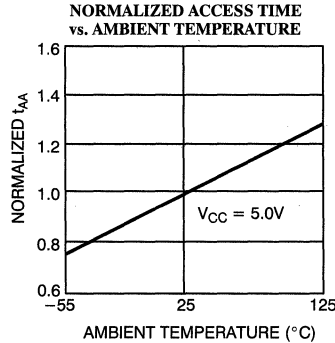
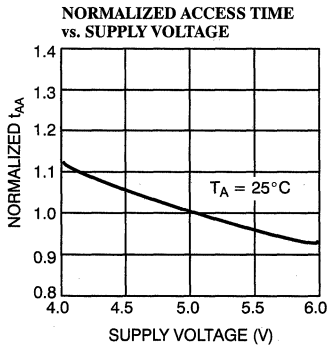
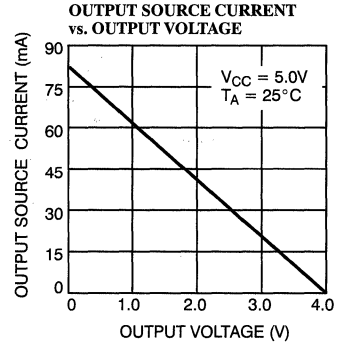
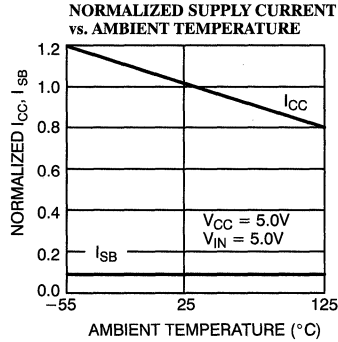
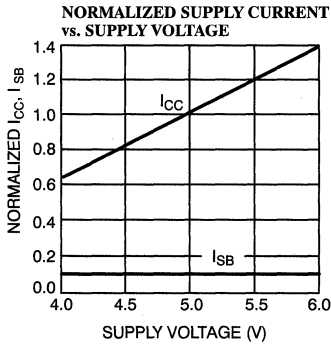
Equivalent to: THÉVENIN EQUIVALENT


Switching Characteristics Over the Operating Range^[3]

Parameter	Description	7C123-7		7C123-9		7C123-10		7C123-12		7C123-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	7		9		10		12		15		ns
t_{AA}	Address to Data Valid		7		9		10		12		15	ns
t_{ACS}	Chip Select to Data Valid		7		8		8		8		10	ns
t_{DOE}	\overline{OE} LOW to Data Valid		7		8		8		8		10	ns
t_{HZCS}	Chip Select to High Z ^[6, 7]		5		6		6		6.5		8	ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[6]		5		6		6		6.5		8	ns
t_{LZCS}	Chip Select to Low Z ^[7]	2		2		2		2		2		ns
t_{LZOE}	\overline{OE} LOW to Low Z	2		2		2		2		2		ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	7		9		10		12		15		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[6]		5.5		6		6		7		8	ns
t_{LZWE}	\overline{WE} HIGH to Low Z	2		2		2		2		2		ns
t_{PWE}	\overline{WE} Pulse Width	5		6.5		7		8		11		ns
t_{SD}	Data Set-Up to Write End	5		6		7		8		11		ns
t_{HD}	Data Hold from Write End	1		1		1		1		1		ns
t_{SA}	Address Set-Up to Write Start	0.5		1		1		2		2		ns
t_{HA}	Address Hold from Write End	1.5		1.5		2		2		2		ns
t_{SCS}	\overline{CS} LOW to Write End	5		6.5		7		8		11		ns
t_{AW}	Address Set-Up to Write End	5.5		7.5		8		10		13		ns

Notes:

- Transition is measured at steady-state HIGH level - 500 mV or steady-state LOW level +500 mV on the output from 1.5V level on the input with load shown in part (b) of AC Test Loads.
- At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.

Typical DC and AC Characteristics


2K x 8 Static RAM

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
— 15 ns
- Low active power
— 440 mW (commercial)
— 550 mW (military)
- Low standby power
— 110 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge
- V_{IH} of 2.2V

Functional Description

The CY7C128A is a high-performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}), and active LOW output enable (\overline{OE}) and three-state drivers. The CY7C128A has an automatic power-down feature, reducing the power consumption by 83% when deselected.

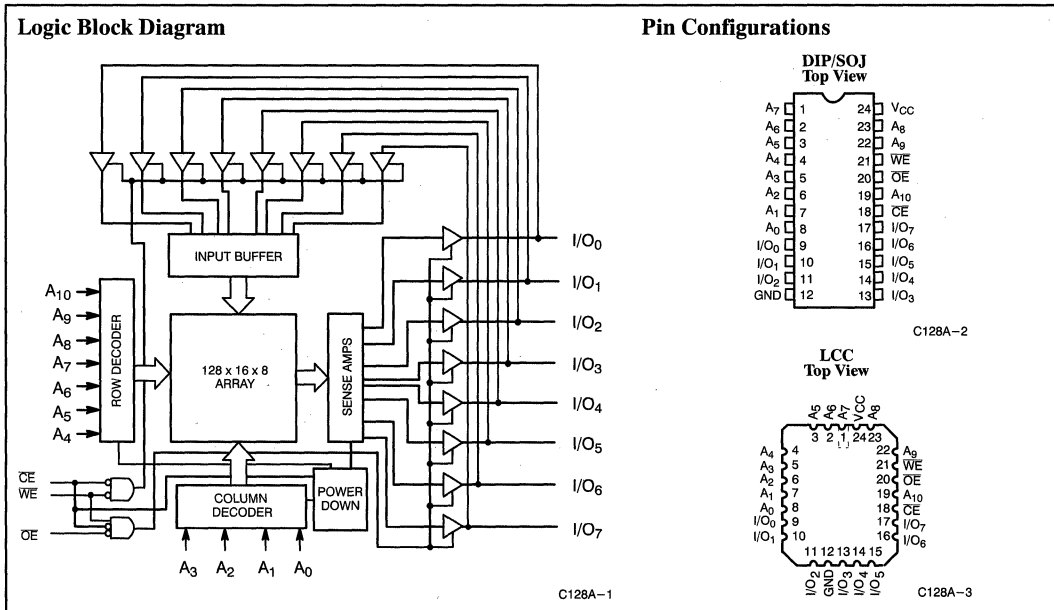
Writing to the device is accomplished when the chip enable (\overline{CE}) and write enable (\overline{WE}) inputs are both LOW.

Data on the eight I/O pins (I/O₀ through I/O₇) is written into the memory location specified on the address pins (A₀ through A₁₀).

Reading the device is accomplished by taking chip enable (\overline{CE}) and output enable (\overline{OE}) LOW while write enable (\overline{WE}) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight I/O pins.

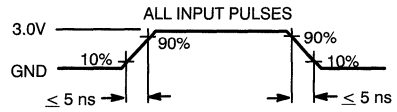
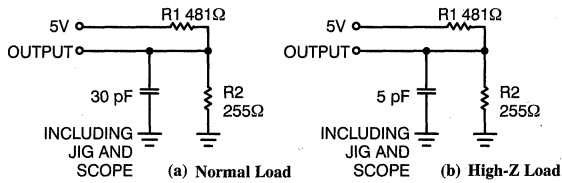
The I/O pins remain in high-impedance state when chip enable (\overline{CE}) or output enable (\overline{OE}) is HIGH or write enable (\overline{WE}) is LOW.

The CY7C128A utilizes a die coat to ensure alpha immunity.



Selection Guide

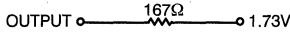
		7C128A-15	7C128A-20	7C128A-25	7C128A-35	7C128A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	120	100	100	100	
	Military		125	125	100	100
Maximum Standby Current (mA)	Commercial	40/40	40/20	20	20	
	Military		40/20	40	20	20

AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT

C128A-4

C128A-5

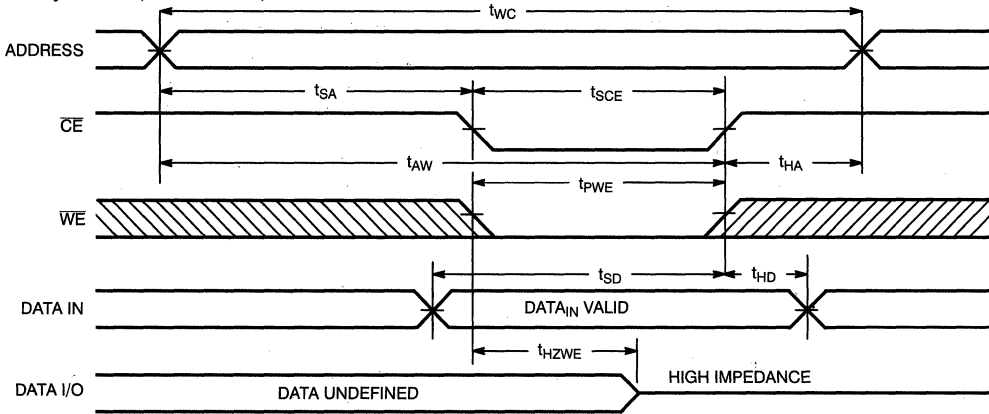

Switching Characteristics Over the Operating Range^[2, 6]

Parameter	Description	7C128A-15		7C128A-20		7C128A-25		7C128A-35		7C128A-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		5		ns
t_{ACE}	\overline{CE} LOW to Data Valid		15		20		25		35		45	ns
t_{DOE}	\overline{OE} LOW to Data Valid		10		10		12		15		20	ns
t_{LZOE}	\overline{OE} LOW to Low Z	3		3		3		3		3		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[7]		8		8		10		12		15	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[8]	5		5		5		5		5		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[7, 8]		8		8		10		15		15	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		15		20		20		20		25	ns
WRITE CYCLE^[9]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCE}	\overline{CE} LOW to Write End	12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	12		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	10		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[7]		7		7		7		10		15	ns
t_{LZWE}	\overline{WE} HIGH to Low Z	5		5		5		5		5		ns

Note:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

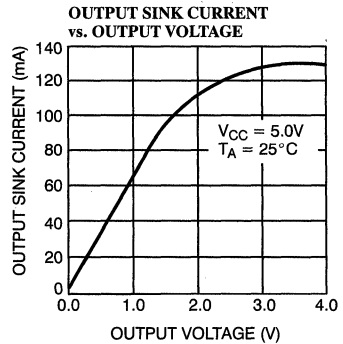
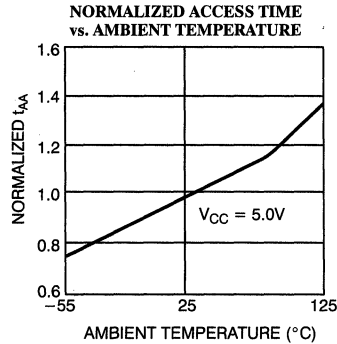
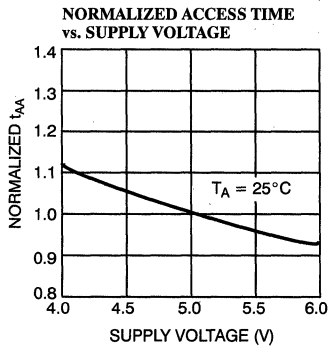
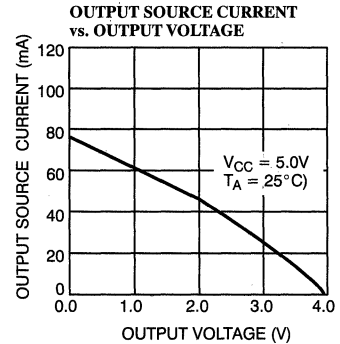
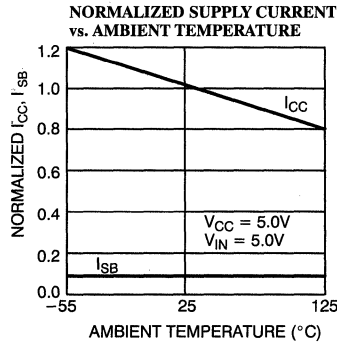
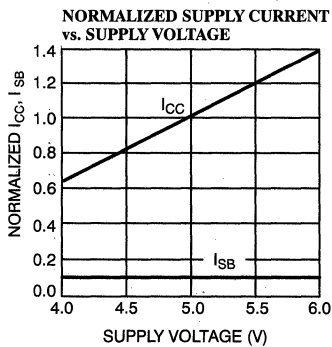
Switching Waveforms (continued)

 Write Cycle No. 2 (\overline{CE} Controlled)^[9, 13, 14]


C128A-9

Note:

 14. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics


MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

Document #: 38-00094-B

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 18 to Pin 9)	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-3.0V to +7.0V

Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military ^[1]	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[2]

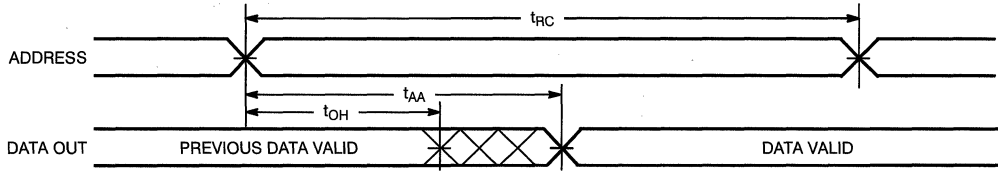
Parameter	Description	Test Conditions	7C148-25 7C149-25		7C148-35, 45 7C149-35, 45		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.0	6.0	2.0	6.0	V
V _{IL}	Input LOW Voltage		-3.0	0.8	-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	10	-10	10	µA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} Output Disabled	-50	50	-50	50	µA
I _{CC}	V _{CC} Operating Supply Current	Max. V _{CC} , $\overline{CS} \leq V_{IL}$, Output Open	Com'l	90		80	mA
			Mil			110	
I _{SB}	Automatic \overline{CS} Power-Down Current	Max. V _{CC} , $\overline{CS} \geq V_{IH}$	7C148 Only	Com'l	15	10	mA
				Mil		10	
I _{PO}	Peak Power-On Current ^[3]	Max. V _{CC} , $\overline{CS} \geq V_{IH}$	7C148 Only	Com'l	15	10	mA
				Mil		10	
I _{OS}	Output Short Circuit Current ^[4]	GND ≤ V _O ≤ V _{CC}		Com'l	±275	±275	mA
				Mil		±350	

Capacitance^[5]

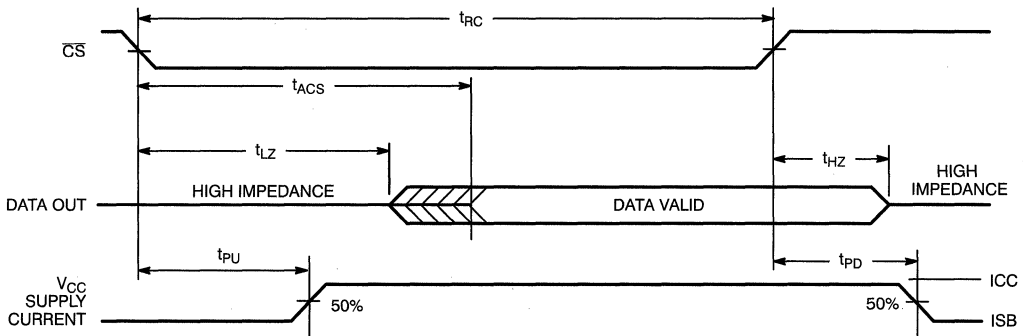
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	8	pF
C _{OUT}	Output Capacitance		8	pF

Notes:

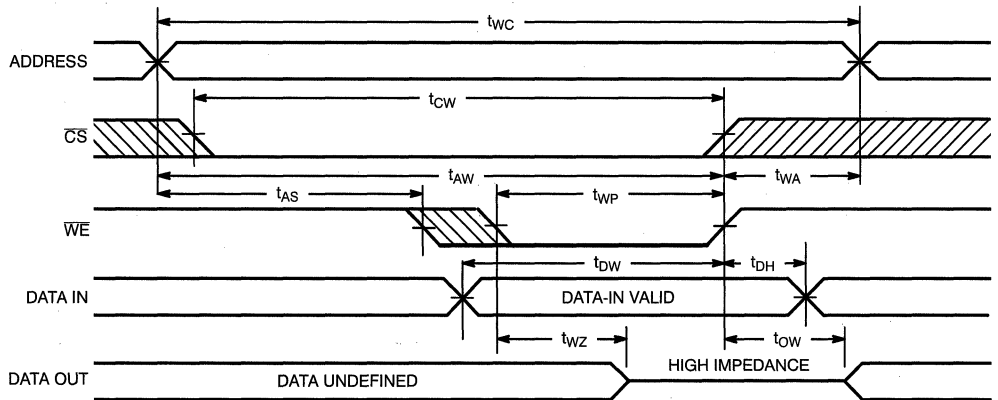
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- A pull-up resistor to V_{CC} on the \overline{CS} input is required to keep the device deselected during V_{CC} power-up. Otherwise current will exceed values given (CY7C148 only).
- For test purposes, not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

Switching Waveforms
Read Cycle No. 1^[10, 11]


C148-6

Read Cycle No. 2^[10, 12]


C148-7

Write Cycle No. 1 (\overline{WE} Controlled)


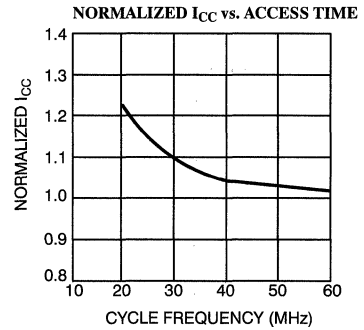
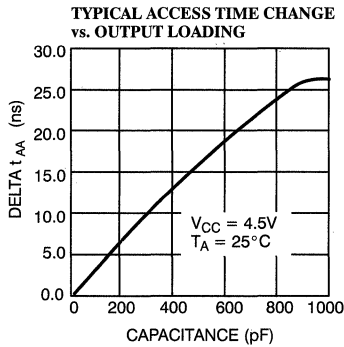
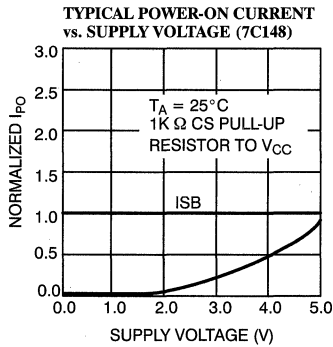
C148-8

Notes:

 10. \overline{WE} is HIGH for read cycle.

 11. Device is continuously selected, $\overline{CS} = V_{IL}$.

 12. Address valid prior to or coincident with \overline{CS} transition LOW.

Typical DC and AC Characteristics

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C148-25PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
35	CY7C148-35PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
	CY7C148-35DMB	D4	18-Lead (300-Mil) CerDIP	Military
45	CY7C148-45PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
	CY7C148-45DMB	D4	18-Lead (300-Mil) CerDIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C149-25PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
35	CY7C149-35PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
	CY7C149-35DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C149-35LMB	L50	18-Pin Rectangular Leadless Chip Carrier	
45	CY7C149-45PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
	CY7C149-45DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C149-45LMB	L50	18-Pin Rectangular Leadless Chip Carrier	

1K x 4 Static RAM
Features

- Memory reset function
- 1024 x 4 static RAM for control store in high-speed computers
- CMOS for optimum speed/power
- High speed
 - 10 ns (commercial)
 - 12 ns (military)
- Low power
 - 495 mW (commercial)
 - 550 mW (military)
- Separate inputs and outputs
- 5-volt power supply $\pm 10\%$ tolerance in both commercial and military
- Capable of withstanding greater than 2001V static discharge
- TTL-compatible inputs and outputs

Functional Description

The CY7C150 is a high-performance CMOS static RAM designed for use in cache memory, high-speed graphics, and data-acquisition applications. The CY7C150 has a memory reset feature that allows the entire memory to be reset in two memory cycles.

Separate I/O paths eliminates the need to multiplex data in and data out, providing for simpler board layout and faster system performance. Outputs are three-stated during write, reset, deselect, or when output enable (\overline{OE}) is held HIGH, allowing for easy memory expansion.

Reset is initiated by selecting the device ($\overline{CS} = \text{LOW}$) and taking the reset (\overline{RS}) input LOW. Within two memory cycles all bits are internally cleared to zero. Since chip select must be LOW for the device to be reset, a global reset signal can be

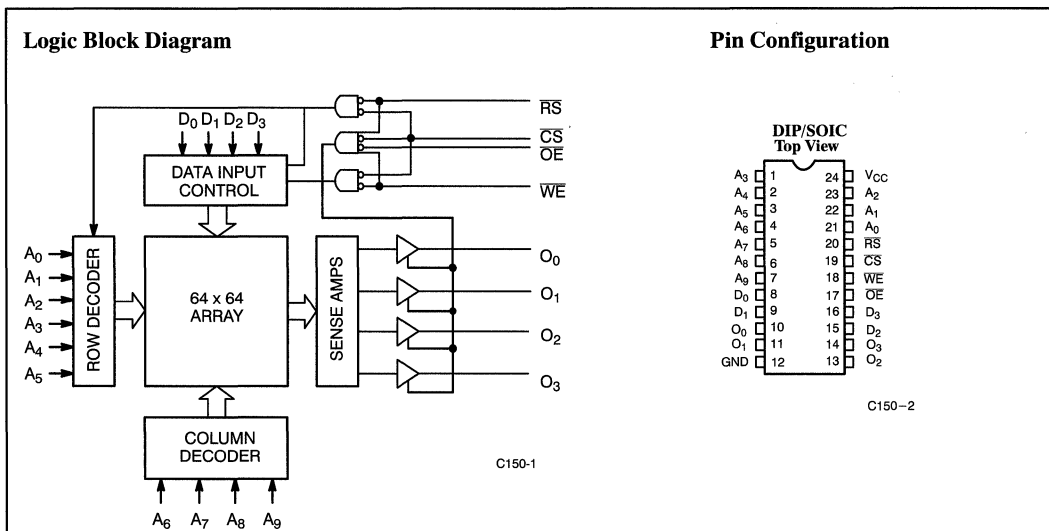
employed, with only selected devices being cleared at any given time.

Writing to the device is accomplished when the chip select (\overline{CS}) and write enable (\overline{WE}) inputs are both LOW. Data on the four data inputs (D_0 – D_3) is written into the memory location specified on the address pins (A_0 through A_9).

Reading the device is accomplished by taking chip select (\overline{CS}) and output enable (\overline{OE}) LOW while write enable (\overline{WE}) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four output pins (O_0 through O_3).

The output pins remain in high-impedance state when chip enable (\overline{CE}) or output enable (\overline{OE}) is HIGH, or write enable (\overline{WE}) or reset (\overline{RS}) is LOW.

A die coat is used to insure alpha immunity.


Selection Guide

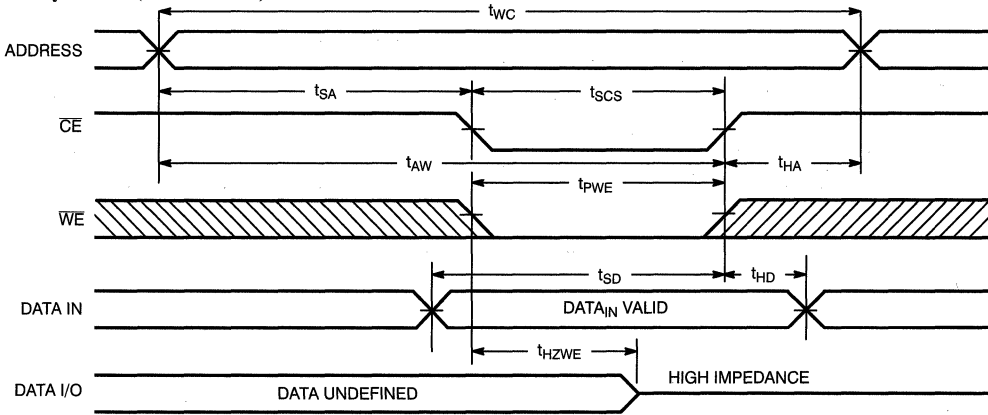
		7C150-10	7C150-12	7C150-15	7C150-25	7C150-35
Maximum Access Time (ns)	Commercial	10	12	15	25	
	Military		12	15	25	35
Maximum Operating Current (mA)	Commercial	90	90	90	90	90
	Military		100	100	100	100

Switching Characteristics Over the Operating Range^[2, 5]

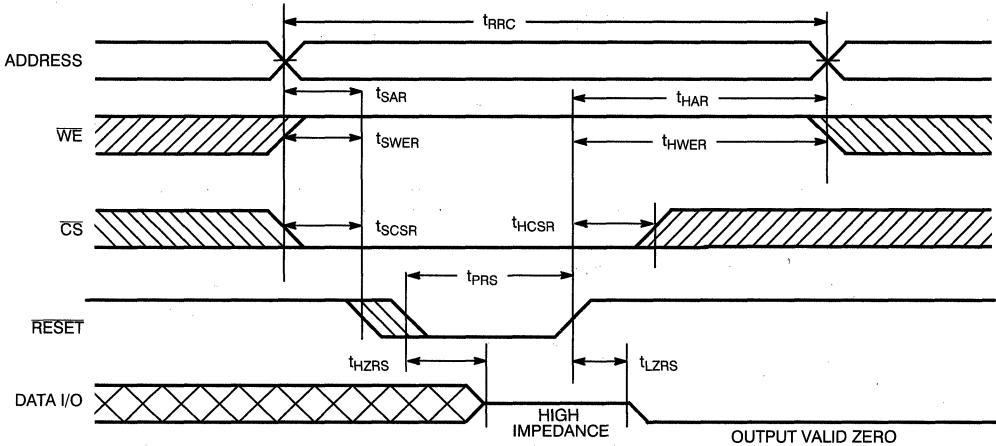
Parameter	Description	7C150-10		7C150-12		7C150-15		7C150-25		7C150-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	10		12		15		25		35		ns
t _{AA}	Address to Data Valid		10		12		15		25		35	ns
t _{OHA}	Output Hold from Address Change	2		2		2		2		2		ns
t _{ACS}	CS LOW to Data Valid		8		10		12		15		20	ns
t _{LZCS}	CS LOW to Low Z ^[6, 7]	0		0		0		0		0		ns
t _{HZCS}	CS HIGH to High Z ^[6, 7]		6		8		11		20		25	ns
t _{DOE}	OE LOW to Data Valid		6		8		10		15		20	ns
t _{LZOE}	OE LOW to Low Z ^[6]	0		0		0		0		0		ns
t _{HZOE}	OE HIGH to High Z ^[6, 7]		6		8		9		20		25	ns
WRITE CYCLE^[8]												
t _{WC}	Write Cycle Time	10		12		15		25		35		ns
t _{SCS}	CS LOW to Write End	6		8		11		15		20		ns
t _{AW}	Address Set-Up to Write End	8		10		13		20		30		ns
t _{HA}	Address Hold from Write End	2		2		2		5		5		ns
t _{SA}	Address Set-Up to Write Start	2		2		2		5		5		ns
t _{PWE}	WE Pulse Width	6		8		11		15		20		ns
t _{SD}	Data Set-Up to Write End	6		8		11		15		20		ns
t _{HD}	Data Hold from Write End	2		2		2		5		5		ns
t _{LZWE}	WE HIGH to Low Z ^[6]	0		0		0		0		0		ns
t _{HZWE}	WE LOW to High Z ^[6, 7]		6		8		12		20		25	ns
RESET CYCLE												
t _{RRC}	Reset Cycle Time	20		24		30		50		70		ns
t _{SAR}	Address Valid to Beginning of Reset	0		0		0		0		0		ns
t _{SWER}	Write Enable HIGH to Beginning of Reset	0		0		0		0		0		ns
t _{SCSR}	Chip Select LOW to Beginning of Reset	0		0		0		0		0		ns
t _{PRS}	Reset Pulse Width	10		12		15		20		30		ns
t _{HCSR}	Chip Select Hold After End of Reset	0		0		0		0		0		ns
t _{HWER}	Write Enable Hold After End of Reset	8		12		15		30		40		ns
t _{HAR}	Address Hold After End of Reset	10		12		15		30		40		ns
t _{LZRS}	Reset HIGH to Output in Low Z ^[6]	0		0		0		0		0		ns
t _{HZRS}	Reset LOW to Output in High Z ^[6, 7]		6		8		12		20		25	ns

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
- t_{HZCS}, t_{HZOE}, t_{HZR}, and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of CS LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be reference to the rising edge of the signal that terminates the write.

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{CS} Controlled)^[8, 12]


C150-8

Reset Cycle^[13]


C150-9

Notes:

12. If \overline{CS} goes HIGH with \overline{WE} HIGH, the output remains in a high-impedance state.

13. Reset cycle is defined by the overlap of \overline{RS} and \overline{CS} for the minimum reset pulse width.

Truth Table

Inputs				Outputs	Mode
CS	WE	OE	RS		
H	X	X	X	High Z	Not Selected
L	H	X	L	High Z	Reset
L	L	X	H	High Z	Write
L	H	L	H	O ₀ –O ₃	Read
L	X	H	H	High Z	Output Disable

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C150–10PC	P13A	24-Lead (300-Mil) MoldedDIP	Commercial
	CY7C150–10SC	S13	24-Lead Molded SOIC	
12	CY7C150–12PC	P13A	24-Lead (300-Mil) MoldedDIP	Commercial
	CY7C150–12SC	S13	24-Lead Molded SOIC	
	CY7C150–12DMB	D14	24-Lead (300-Mil) CerDIP	Military
15	CY7C150–15PC	P13A	24-Lead (300-Mil) MoldedDIP	Commercial
	CY7C150–15SC	S13	24-Lead Molded SOIC	
	CY7C150–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
25	CY7C150–25PC	P13A	24-Lead (300-Mil) MoldedDIP	Commercial
	CY7C150–25SC	S13	24-Lead Molded SOIC	
	CY7C150–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
35	CY7C150–35DMB	D14	24-Lead (300-Mil) CerDIP	Military



CY7C161 CY7C162

16K x 4 Static RAM with Separate I/O

Features

- High speed
— 15-ns
- Transparent write (7C161)
- CMOS for optimum speed/power
- Low active power
— 633 mW
- Low standby power
— 220 mW
- TTL compatible inputs and outputs
- Automatic power-down when deselected

Functional Description

The CY7C161 and CY7C162 are high-performance CMOS static RAMs organized as 16,384 by 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables (\overline{CE}_1 , \overline{CE}_2) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 65% when deselected.

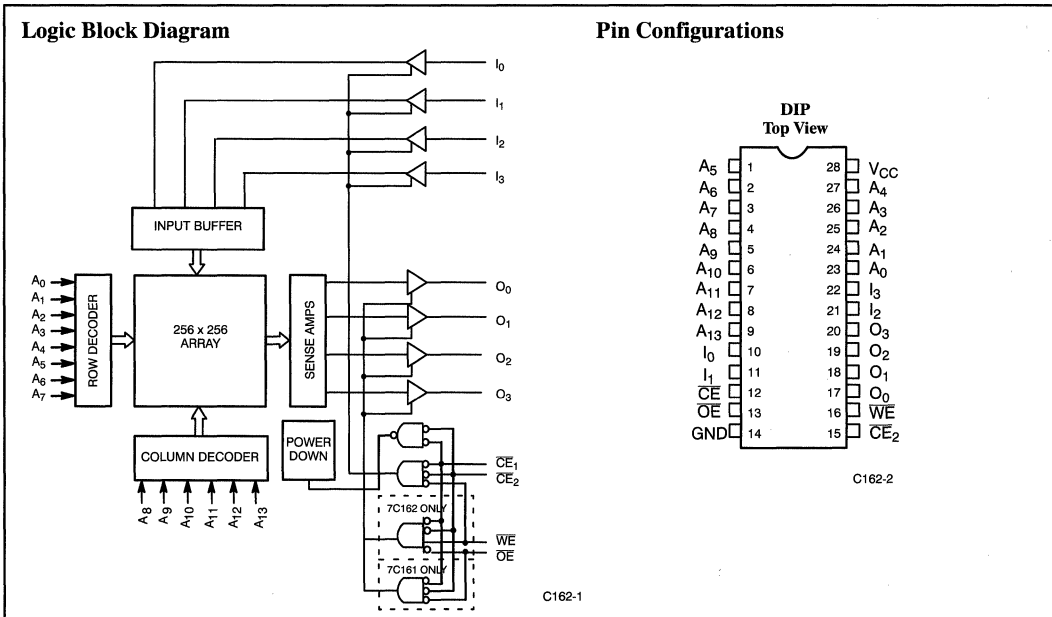
Writing to the device is accomplished when the chip enable (\overline{CE}_1 , \overline{CE}_2) and write enable (\overline{WE}) inputs are both LOW. Data on the four input pins (I_0 through I_3) is written

into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enables (\overline{CE}_1 , \overline{CE}_2) LOW while write enable (\overline{WE}) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins stay in a high-impedance state when write enable (\overline{WE}) is LOW (7C162 only), or one of the chip enables (\overline{CE}_1 , \overline{CE}_2) are HIGH.

A die coat is used to ensure alpha immunity.



Selection Guide^[1]

	7C161-12 7C162-12	7C161-15 7C162-15	7C161-20 7C162-20	7C161-25 7C162-25	7C161-35 7C162-35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	160	115	80	70	70
Maximum Standby Current (mA)	40/20	40/20	40/20	20/20	20/20

Shaded areas indicate preliminary information.

Note:

1. For military specifications, see the CY7C161A/CY7C162A datasheet.

Electrical Characteristics Over the Operating Range (continued)

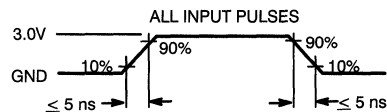
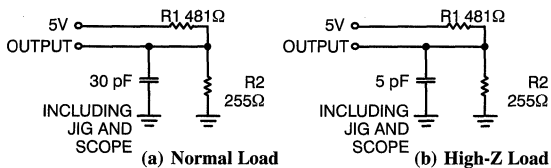
Parameter	Description	Test Conditions	7C161-20 7C162-20		7C161-25,35 7C162-25,35		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[2]		-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		80		70	mA
I _{SB1}	Automatic \overline{CE}_1 Power-Down Current	Max. V _{CC} , CE ₁ ≥ V _{IH} Min. Duty Cycle = 100%		40		20	mA
I _{SB2}	Automatic \overline{CE}_1 Power-Down Current	Max. V _{CC} , CE ₁ ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20		20	mA

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

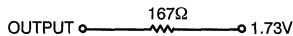
- Minimum voltage is equal to -3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

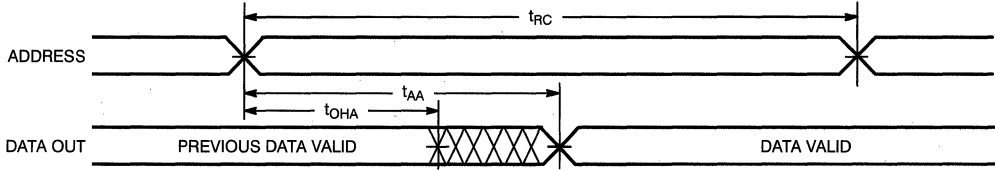
AC Test Loads and Waveforms


C162-3

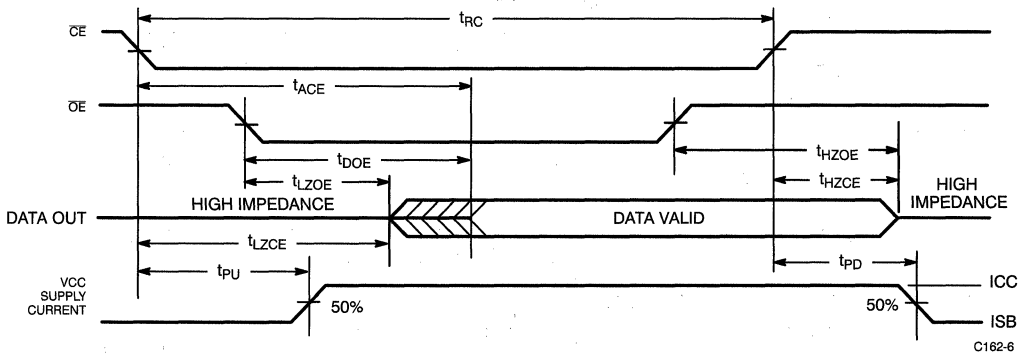
C162-4

Equivalent to: THEVENIN EQUIVALENT

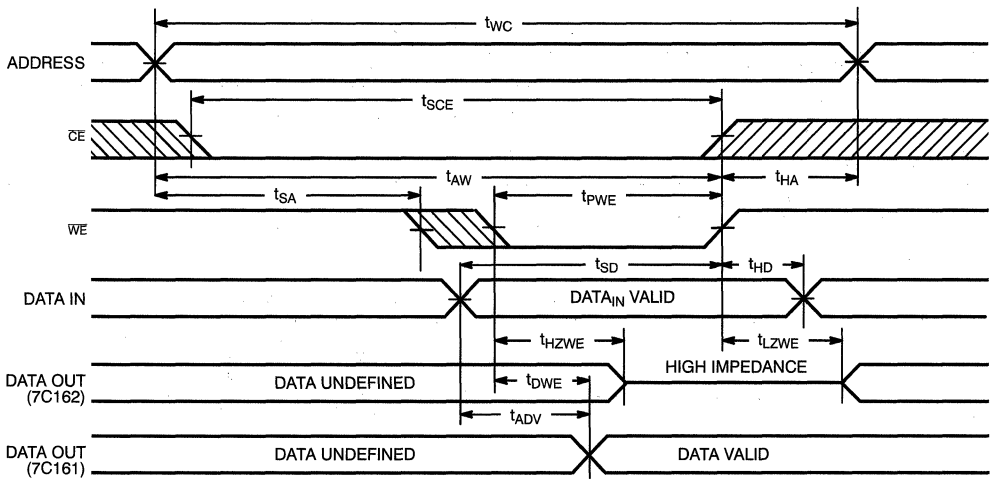


Switching Waveforms^[8]
Read Cycle No. 1^[10, 11]


C162-5

Read Cycle No. 2^[10, 12]


C162-6

Write Cycle No. 1 (\overline{WE} Controlled)^[9]


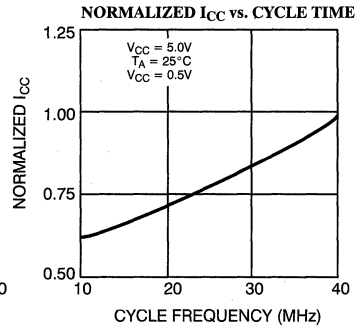
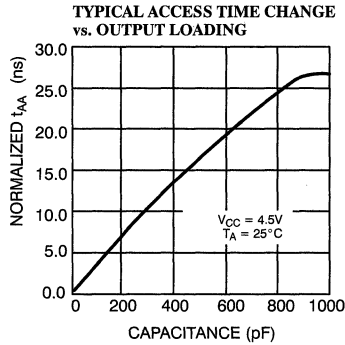
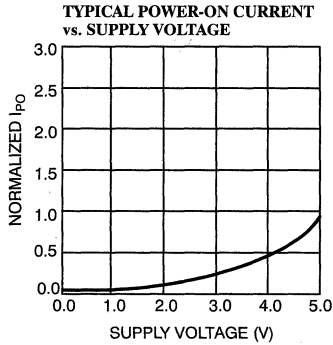
C162-7

Notes:

 10. \overline{WE} is HIGH for read cycle.

 11. Device is continuously selected, $\overline{CE}_1, \overline{CE}_2 = V_{IL}$.

 12. Address valid prior to or coincident with $\overline{CE}_1, \overline{CE}_2$ transition LOW.

Typical DC and AC Characteristics (continued)

Address Designators

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y0	6
A11	Y1	7
A12	Y5	8
A13	Y4	9
A0	Y3	23
A1	Y2	24
A2	X0	25
A3	X1	26
A4	X2	27

16K x 4 Static RAM with Separate I/O

Features

- High speed
— 20 ns t_{AA}
- CMOS for optimum speed/power
- Transparent write (7C161A)
- Low active power
— 550 mW
- Low standby power
— 220 mW
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

Functional Description

The CY7C161A and CY7C162A are high-performance CMOS static RAMs organized as 16,384 by 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables (\overline{CE}_1 , \overline{CE}_2) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 60% when deselected.

Writing to the device is accomplished when the chip enable (\overline{CE}_1 , \overline{CE}_2) and write enable (\overline{WE}) inputs are both LOW. Data on the four input pins (I_0 through I_3) is written

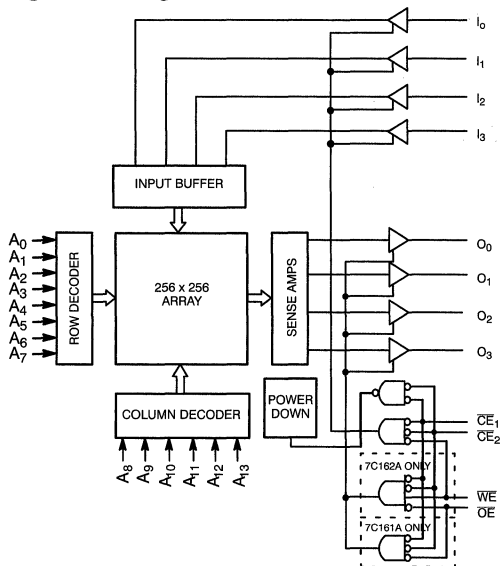
into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enables (\overline{CE}_1 , \overline{CE}_2) LOW while write enable (\overline{WE}) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

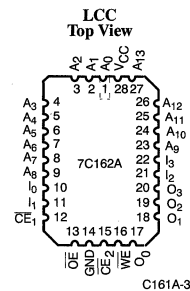
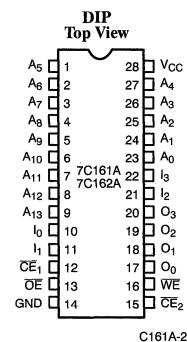
The output pins stay in high-impedance state when write enable (\overline{WE}) is LOW (7C162A only), or one of the chip enables (\overline{CE}_1 , \overline{CE}_2) are HIGH.

A die coat is used to ensure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide^[1]

		7C161A-15 7C162A-15	7C161A-20 7C162A-20	7C161A-25 7C162A-25	7C161A-35 7C162A-35
Maximum Access Time (ns)		15	20	25	35
Maximum Operating Current (mA)	Military	160	100	100	100
Maximum Standby Current (mA)	Military	40/20	40/20	40/20	30/20

Shaded area contains preliminary information.

Note:

1. For commercial specifications, see the CY7C161/CY7C162 datasheet.

Electrical Characteristics Over the Operating Range^[4] (continued)

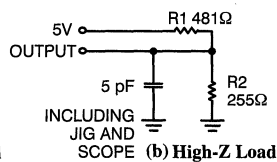
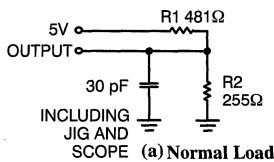
Parameter	Description	Test Conditions	7C161A-25 7C162A-25		7C161A-35 7C162A-35		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[2]		-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		100		100	mA
I _{SB1}	Automatic \overline{CE} Power-Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, Min. Duty Cycle = 100%		40		30	mA
I _{SB2}	Automatic \overline{CE} Power-Down Current	Max. V _{CC} , $\overline{CE}_1 \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		20		20	mA

Capacitance^[6]

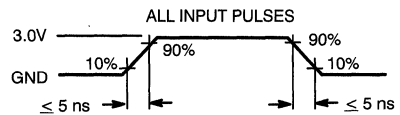
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

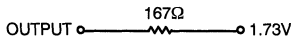
AC Test Loads and Waveforms


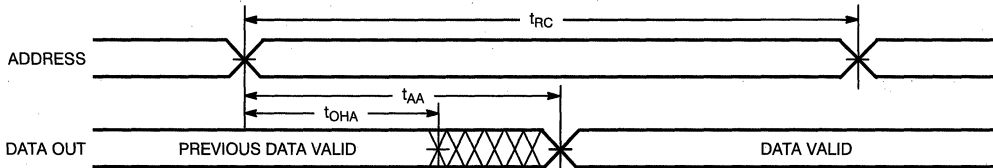
C161A-4



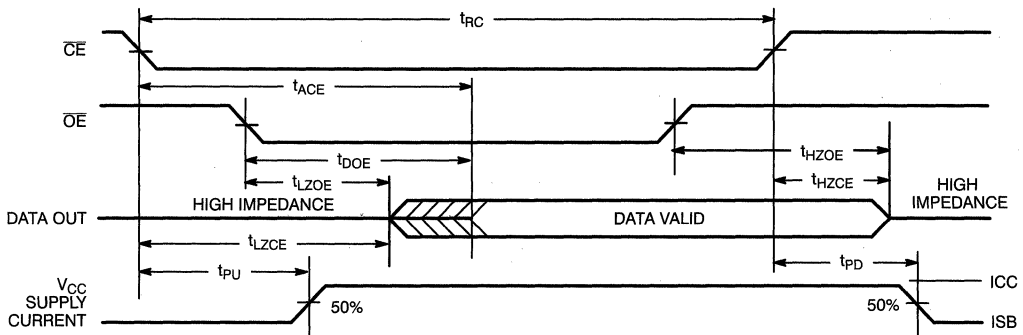
C161A-5

Equivalent to: THÉVENIN EQUIVALENT

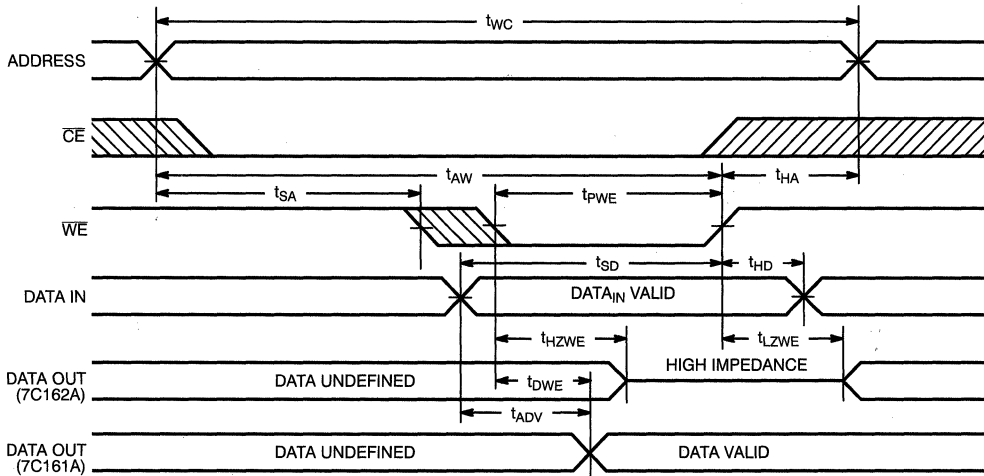


Switching Waveforms^[8]
Read Cycle No. 1^[12, 13]


C161A-6

Read Cycle No. 2^[12, 14]


C161A-7

Write Cycle No. 1 (WE Controlled)^[11]


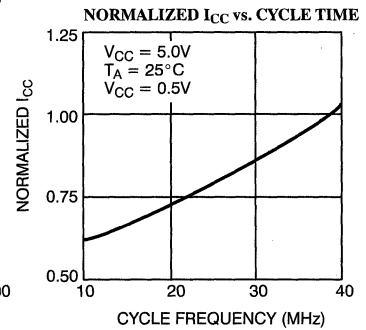
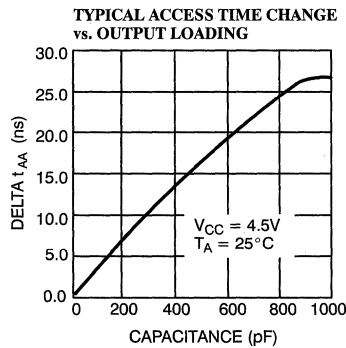
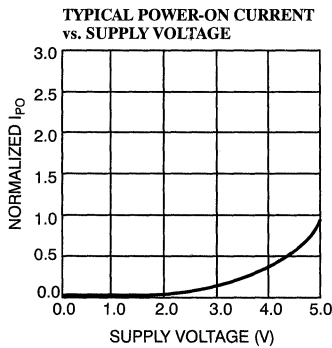
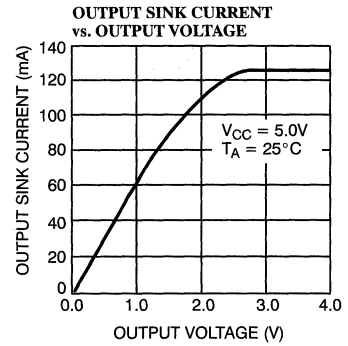
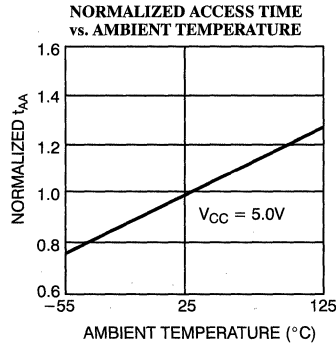
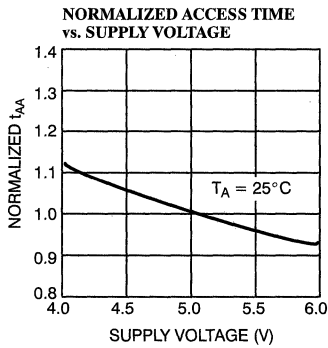
C161A-8

Notes:

12. WE is HIGH for read cycle.

 13. Device is continuously selected, $\overline{CE}_1, \overline{CE}_2 = V_{IL}$.

 14. Address valid prior to or coincident with $\overline{CE}_1, \overline{CE}_2$ transition LOW.

Typical DC and AC Characteristics (continued)

Address Designators

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y0	6
A11	Y1	7
A12	Y5	8
A13	Y4	9
A0	Y3	23
A1	Y2	24
A2	X0	25
A3	X1	26
A4	X2	27

16K x 4 Static RAM

Features

- High speed
— 15 ns
- Output enable (\overline{OE}) feature (7C166)
- CMOS for optimum speed/power
- Low active power
— 633 mW
- Low standby power
— 220 mW
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

Functional Description

The CY7C164 and CY7C166 are high-performance CMOS static RAMs organized as 16,384 by 4 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}) and three-state drivers. The CY7C166 has an active low output enable (\overline{OE}) feature. Both devices have an automatic power-down feature, reducing the power consumption by 65% when deselected.

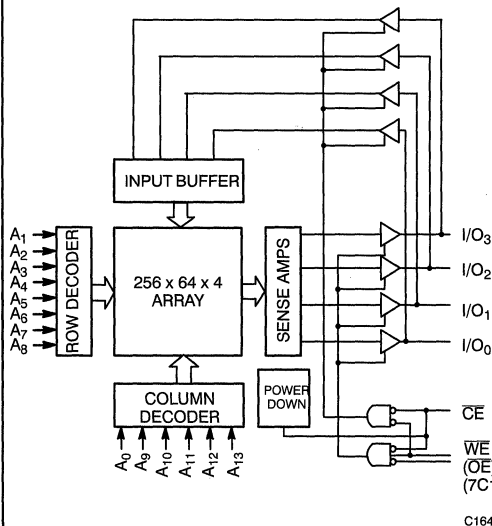
Writing to the device is accomplished when the chip enable (\overline{CE}) and write enable (\overline{WE}) inputs are both LOW (and the output enable (\overline{OE}) is LOW for the 7C166).

Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

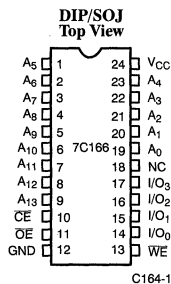
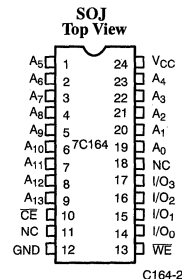
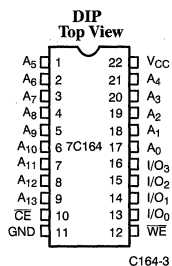
Reading the device is accomplished by taking chip enable (\overline{CE}) LOW (and \overline{OE} LOW for 7C166), while write enable (\overline{WE}) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in a high-impedance state when chip enable (\overline{CE}) is HIGH (or output enable (\overline{OE}) is HIGH for 7C166). A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configurations



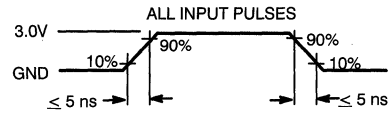
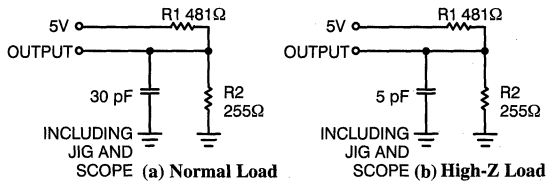
Selection Guide^[1]

	7C164-12 7C166-12	7C164-15 7C166-15	7C164-20 7C166-20	7C164-25 7C166-25	7C164-35 7C166-35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	160	115	80	70	70
Maximum Standby Current (mA)	40/20	40/20	40/20	20/20	20/20

Shaded area contains preliminary information.

Note:

1. For military specifications, see the CY6C164A/CY7C166A datasheet.

AC Test Loads and Waveforms


C164-6

 Equivalent to: THÉVENIN EQUIVALENT
 OUTPUT ——— 167Ω ——— 1.73V

C164-5

Switching Characteristics Over the Operating Range^[6]

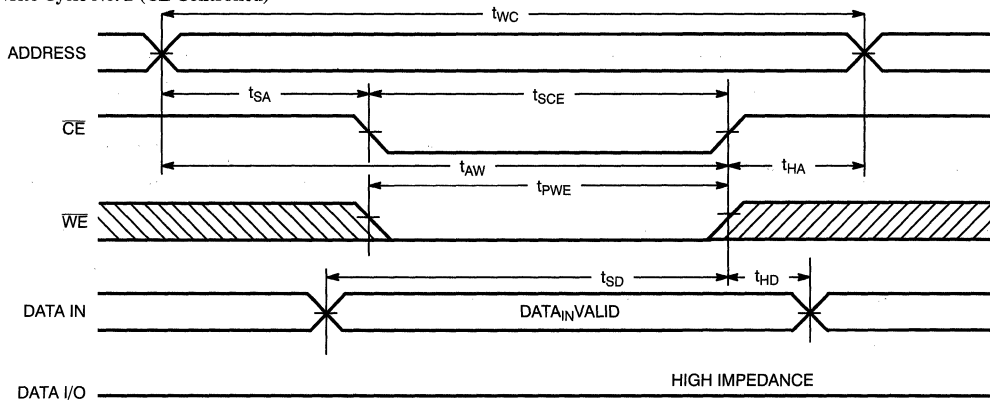
Parameter	Description	7C164-12 7C166-12		7C164-15 7C166-15		7C164-20 7C166-20		7C164-25 7C166-25		7C164-35 7C166-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	12		15		20		25		35		ns
t _{AA}	Address to Data Valid		12		15		20		25		35	ns
t _{OHA}	Output Hold from Address Change	3		3		5		5		5		ns
t _{ACE}	\overline{CE} LOW to Data Valid		12		15		20		25		35	ns
t _{DOE}	\overline{OE} LOW to Data Valid	7C166	6		10		10		12		15	ns
t _{LZOE}	\overline{OE} LOW to Low Z	7C166	0		3		3		3		3	ns
t _{HZOE}	\overline{OE} HIGH to High Z	7C166	7		8		8		10		12	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[7]	3		3		5		5		5		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[7, 8]		7		8		8		10		15	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		12		15		20		20		20	ns
WRITE CYCLE^[9]												
t _{WC}	Write Cycle Time	12		15		20		20		25		ns
t _{SCE}	\overline{CE} LOW to Write End	8		12		15		20		25		ns
t _{AW}	Address Set-Up to Write End	9		12		15		20		25		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	8		12		15		15		20		ns
t _{SD}	Data Set-Up to Write End	6		10		10		10		15		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[7]	3		5		5		5		5		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[7, 8]		6		7		7		7		10	ns

Shaded area contains preliminary information.

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed by design and not 100% tested.
- t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) in AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

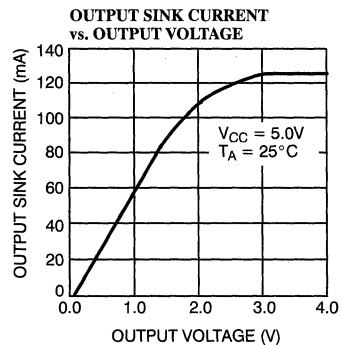
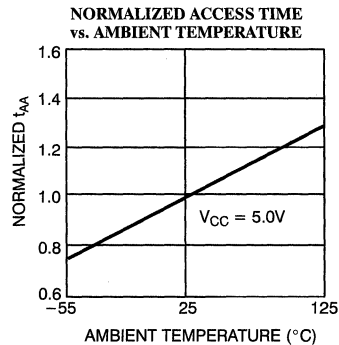
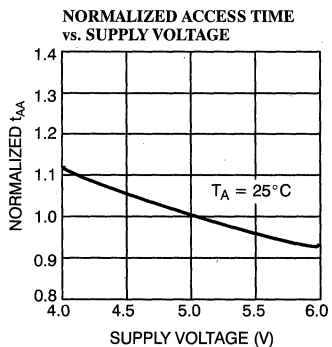
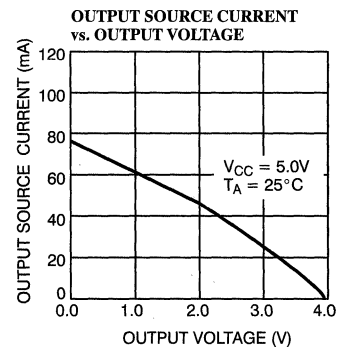
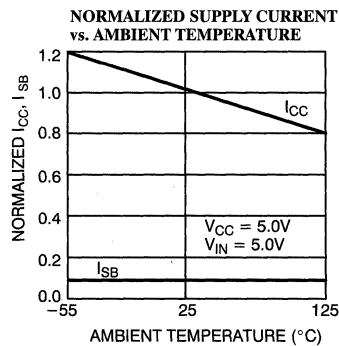
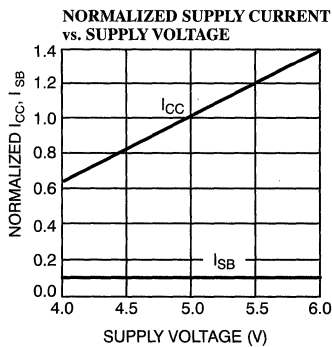
Switching Waveforms (continued)

 Write Cycle No. 2 (\overline{CE} Controlled)^[9, 13, 14]


C164-10

Note:

14. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics


Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C164-12PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-12VC	V13	24-Lead Molded SOJ	
15	CY7C164-15PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-15VC	V13	24-Lead Molded SOJ	
20	CY7C164-20PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-20VC	V13	24-Lead Molded SOJ	
25	CY7C164-25PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-25VC	V13	24-Lead Molded SOJ	
35	CY7C164-35PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-35VC	V13	24-Lead Molded SOJ	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C166-12PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-12VC	V13	24-Lead Molded SOJ	
15	CY7C166-15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-15VC	V13	24-Lead Molded SOJ	
20	CY7C166-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-20VC	V13	24-Lead Molded SOJ	
25	CY7C166-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-25VC	V13	24-Lead Molded SOJ	
35	CY7C166-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-35VC	V13	24-Lead Molded SOJ	

Shaded areas contain preliminary information.

Document #: 38-00032-I



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied -55°C to +125°C
 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Voltage Applied to Outputs in High Z State^[2] -0.5V to +7.0V
 DC Input Voltage^[2] -0.5V to +7.0V

Output Current into Outputs (Low) 20 mA
 Static Discharge Voltage (per MIL-STD-883, Method 3015) >2001V
 Latch-up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Military ^[3]	-55°C to +125°C	5V ± 10%

Notes:

- Minimum voltage is equal to -3.0V for pulse durations less than 30 ns.
- T_A is the “instant on” case temperature.

Electrical Characteristics Over the Operating Range^[4]

Parameter	Description	Test Conditions	7C164A-15 7C166A-15		7C164A-20 7C166A-20		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[2]		-3.0	0.8	-3.0	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	µA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	µA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		160		100	mA
I _{SB1}	Automatic \overline{CE} ^[6] Power Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH}$ Min. Duty Cycle = 100%		40		40	mA
I _{SB2}	Automatic \overline{CE} ^[6] Power Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH} - 0.3V$ V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20		20	mA

Shaded area contains preliminary information.

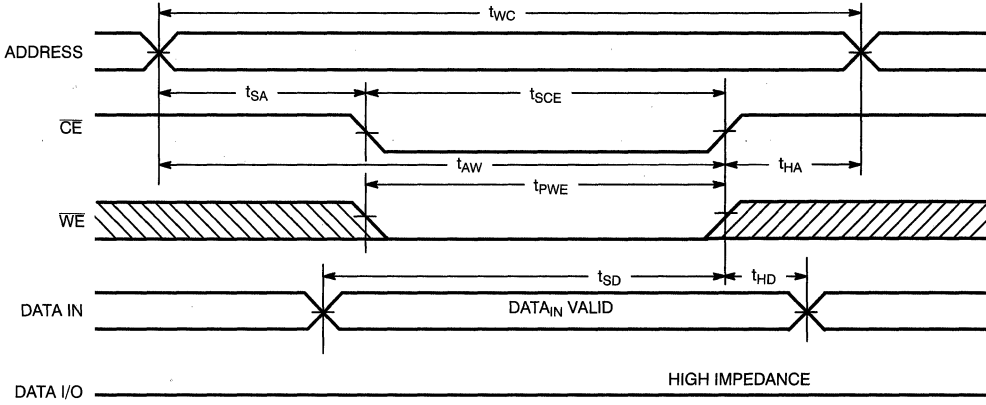
Switching Characteristics Over the Operating Range^[4, 8]

Parameter	Description	7C164A-15 7C166A-15		7C164A-20 7C166A-20		7C164A-25 7C166A-25		7C164A-35 7C166A-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t _{RC}	Read Cycle Time	15		20		25		35		ns
t _{AA}	Address to Data Valid		15		20		25		35	ns
t _{OHA}	Output Hold from Address Change	3		3		3		3		ns
t _{ACE}	CE LOW to Data Valid		15		20		25		35	ns
t _{DOE}	OE LOW to Data Valid (7C166A)		7		10		12		15	ns
t _{LZOE}	OE LOW to Low Z (7C166A)	0		3		3		3		ns
t _{HZOE}	OE HIGH to High Z (7C166A)		8		8		10		12	ns
t _{LZCE}	CE LOW to Low Z ^[9]	3		5		5		5		ns
t _{HZCE}	CE HIGH to High Z ^[9, 10]		8		8		10		15	ns
t _{PU}	CE LOW to Power-Up	0		0		0		0		ns
t _{PD}	CE HIGH to Power-Down		15		20		20		20	ns
WRITE CYCLE^[11]										
t _{WC}	Write Cycle Time	15		20		20		25		ns
t _{SCE}	CE LOW to Write End	10		15		20		25		ns
t _{AW}	Address Set-Up to Write End	10		15		20		25		ns
t _{HA}	Address Hold from Write End	0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t _{PWE}	WE Pulse Width	10		15		15		20		ns
t _{SD}	Data Set-Up to Write End	7		10		10		15		ns
t _{HD}	Data Hold from Write End	0		0		0		0		ns
t _{LZWE}	WE HIGH to Low Z ^[9]	3		5		5		5		ns
t _{HZWE}	WE LOW to High Z ^[9, 10]		7		7		7		10	ns

Shaded area contains preliminary information.

Notes:

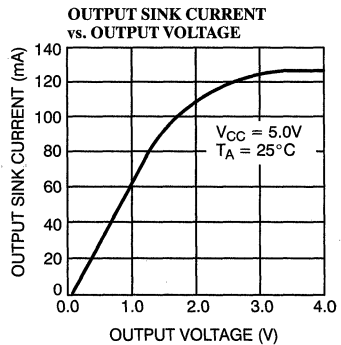
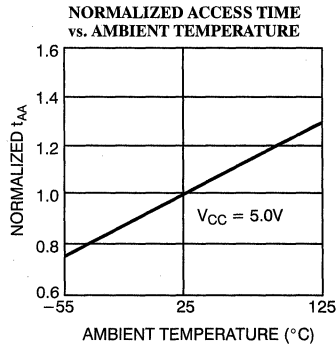
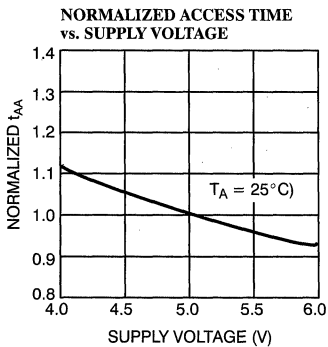
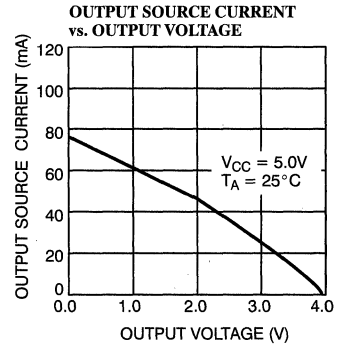
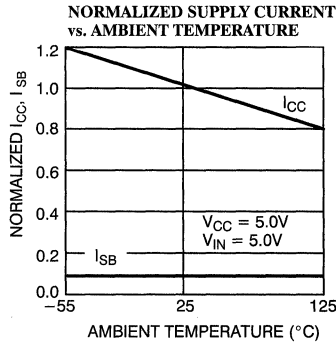
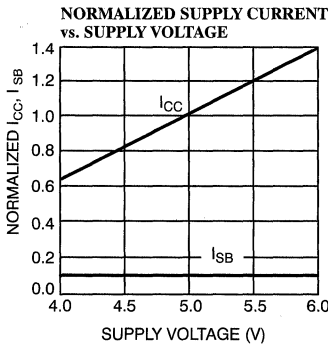
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed by design and not 100% tested.
- t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) in AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms (continued)
Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)^[11, 15, 16]


C164A-9

Note:

16. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics


Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
15	CY7C164A-15DMB	D10	22-Lead (300-Mil) CerDIP	Military
20	CY7C164A-20DMB	D10	22-Lead (300-Mil) CerDIP	Military
25	CY7C164A-25DMB	D10	22-Lead (300-Mil) CerDIP	Military
35	CY7C164A-35DMB	D10	22-Lead (300-Mil) CerDIP	Military
Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
15	CY7C166A-15DMB	D14	24-Lead (300-Mil) CerDIP	Military
20	CY7C166A-20DMB	D14	24-Lead (300-Mil) CerDIP	Military
25	CY7C166A-25DMB	D14	24-Lead (300-Mil) CerDIP	Military
35	CY7C166A-35DMB	D14	24-Lead (300-Mil) CerDIP	Military

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
$V_{IL Max.}$	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB1}	1, 2, 3

Document #: 38-00113-D

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
$t_{DOE}^{[17]}$	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Note:

17. 7C166A only.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 20 to Pin 10)	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-3.0V to +7.0V

Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military ^[1]	-55°C to +125°C	5V ± 10%

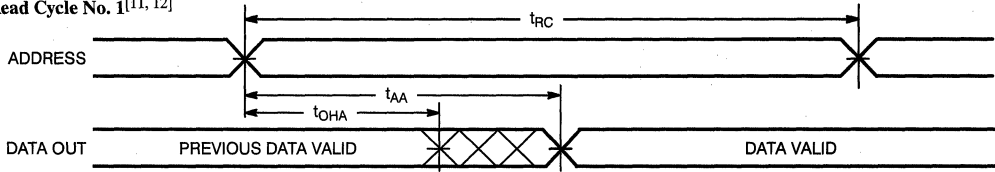
Electrical Characteristics Over the Operating Range^[2]

Parameter	Description	Test Conditions	7C167A-15		7C167A-20		7C167A-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output High Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output Low Voltage	V _{CC} = Min., I _{OL} = 12.0 mA, 8.0 mA Mil		0.4		0.4		0.4	V
V _{IH}	Input High Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input Low Voltage ^[3]		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} Output Disabled	-10	+10	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-350		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	90		80	60		mA
			Mil			80	70		
I _{SB}	Automatic \overline{CE} Power-Down Current ^[5]	Max. V _{CC} , $\overline{CE} \geq V_{IH}$	Com'l	40		40	20		mA
			Mil			40	20		

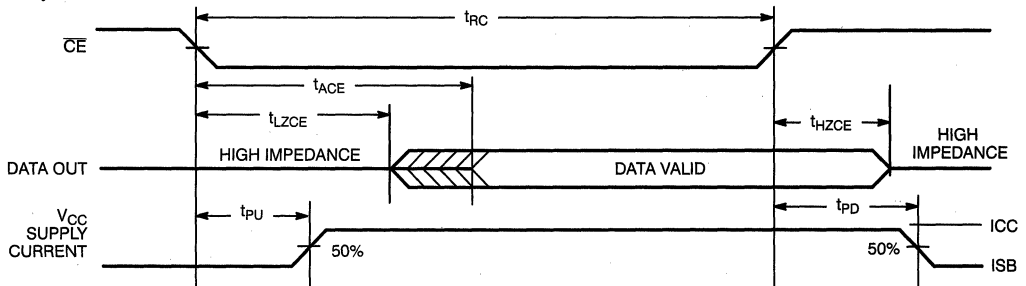
Parameter	Description	Test Conditions	7C167A-35		7C167A-45		Unit	
			Min.	Max.	Min.	Max.		
V _{OH}	Output High Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V	
V _{OL}	Output Low Voltage	V _{CC} = Min., I _{OL} = 12.0 mA, 8.0 mA Mil		0.4		0.4	V	
V _{IH}	Input High Voltage		2.2	V _{CC}	2.2	V _{CC}	V	
V _{IL}	Input Low Voltage ^[3]		-0.5	0.8	-0.5	0.8	V	
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} Output Disabled	-10	+10	-10	+10	μA	
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-350		-350	mA	
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	60		50		mA
			Mil		60		50	
I _{SB}	Automatic \overline{CE} Power-Down Current ^[5]	Max. V _{CC} , $\overline{CE} \geq V_{IH}$	Com'l	20				mA
			Mil		20		20	

Notes:

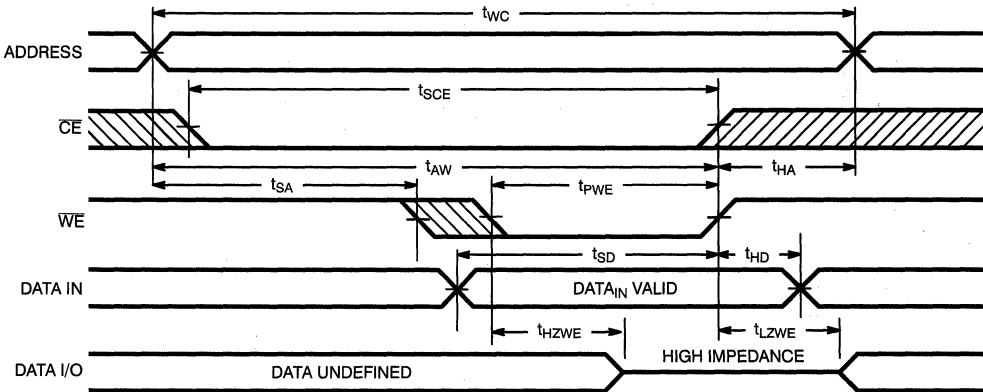
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} min. = -3.0V for pulse durations less than 30 ns.
4. Duration of the short circuit should not exceed 30 seconds.
5. A pull-up resistor to V_{CC} on the \overline{CE} input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

Switching Waveforms
Read Cycle No. 1^[11, 12]


C167A-5

Read Cycle No. 2^[11, 13]


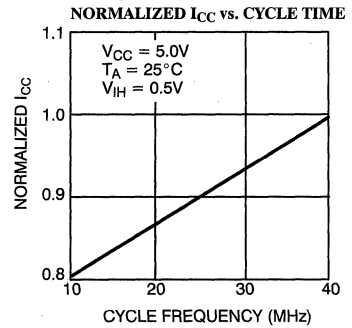
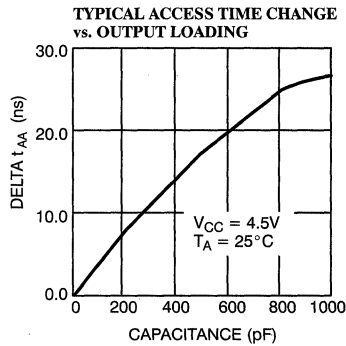
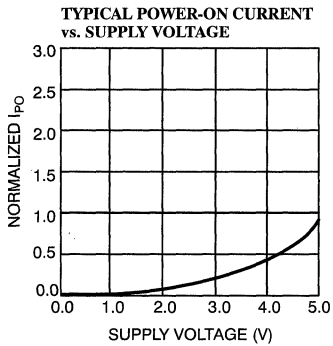
C167A-6

Write Cycle No. 1 (WE Controlled)^[10]


C167A-7

Notes:

11. \overline{WE} is high for read cycle.
12. Device is continuously selected, $\overline{CE} = V_{IL}$.
13. Address valid prior to or coincident with \overline{CE} transition LOW.
14. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics (continued)

Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	80	CY7C167A-15PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C167A-15VC	V5	20-Lead Molded SOJ	
20	80	CY7C167A-20PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C167A-20VC	V5	20-Lead Molded SOJ	
		CY7C167A-20DMB	D6	20-Lead (300-Mil) CerDIP	Military
25	60	CY7C167A-25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C167A-25VC	V5	20-Lead Molded SOJ	
		CY7C167A-25DMB	D6	20-Lead (300-Mil) CerDIP	Military
35	60	CY7C167A-35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C167A-35VC	V5	20-Lead Molded SOJ	
		CY7C167A-35DMB	D6	20-Lead (300-Mil) CerDIP	Military
45	50	CY7C167A-45DMB	D6	20-Lead (300-Mil) CerDIP	Military

4K x 4 Static RAM
Features

- Automatic power-down when deselected (CY7C168A)
- CMOS for optimum speed/power
- High speed
 - $t_{AA} = 15$ ns
 - $t_{ACE} = 10$ ns (CY7C169A)
- Low active power
 - 385 mW
- Low standby power (CY7C168A)
 - 83 mW
- TTL-compatible inputs and outputs
- V_{IH} of 2.2V
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C168A and CY7C169A are high-performance CMOS static RAMs organized as 4096 by 4 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}) and three-state drivers. The CY7C168A has an automatic power-down feature, reducing the power consumption by 77% when deselected.

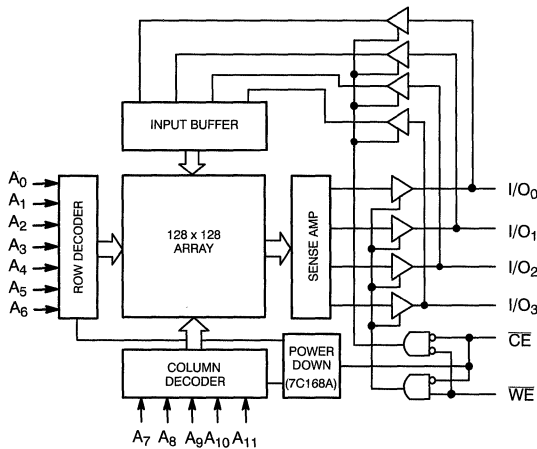
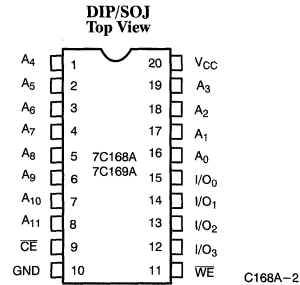
Writing to the device is accomplished when the chip select (\overline{CE}) and write enable (\overline{WE}) inputs are both LOW. Data on the four data input/output pins (I/O_0 through I/O_3) is written into the memory location

specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking the chip enable (\overline{CE}) LOW, while (\overline{WE}) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the four data input/output pins (I/O_0 through I/O_3).

The input/output pins remain in a high-impedance state when chip enable is HIGH or write enable (\overline{WE}) is LOW.

A die coat is used to insure alpha immunity.

Logic Block Diagram

Pin Configurations

Selection Guide

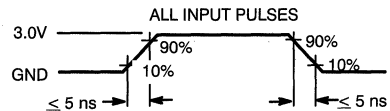
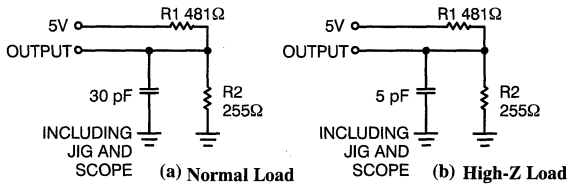
		7C168A-15 7C169A-15	7C168A-20 7C169A-20	7C168A-25 7C169A-25	7C168A-35 7C169A-35	7C168A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	115	90	70	70	
	Military		90	80	70	70

Electrical Characteristics Over the Operating Range^[2] (continued)

Parameter	Description	Test Conditions	7C168A-25 7C169A-25		7C168A-35 7C169A-35		7C168A-45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[3]		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	10	-10	10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} Output Disabled	-10	+10	-50	50	-50	50	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-350		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	70		70			mA
			Mil	80		70	70		
I _{SB1}	Automatic CS Power-Down Current	Max. V _{CC} , CE ≥ V _{IH}	Com'l	20		20			mA
			Mil	20		20	20		
I _{SB2}	Automatic CE Power-Down Current	Max. V _{CC} , CE ≥ V _{CC} - 0.3 V	Com'l	20		20			mA
			Mil	20		20	20		

Capacitance^[5]

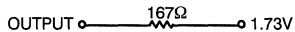
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms


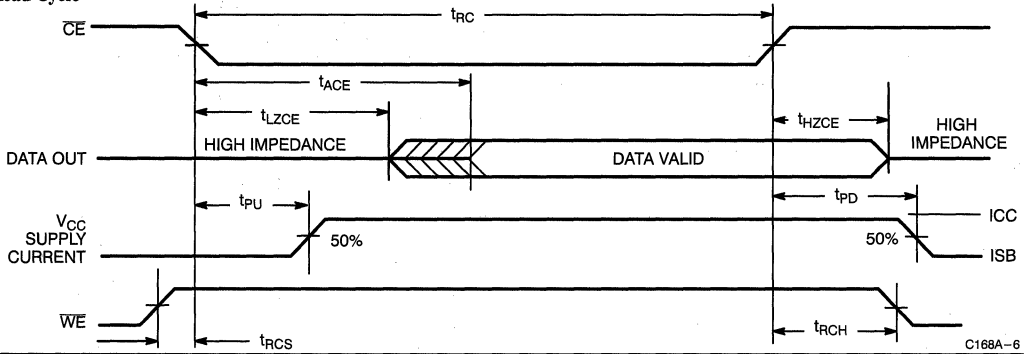
C168A-4

C168A-3

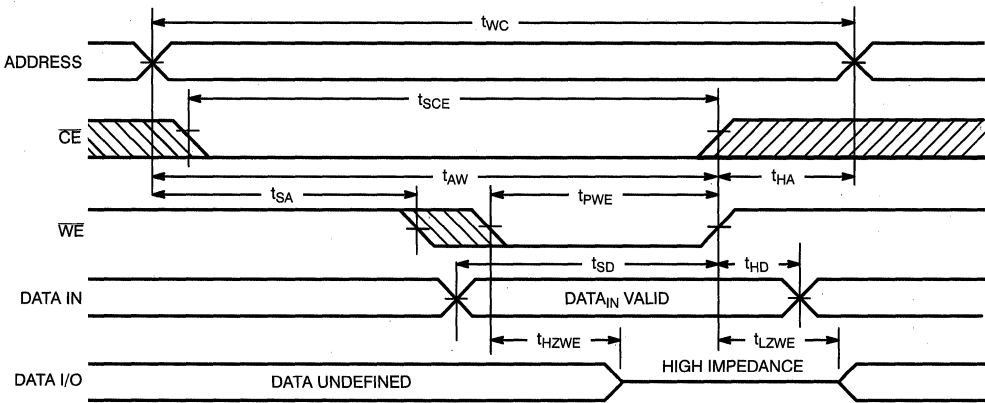
Equivalent to: THEVENIN EQUIVALENT


Notes:

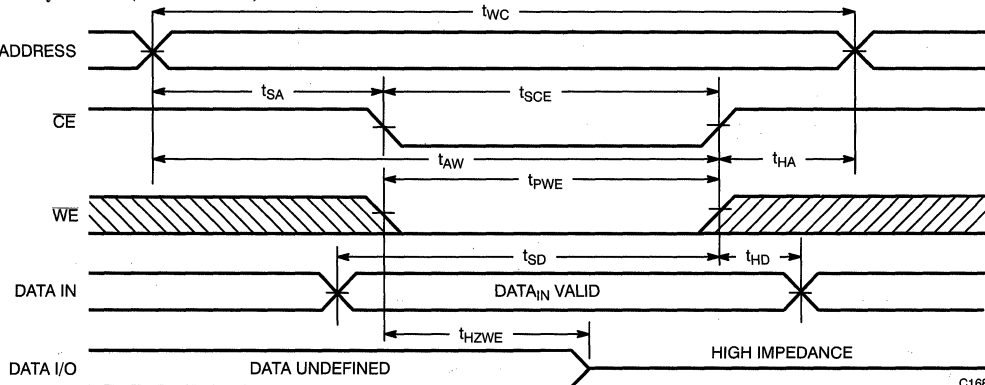
5. Tested initially and after any design or process changes that may affect these parameters.

Switching Waveforms (continued)
Read Cycle^[11, 13]


C168A-6

Write Cycle No. 1 (WE Controlled)^[10]


C168A-7

Write Cycle No. 2 (\overline{CS} Controlled)^[10, 14]


C168A-8

Ordering Information

Speed (ns)	I _{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	115	CY7C168A-15PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C168A-15VC	V5	20-Lead Molded SOJ	
20	90	CY7C168A-20PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C168A-20VC	V5	20-Lead Molded SOJ	
		CY7C168A-20DMB	D6	20-Lead (300-Mil) CerDIP	
25	70	CY7C168A-25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C168A-25VC	V5	20-Lead Molded SOJ	
		80	CY7C168A-25DMB	D6	20-Lead (300-Mil) CerDIP
35	70	CY7C168A-35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C168A-35VC	V5	20-Lead Molded SOJ	
		CY7C168A-35DMB	D6	20-Lead (300-Mil) CerDIP	
45	70	CY7C168A-45DMB	D6	20-Lead (300-Mil) CerDIP	Military

Speed (ns)	I _{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	115	CY7C169A-15PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C169A-15VC	V5	20-Lead Molded SOJ	
20	90	CY7C169A-20PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C169A-20VC	V5	20-Lead Molded SOJ	
25	70	CY7C169A-25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C169A-25VC	V5	20-Lead Molded SOJ	
35	70	CY7C169A-35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C169A-35VC	V5	20-Lead Molded SOJ	

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1} ^[15]	1, 2, 3
I _{SB2} ^[15]	1, 2, 3

Note:

15. CY7C168A only.

Document #: 38-00095-D

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{RCS}	7, 8, 9, 10, 11
t _{RCH}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 22 to Pin 21)	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-3.0V to +7.0V
Output Current into Outputs (LOW)	20 mA

Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Latch-up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military ^[1]	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[2]

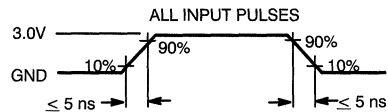
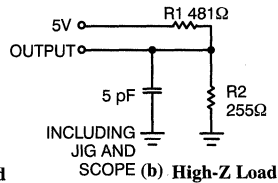
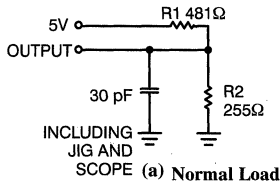
Parameter	Description	Test Conditions	7C170A-15		7C170A-20, 25, 35, 45		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage		-3.0	0.8	-3.0	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com ¹	115		90	mA
			Mil			120	mA

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

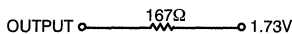
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

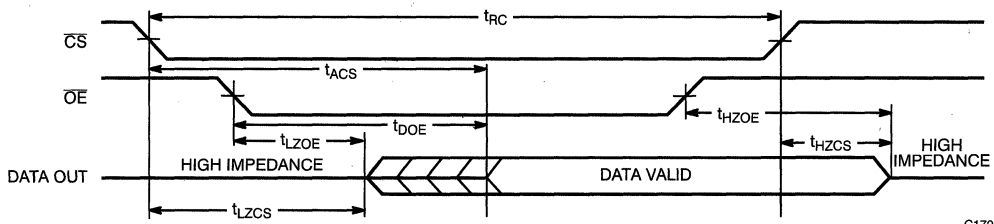
AC Test Loads and Waveforms


C170A-5

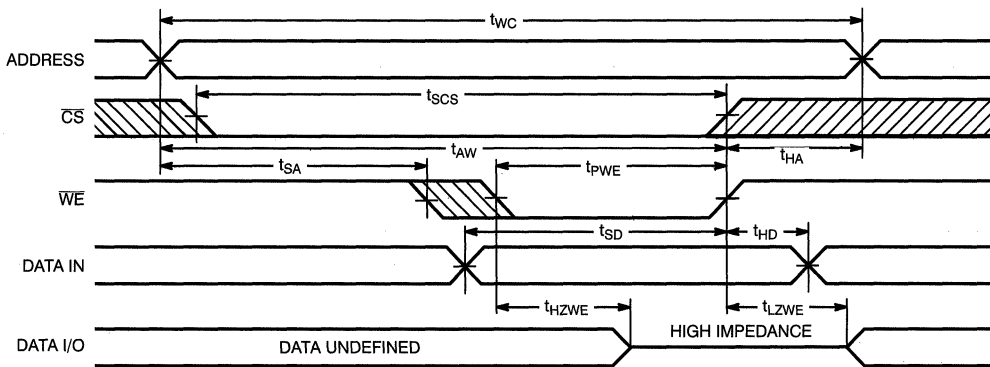
C170A-4

Equivalent to: THÉVENIN EQUIVALENT

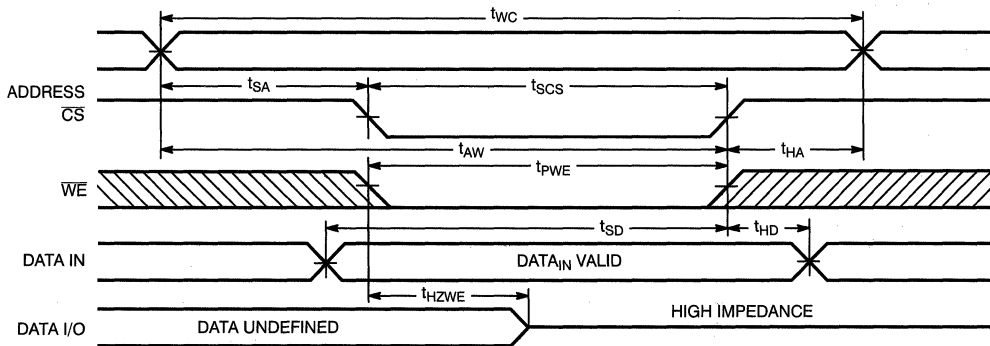


Switching Waveforms (continued)
Read Cycle No. 2^[9, 11]


C170A-7

Write Cycle No. 1^[8, 12]


C170A-8

Write Cycle No. 2^[8, 12, 13]


C170A-9

Notes:

 11. Data I/O will be high-impedance if $\overline{OE} = V_{IH}$.

 12. Address valid prior to or coincident with \overline{CS} transition LOW.

 13. If \overline{CS} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.



CY7C171A CY7C172A

4K x 4 Static RAM with Separate I/O

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
— $t_{AA} = 15$ ns
- Transparent write (CY7C171A)
- Low active power
— 375 mW
- Low standby power
— 93 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C171A and CY7C172A are high-performance CMOS static RAMs organized as 4096 by 4 bits with separate I/O. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 77% when deselected.

Writing to the device is accomplished when the chip enable (CE) and write enable (WE) inputs are both LOW. Data on the four input/output pins (I_0 through I_3) is

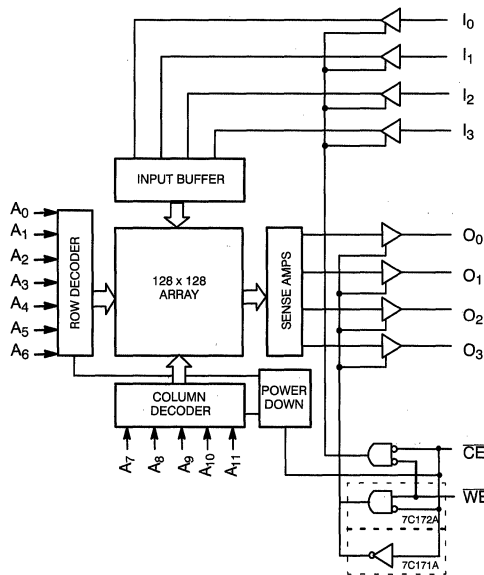
written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking chip enable (\overline{CE}) LOW, while write enable (WE) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

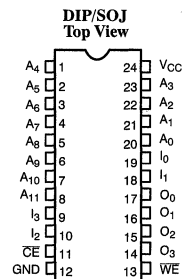
The output pins remain in a high-impedance state when write enable (WE) is LOW (7C172A only), or chip enable is HIGH.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configurations



C171A-2

Selection Guide

	7C171A-15 7C172A-15	7C171A-20 7C172A-20	7C171A-25 7C172A-25	7C171A-35 7C172A-35	7C171A-45 7C172A-45
Maximum Access Time (ns)	15	20	25	35	45
Maximum Operating Current (mA)	Commercial	115	80	70	70
	Military		90	80	70

Electrical Characteristics Over the Operating Range^[2] (continued)

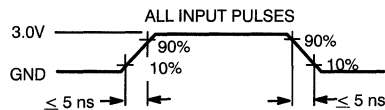
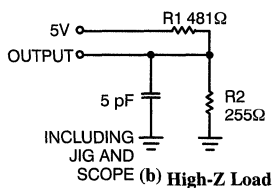
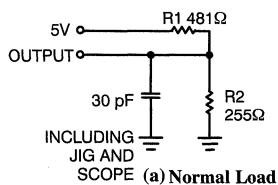
Parameter	Description	Test Conditions	7C171A-35 7C172A-35		7C171A-45 7C172A-45		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage		-3.0	0.8	-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max. I _{OUT} = 0 mA	Com ¹	70			mA
			Mil	70		70	mA
I _{SB1}	Automatic \overline{CE} Power-Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH}$ Min. Duty Cycle = 100%	Com ¹	20			mA
			Mil	20		20	mA
I _{SB2}	Automatic \overline{CE} Power-Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V	Com ¹	20			mA
			Mil	20		20	mA

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

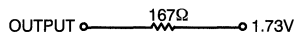
- See the last page of this specification for Group A subgroup testing information.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters

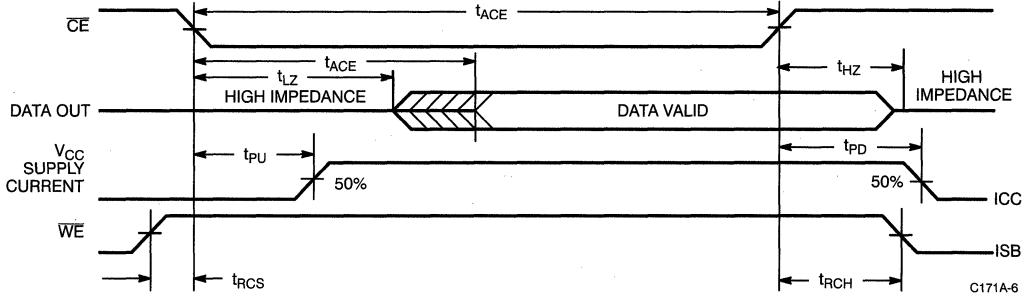
AC Test Loads and Waveforms


C171A-4

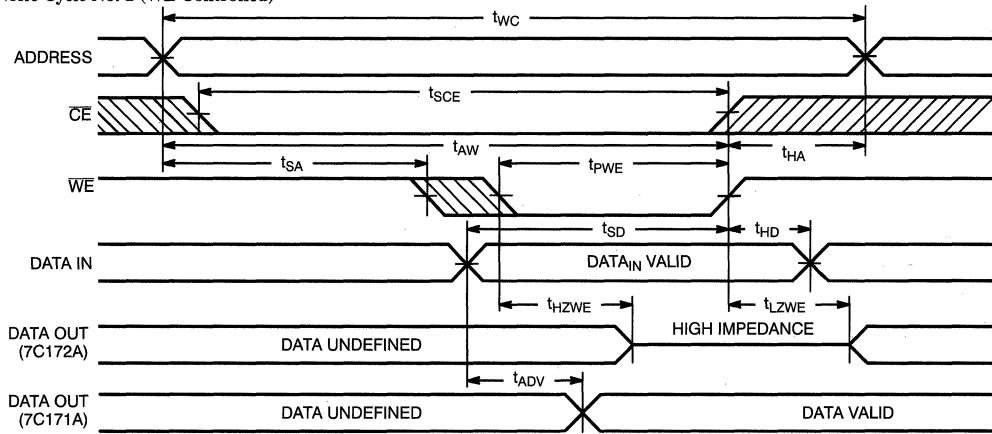
C171A-3

Equivalent to: THÉVENIN EQUIVALENT

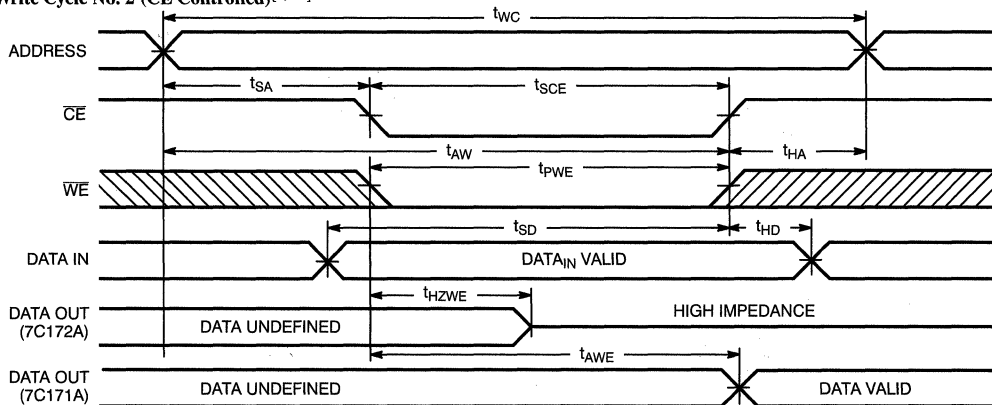


Switching Waveforms (continued)
Read Cycle No. 2^[9, 11]


C171A-6

Write Cycle No. 1 (WE Controlled)^[8]


C171A-7

Write Cycle No. 2 (CE Controlled)^[8, 12]


C171A-8

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C171A-15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
20	CY7C171A-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
25	CY7C171A-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
35	CY7C171A-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C172A-15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A-15VC	V13	24-Lead Molded SOJ	
20	CY7C172A-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A-20VC	V13	24-Lead Molded SOJ	
	CY7C172A-20DMB	D14	24-Lead (300-Mil) CerDIP	Military
25	CY7C172A-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A-25VC	V13	24-Lead Molded SOJ	
	CY7C172A-25DMB	D14	24-Lead (300-Mil) CerDIP	Military
35	CY7C172A-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A-35DMB	D14	24-Lead (300-Mil) CerDIP	Military
45	CY7C172A-45DMB	D14	24-Lead (300-Mil) CerDIP	Military



32K x 18 Synchronous Cache RAM

Features

- Supports 66-MHz Pentium™ micro-processor cache systems with zero wait states
- 32K by 18 common I/O
- Fast clock-to-output times
— 8.5 ns
- Two-bit wraparound counter supporting Pentium and 486 burst sequence (CY7C178)
- Two-bit wraparound counter supporting linear burst sequence (CY7C179)
- Separate processor and controller address strobes
- Synchronous self-timed write

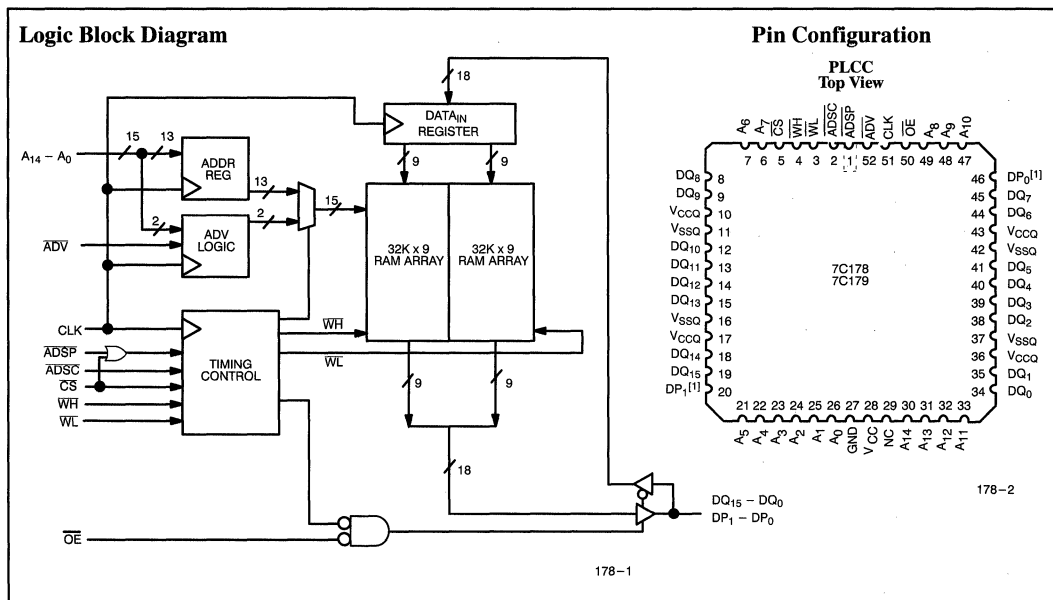
- Direct interface with the processor and external cache controller
- Asynchronous output enable
- I/Os capable of 3.3V operation
- Industry-standard pinout
- 52-pin PLCC and PQFP

Functional Description

The CY7C178 and CY7C179 are 32K by 18 synchronous cache RAMs designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 8.5 ns. A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

The CY7C178 is designed for Intel Pentium and i486 CPU-based systems; its counter follows the burst sequence of the Pentium and the i486 processors. The CY7C179 is architected for processors with linear burst sequences. Burst accesses can be initiated with the processor address strobe (ADSP) or the cache controller address strobe (ADSC) inputs. Address advancement is controlled by the address advancement (ADV) input.

A synchronous self-timed write mechanism is provided to simplify the write interface. A synchronous chip select input and an asynchronous output enable input provide easy control for bank selection and output three-state control.



Selector Guide

	7C178-8 7C179-8	7C178-10 7C179-10	7C178-12 7C179-12
Maximum Access Time (ns)	8.5	10.5	12.5
Maximum Operating Current (mA)	Commercial	225	180
	Military		270

Shaded area contains advanced information.

Note:

1. DP₀ and DP₁ are functionally equivalent to DQ_x.
Pentium is a trademark of Intel Corporation.

Pin Definitions

Signal Name	Type	# of Pins	Description
V _{CC}	Input	1	+5V Power
V _{CCQ}	Input	4	+5V or 3.3V (Outputs)
GND	Input	1	Ground
V _{SSQ}	Input	4	Ground (Outputs)
CLK	Input	1	Clock
A ₁₄ – A ₀	Input	15	Address
ADSP	Input	1	Address Strobe from Processor
ADSC	Input	1	Address Strobe from Cache Controller
WH	Input	1	Write Enable – High Byte
WL	Input	1	Write Enable – Low Byte
ADV	Input	1	Advance
OE	Input	1	Output Enable
CS	Input	1	Chip Select
DQ ₁₅ –DQ ₀	Input/Output	16	Regular Data
DP ₁ –DP ₀	Input/Output	2	Parity Data

Pin Descriptions

Signal Name	I/O	Description
Input Signals		
CLK	I	Clock signal. It is used to capture the address, the data to be written, and the following control signals: ADSP, ADSC, CS, WH, WL, and ADV. It is also used to advance the on-chip auto-address-increment logic (when the appropriate control signals have been set).
A ₁₄ –A ₀	I	Fifteen address lines used to select one of 32K locations. They are captured in an on-chip register on the rising edge of CLK if ADSP or ADSC is LOW. The rising edge of the clock also loads the lower two address lines, A ₁ – A ₀ , into the on-chip auto-address-increment logic if ADSP or ADSC is LOW.
ADSP	I	Address strobe from processor. This signal is sampled at the rising edge of CLK. When this input and/or ADSC is asserted, A ₀ – A ₁₄ will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. If both ADSP and ADSC are asserted at the rising edge of CLK, only ADSP will be recognized. The ADSP input should be connected to the ADS output of the processor. ADSP is ignored when CS is HIGH.
ADSC	I	Address strobe from cache controller. This signal is sampled at the rising edge of CLK. When this input and/or ADSP is asserted, A ₀ – A ₁₄ will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. The ADSC input should <i>not</i> be connected to the ADS output of the processor.

Signal Name	I/O	Description
WH	I	Write signal for the high-order half of the RAM array. This signal is sampled by the rising edge of CLK. If WH is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of DQ ₁₅ – DQ ₈ and DP ₁ from the on-chip data register into the selected RAM location. There is one exception to this. If ADSP, WH, and CS are asserted (LOW) at the rising edge of CLK, the write signal, WH, is ignored. Note that ADSP has no effect on WH if CS is HIGH.
WL	I	Write signal for the low-order half of the RAM array. This signal is sampled by the rising edge of CLK. If WL is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of DQ ₇ – DQ ₀ and DP ₀ from the on-chip data register into the selected RAM location. There is one exception to this. If ADSP, WL, and CS are asserted (LOW) at the rising edge of CLK, the write signal, WL, is ignored. Note that ADSP has no effect of WL if CS is HIGH.
ADV	I	Advance. This signal is sampled by the rising edge of CLK. When it is asserted, it automatically increments the 2-bit on-chip auto-address-increment counter. In the CY7C179, the address will be incremented linearly. In the CY7C178, the address will be incremented according to the Pentium/486 burst sequence. This signal is ignored if ADSP or ADSC is asserted concurrently with CS. Note that ADSP has no effect on ADV if CS is HIGH.
CS	I	Chip select. This signal is sampled by the rising edge of CLK. If CS is HIGH and ADSC is LOW, the SRAM is deselected. If CS is LOW and ADSC or ADSP is LOW, a new address is captured by the address register. If CS is HIGH, ADSP is ignored.

Electrical Characteristics Over the Operating Range (continued)^[4]

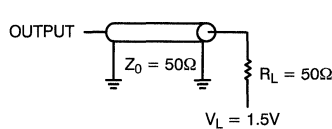
Parameter	Description	Test Conditions	7C178-8 7C179-8		7C178-10 7C179-10		7C178-12 7C179-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{OS}	Output Short Circuit Current ^[5]	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}$		-300		-300		-300	mA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{out} = 0\text{mA}, f = f_{MAX} = 1/t_{TRC}$	Com'1	225		210		190	mA
			Mil					270	
I_{SB1}	Automatic CE Power-Down Current – TTL Inputs	Max. $V_{CC}, \overline{CS} \geq V_{IH}, V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$	Com'1	50		40		30	mA
			Mil					50	
I_{SB2}	Automatic CE Power-Down Current – CMOS Inputs	Max. $V_{CC}, \overline{CS} \geq V_{CC} - 0.3\text{V}, V_{IN} \geq V_{CC} - 0.3\text{V}$ or $V_{IN} \leq 0.3\text{V}, f = 0$ ^[6]	Com'1	20		20		20	mA
			Mil					20	

Shaded areas contain advanced information

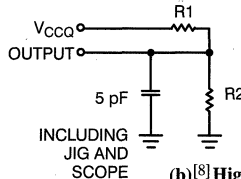
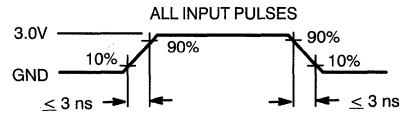
Capacitance^[7]

Parameter	Description	Test Conditions	Max.	Unit	
C_{IN} : Addresses	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1\text{MHz}, V_{CC} = 5.0\text{V}$	Com'1	4.5	pF
			Mil	6	
C_{IN} : Other Inputs			Com'1	5	pF
			Mil	8	
C_{OUT}	Output Capacitance		Com'1	8	pF
			Mil	10	

Shaded areas contain advanced information

AC Test Loads and Waveforms


(a) Normal Load

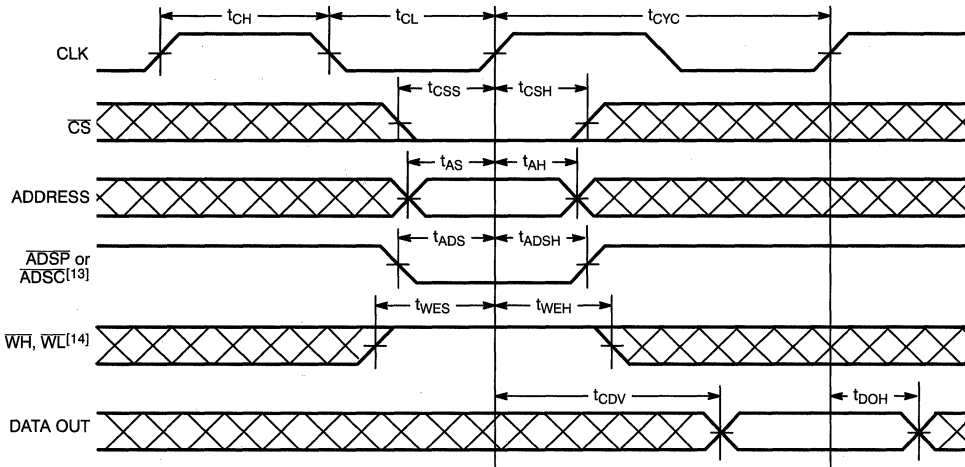

 (b)^[8] High-Z Load


178-3

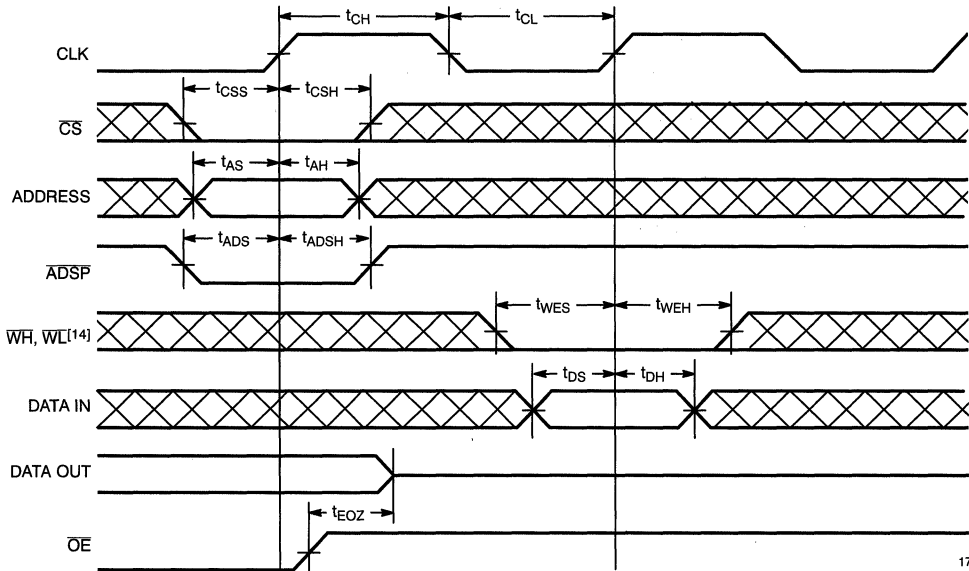
178-4

Notes:

- Not more than one output should be shortened at one time. Duration of the short circuit should not exceed 30 seconds.
- Inputs are disabled, clock signal allowed to run at speed.
- Tested initially and after any design or process changes that may affect these parameters.
- Resistor values for $V_{CCQ} = 5\text{V}$ are $R1 = 481\Omega$ and $R2 = 255\Omega$. Resistor values for $V_{CCQ} = 3.3\text{V}$ are $R1 = 1179\Omega$ and $R2 = 868\Omega$.

Switching Waveforms
Single Read^[12]


178-5

Single Write Timing: Write Initiated by $\overline{\text{ADSP}}$


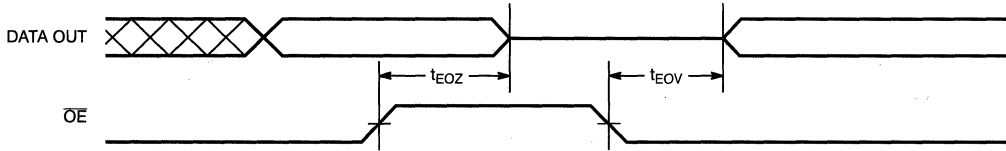
178-6

Notes:

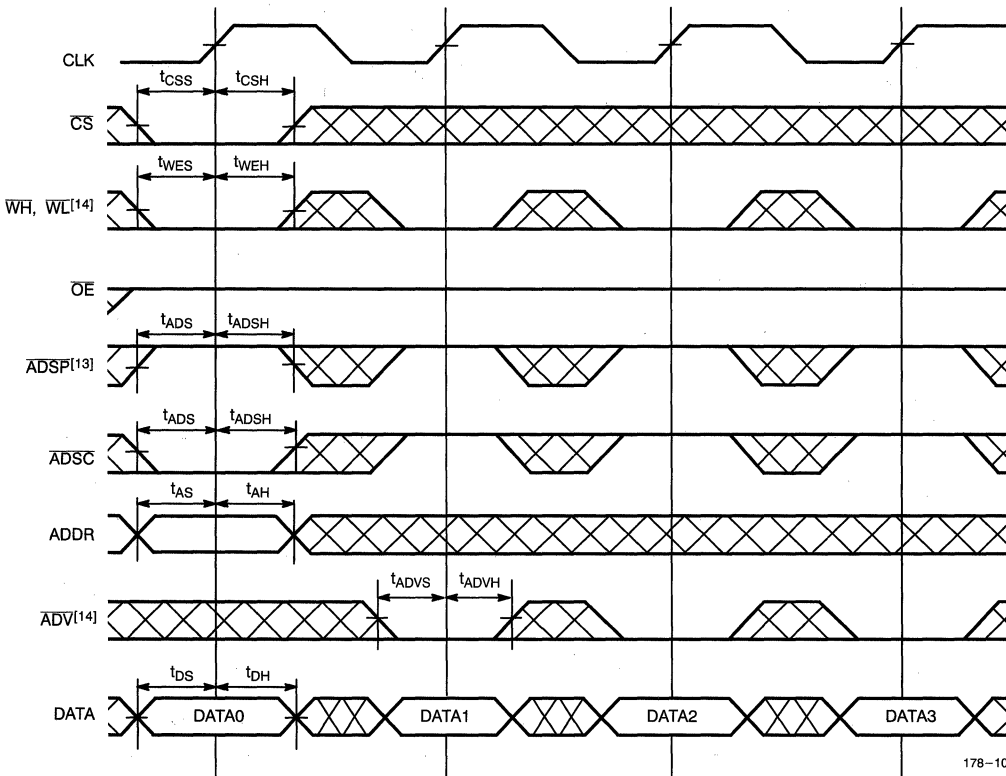
 12. $\overline{\text{OE}}$ is LOW throughout this operation.

 13. If $\overline{\text{ADSP}}$ is asserted while $\overline{\text{CS}}$ is HIGH, $\overline{\text{ADSP}}$ will be ignored.

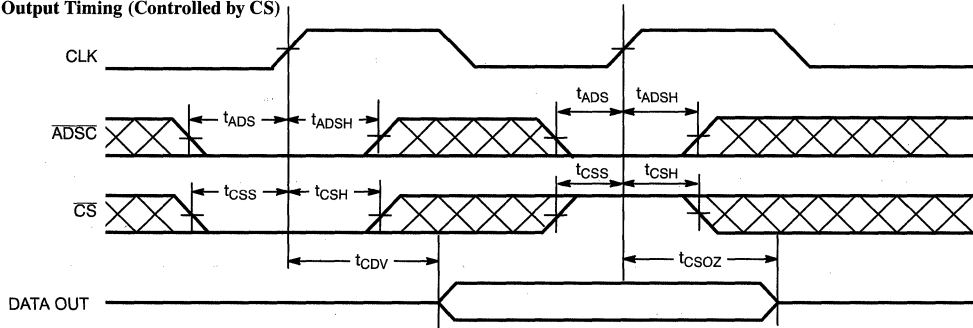
 14. $\overline{\text{ADSP}}$ has no effect on $\overline{\text{ADV}}$, $\overline{\text{WH}}$, and $\overline{\text{WL}}$ if $\overline{\text{CS}}$ is HIGH.

Switching Waveforms (continued)
Output (Controlled by \overline{OE})


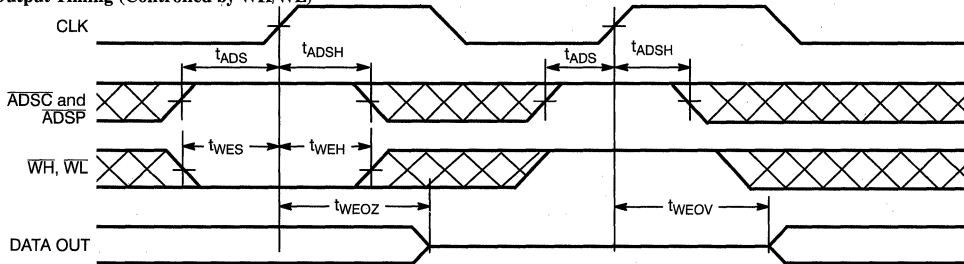
178-9

Write Burst Timing: Write Initiated by \overline{ADSC}


178-10

Switching Waveforms (continued)
Output Timing (Controlled by \overline{CS})


178-12

Output Timing (Controlled by $\overline{WH/WL}$)


178-13

Truth Table

Input						Address	Operation
\overline{CS}	\overline{ADSP}	\overline{ADSC}	\overline{ADV}	\overline{WH} or \overline{WL}	CLK		
H	L	H	H	H	L→H	Same address as previous cycle	\overline{ADSP} ignored, read cycle
H	L	H	L	H	L→H	Incremented burst address	\overline{ADSP} ignored, read cycle in burst sequence
H	L	H	H	L	L→H	Same address as previous cycle	\overline{ADSP} ignored, write cycle
H	L	H	L	L	L→H	Incremented burst address	\overline{ADSP} ignored, write cycle in burst sequence
H	X	L	X	X	L→H	N/A	Chip deselected
L	L	X	X	X	L→H	External	Read cycle, begin burst
L	H	L	X	H	L→H	External	Read cycle, begin burst
L	H	L	X	L	L→H	External	Write cycle, begin burst
X	H	H	L	L	L→H	Incremented burst address	Write cycle, in burst sequence
X	H	H	L	H	L→H	Incremented burst address	Read cycle, in burst sequence
X	H	H	H	L	L→H	Same address as previous cycle	Write cycle
X	H	H	H	H	L→H	Same address as previous cycle	Read cycle



8K x 9 Static RAM

Features

- High speed
— $t_{AA} = 25$ ns
- 9-bit organization is ideal for cache memory applications
- CMOS for optimum speed/power
- Low active power
— 770 mW
- Low standby power
— 195 mW
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- Easy memory expansion with \overline{CE}_1 , CE_2 , \overline{OE} options

Functional Description

The CY7C182 is a high-speed CMOS static RAM organized as 8,192 by 9 bits and it is manufactured using Cypress's high-performance CMOS technology. Access times as fast as 25 ns are available with maximum power consumption of only 770 mW.

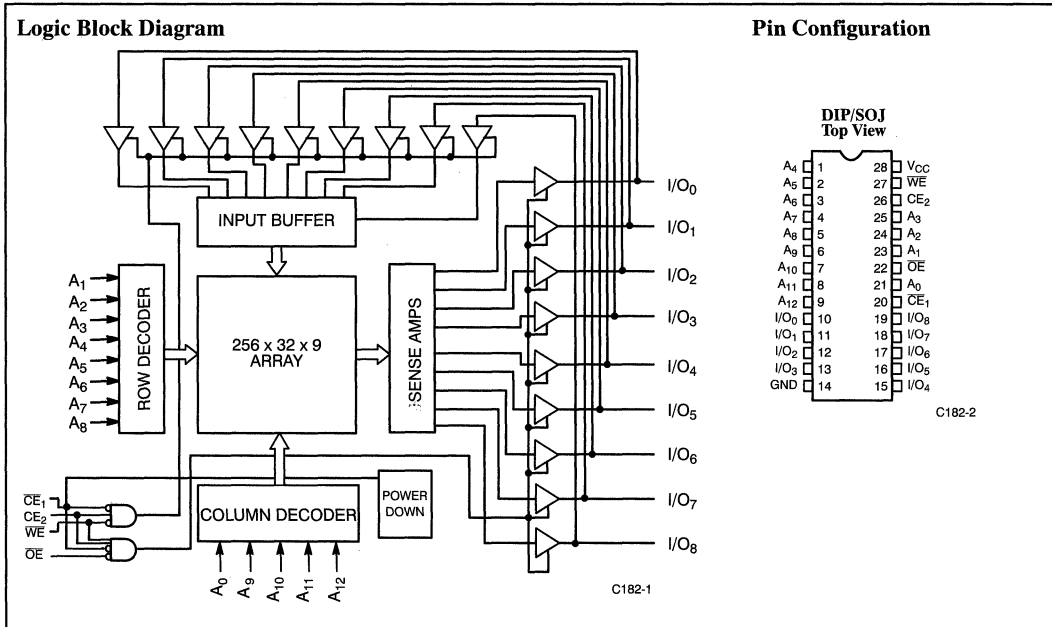
The CY7C182, which is oriented toward cache memory applications, features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by more than 70% when the circuit is deselected. Easy memory expansion is provided by an active-LOW chip enable (\overline{CE}_1), an active HIGH chip enable (CE_2), an active-LOW output enable (\overline{OE}), and three-state drivers.

An active-LOW write enable signal (\overline{WE}) controls the writing/reading operation of

the memory. When \overline{CE}_1 and \overline{WE} inputs are both LOW, data on the nine data input/output pins (I/O_0 through I/O_8) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, (\overline{CE}_1 and \overline{OE} active LOW and CE_2 active HIGH), while (\overline{WE}) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the nine data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH.

A die coat is used to ensure alpha immunity.



Selection Guide

	7C182-20	7C182-25	7C182-35	7C182-45
Maximum Access Time (ns)	20	25	35	45
Maximum Operating Current (mA) Com'l	150	140	140	140
Maximum Standby Current (mA)	35	35	35	35

Shaded area contains preliminary information.

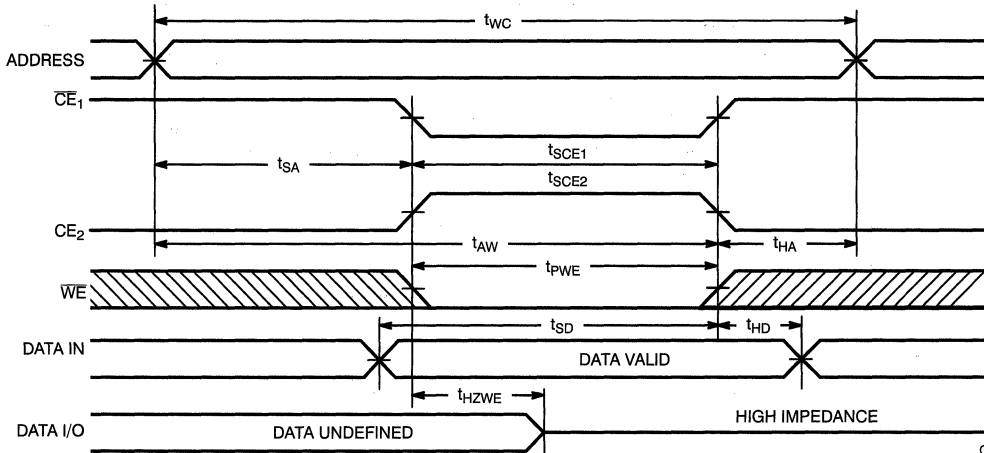
Switching Characteristics Over the Operating Range

Parameter	Description	7C182-20		7C182-25		7C182-35		7C182-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE^[4]										
t _{RC}	Read Cycle Time	20		25		35		45		ns
t _{AA}	Address to Data Valid		20		25		35		45	ns
t _{OHA}	Data Hold from Address Change	3		3		3		3		ns
t _{ACE1}	\overline{CE}_1 Access Time		20		25		35		45	ns
t _{ACE2}	CE ₂ Access Time		20		25		35		45	ns
t _{LZCE1}	\overline{CE}_1 LOW to Low Z	5		5		5		5		ns
t _{LZCE2}	CE ₂ HIGH to Low Z	5		5		5		5		ns
t _{HZCE1}	\overline{CE}_1 HIGH to High Z ^[5]		15		18		20		25	ns
t _{HZCE2}	CE ₂ LOW to High Z ^[5]		15		18		20		25	ns
t _{PU}	\overline{CE}_1 LOW to Power-Up	0		0		0		0		ns
t _{PD}	\overline{CE}_1 HIGH to Power-Down		20		20		20		25	ns
t _{DOE}	\overline{OE} Access Time		15		18		20		20	ns
t _{LZOE}	\overline{OE} LOW to Low Z	3		3		3		3		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[5]		15		18		20		25	ns
WRITE CYCLE^[6]										
t _{WC}	Write Cycle Time	20		25		35		45		ns
t _{SA}	Address Set-Up Time	0		0		0		0		ns
t _{AW}	Address Valid to End of Write	15		20		30		40		ns
t _{SD}	Data Set-Up Time	10		15		20		25		ns
t _{SCE1}	\overline{CE}_1 LOW to Write End	15		20		30		40		ns
t _{SCE2}	CE ₂ HIGH to Write End	15		20		30		40		ns
t _{PWE}	\overline{WE} Pulse Width	15		20		25		30		ns
t _{HA}	Address Hold from End of Write	0		0		0		0		ns
t _{HD}	Data Hold Time	0		0		0		0		ns
t _{LZWE}	Write HIGH to Low Z ^[7]	3		3		3		3		ns
t _{HZWE}	Write LOW to High Z ^[5, 7, 8]		13		13		15		20	ns

Shaded area contains preliminary information.

Notes:

- WE is HIGH for read cycle.
- t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, CE₂ HIGH, and WE LOW. All three signals must be asserted to initiate a write and any signal can terminate a write by being deasserted. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- At any given temperature and voltage condition, t_{LZWE} is less than t_{HZWE} for any given device. These parameters are sampled and not 100% tested.
- Address valid prior to or coincident with \overline{CE} transition LOW and CE₂ transition HIGH.

Switching Waveforms (continued)
Write Cycle No. 2 (CE Controlled)^[6, 10]


C182-8

Truth Table

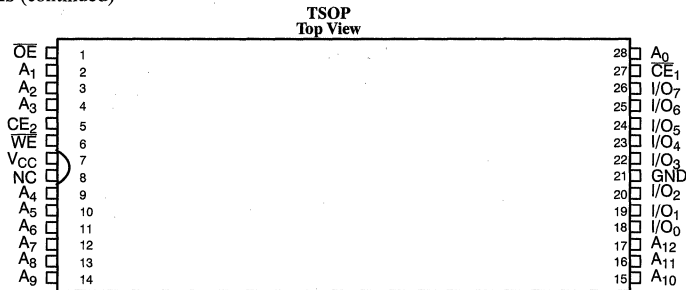
CE ₁	CE ₂	OE	WE	Data In	Data Out	Mode
H	X	X	X	Z	Z	Deselect/Power-Down
L	H	L	H	Z	Valid	Read
L	H	X	L	Valid	Z	Write
L	H	H	H	Z	Z	Output Disable
X	L	X	X	Z	Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C182-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C182-20VC	V21	28-Lead Molded SOJ	
25	CY7C182-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C182-25VC	V21	28-Lead Molded SOJ	
35	CY7C182-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C182-35VC	V21	28-Lead Molded SOJ	
45	CY7C182-45PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C182-45VC	V21	28-Lead Molded SOJ	

Shaded area contains preliminary information.

Document #: 38-00110-E

Pin Configurations (continued)


C185-3

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ^[2]	-0.5V to +7.0V
DC Input Voltage ^[2]	-0.5V to +7.0V

Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C185-12		7C185-15		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[2]		-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	µA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	µA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		140		130	mA
I _{SB1}	Automatic \overline{CE}_1 Power-Down Current	Max. V _{CC} , $\overline{CE}_1 \geq V_{IH}$, Min. Duty Cycle = 100%		40		40	mA
I _{SB2}	Automatic \overline{CE}_1 Power-Down Current	Max. V _{CC} , $\overline{CE}_1 \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		15		15	mA

Shaded areas contain preliminary information.

Notes:

- Minimum voltage is equal to -3.0V for pulse durations less than 30 ns.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

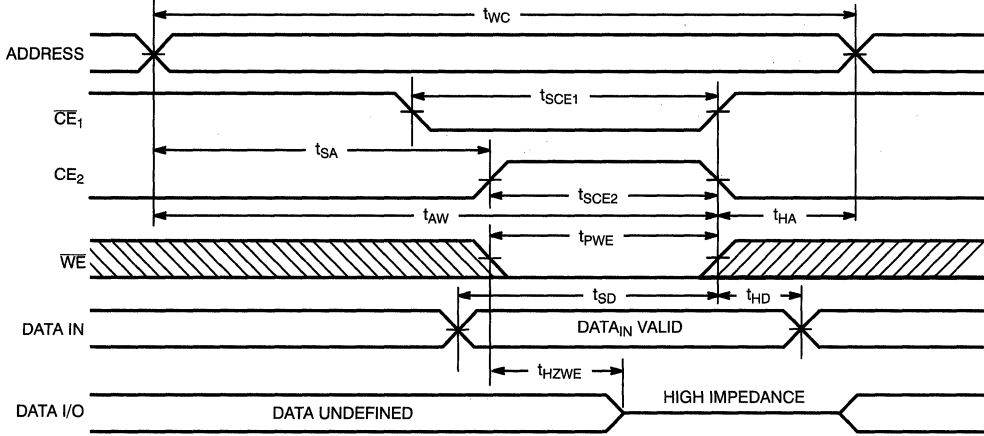
Switching Characteristics Over the Operating Range^[5]

Parameter	Description	7C185-12		7C185-15		7C185-20		7C185-25		7C185-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	12		15		20		25		35		ns
t _{AA}	Address to Data Valid		12		15		20		25		35	ns
t _{OHA}	Data Hold from Address Change	3		3		5		5		5		ns
t _{ACE1}	\overline{CE}_1 LOW to Data Valid		12		15		20		25		35	ns
t _{ACE2}	CE ₂ HIGH to Data Valid		12		15		20		25		35	ns
t _{DOE}	\overline{OE} LOW to Data Valid		6		8		9		12		15	ns
t _{LZOE}	\overline{OE} LOW to Low Z	2		3		3		3		3		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[6]		6		7		8		10		10	ns
t _{LZCE1}	\overline{CE}_1 LOW to Low Z ^[7]	3		3		5		5		5		ns
t _{LZCE2}	CE ₂ HIGH to Low Z	3		3		3		3		3		ns
t _{HZCE}	\overline{CE}_1 HIGH to High Z ^[6,7] CE ₂ LOW to High Z		6		7		8		10		10	ns
t _{PU}	\overline{CE}_1 LOW to Power-Up	0		0		0		0		0		ns
t _{PD}	\overline{CE}_1 HIGH to Power-Down		12		15		20		20		20	ns
WRITE CYCLE^[8]												
t _{WC}	Write Cycle Time	12		15		20		25		35		ns
t _{SCE1}	\overline{CE}_1 LOW to Write End	8		12		15		20		20		ns
t _{SCE2}	CE ₂ HIGH to Write End	8		12		15		20		20		ns
t _{AW}	Address Set-Up to Write End	9		12		15		20		25		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	8		12		15		15		20		ns
t _{SD}	Data Set-Up to Write End	6		8		10		10		12		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[6]		6		7		7		7		8	ns
t _{LZWE}	\overline{WE} HIGH to Low Z	3		3		5		5		5		ns

Shaded areas contain preliminary information.

Notes:

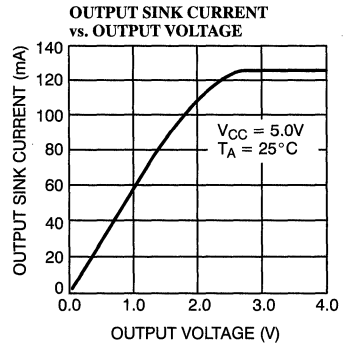
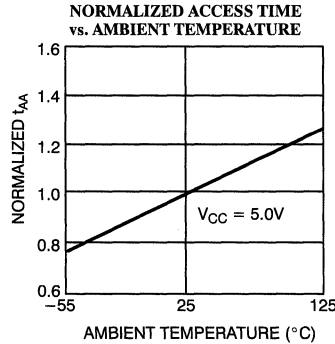
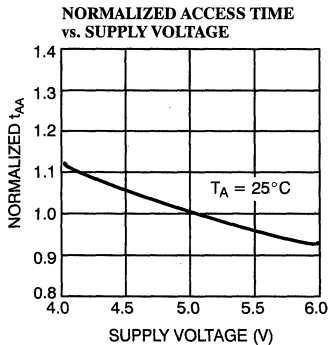
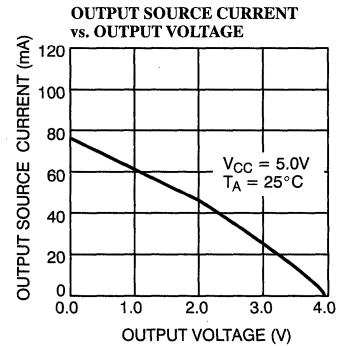
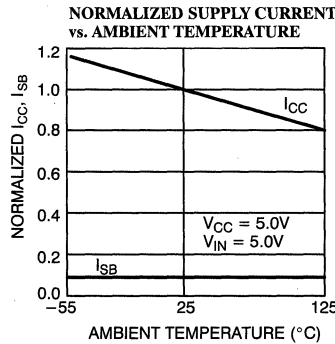
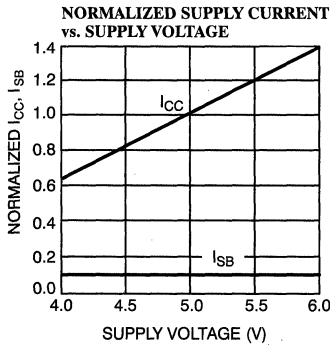
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, CE₂ HIGH, and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms (continued)
Write Cycle No. 2 (CE Controlled) [10, 12, 13]


C185-9

Note:

13. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics


Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C185-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185-12VC	V21	28-Lead Molded SOJ	
15	CY7C185-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185-15VC	V21	28-Lead Molded SOJ	
	CY7C185-15ZC	Z28	28-Lead Thin Small Outline Package	
20	CY7C185-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185-20VC	V21	28-Lead Molded SOJ	
	CY7C185-20ZC	Z28	28-Lead Thin Small Outline Package	
25	CY7C185-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185-25VC	V21	28-Lead Molded SOJ	
	CY7C185-25ZC	Z28	28-Lead Thin Small Outline Package	
35	CY7C185-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185-35VC	V21	28-Lead Molded SOJ	
	CY7C185-35ZC	Z28	28-Lead Thin Small Outline Package	

Shaded areas contain preliminary information.

Document #: 38-00037-J

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 28 to Pin 14)	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ^[2]	-0.5V to +7.0V
DC Input Voltage ^[2]	-0.5V to +7.0V

Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Military ^[3]	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[4]

Parameter	Description	Test Conditions	7C185A-15		7C185A-20		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[2]		-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND		-350		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max. I _{OUT} = 0 mA		170		135	mA
I _{SB1}	Automatic \overline{CE}_1 Power-Down Current	Max. V _{CC} , $\overline{CE}_1 \geq V_{IH}$, Min. Duty Cycle = 100%		40		40	mA
I _{SB2}	Automatic \overline{CE}_1 Power-Down Current	Max. V _{CC} , $\overline{CE}_1 \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≥ 0.3V		20		20	mA

Shaded area contains advanced information.

Notes:

- V_{IL} (min.) = -3.0V for pulse durations less than 30 ns.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

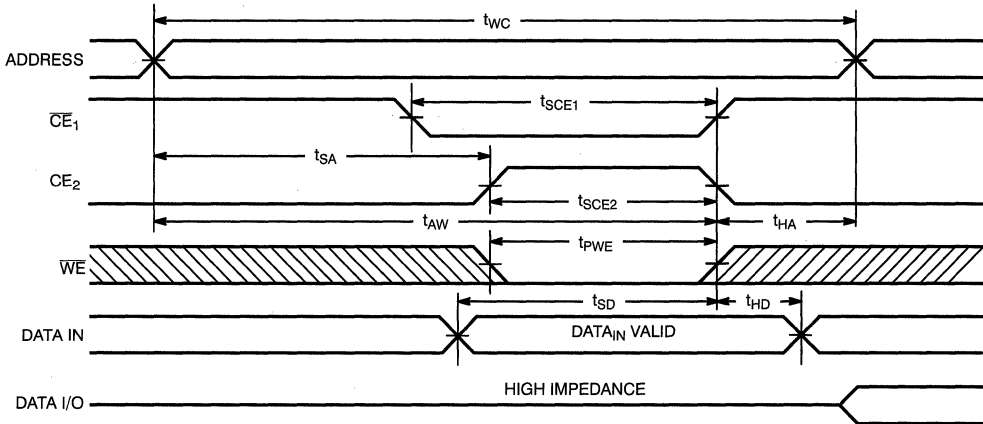
Switching Characteristics Over the Operating Range^[3, 7]

Parameter	Description	7C185A-15		7C185A-20		7C185A-25		7C185A-35		7C185A-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	15		20		25		35		45		ns
t _{AA}	Address to Data Valid		15		20		25		35		45	ns
t _{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t _{ACE1}	\overline{CE}_1 LOW to Data Valid		15		20		25		35		45	ns
t _{ACE2}	CE ₂ HIGH to Data Valid		15		20		25		35		30	ns
t _{DOE}	\overline{OE} LOW to Data Valid		7		10		12		15		20	ns
t _{LZOE}	\overline{OE} LOW to Low Z	0		3		3		3		3		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[8]		8		8		10		12		15	ns
t _{LZCE1}	\overline{CE}_1 LOW to Low Z ^[9]	3		5		5		5		5		ns
t _{LZCE2}	CE ₂ HIGH to Low Z	3		3		3		3		3		ns
t _{HZCE}	\overline{CE}_1 HIGH to High Z ^[8, 9] CE ₂ LOW to High Z		8		8		10		15		15	ns
t _{PU}	\overline{CE}_1 LOW to Power-Up	0		0		0		0		0		ns
t _{PD}	\overline{CE}_1 HIGH to Power-Down		15		20		20		20		25	ns
WRITE CYCLE^[10]												
t _{WC}	Write Cycle Time	15		20		20		25		40		ns
t _{SCE1}	\overline{CE}_1 LOW to Write End	10		15		20		25		30		ns
t _{SCE2}	CE ₂ HIGH to Write End	10		15		20		25		30		ns
t _{AW}	Address Set-Up to Write End	10		15		20		25		30		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t _{PWE}	WE Pulse Width	10		15		15		20		20		ns
t _{SD}	Data Set-Up to Write End	7		10		10		15		15		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{LZWE}	WE HIGH to Low Z	3		3		5		5		5		ns
t _{HZWE}	WE LOW to High Z ^[8]		7		7		7		10		15	ns

Shaded area contains advanced information.

Notes:

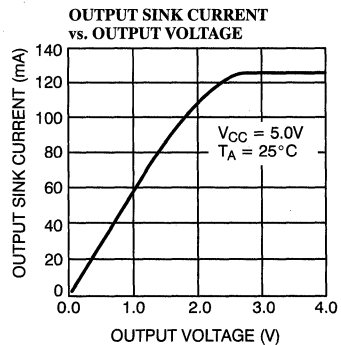
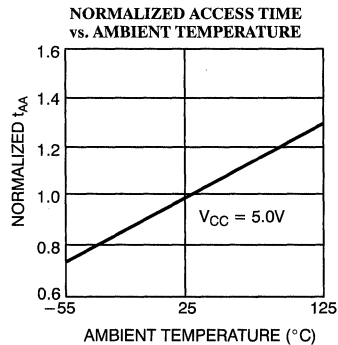
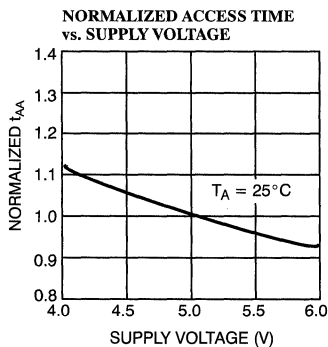
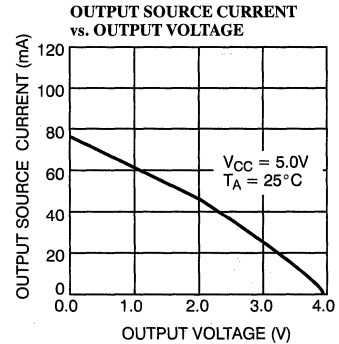
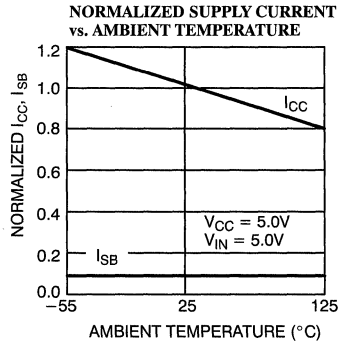
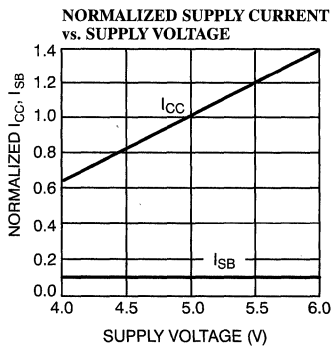
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
- Device is continuously selected. \overline{OE} , \overline{CE} = V_{IL}. CE₂ = V_{IH}.

Switching Waveforms (continued)
Write Cycle No. 2 (CE Controlled) [13, 14, 15]


C185A-9

Note:

15. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics


Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C185A-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C185A-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C185A-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A-25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C185A-35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A-35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C185A-45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A-45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{OS}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE1}	7, 8, 9, 10, 11
t _{ACE2}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE1}	7, 8, 9, 10, 11
t _{SCE2}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

Document #: 38-00114-B

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 22 to Pin 11)	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ^[2]	-0.5V to +7.0V
DC Input Voltage ^[2]	-0.5V to +7.0V

Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C187-12		7C187-15		7C187-20		7C187-25, 35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 12.0 mA		0.4		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[2]		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	-5	+5	-5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-350		-350		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		160		90		80		70	mA
I _{SB1}	Automatic \overline{CE} Power-Down Current ^[4]	Max. V _{CC} , $\overline{CE} \geq V_{IH}$		40		40		40		20	mA
I _{SB2}	Automatic \overline{CE} Power-Down Current	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20		20		20		20	mA

Shaded area indicates preliminary information.

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

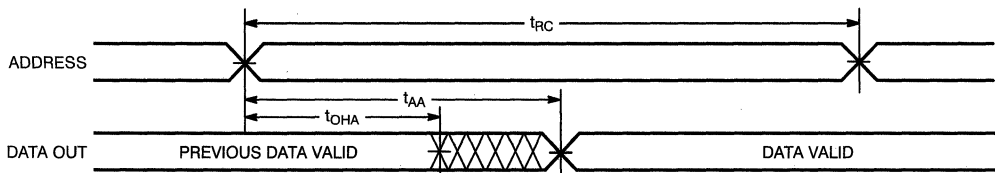
Notes:

- V_{IL} (min.) = -3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V_{CC} on the \overline{CE} input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

- Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range^[6] (continued)

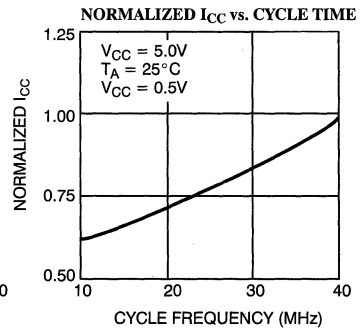
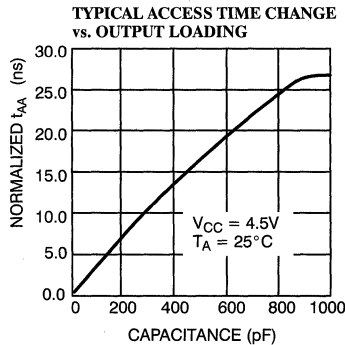
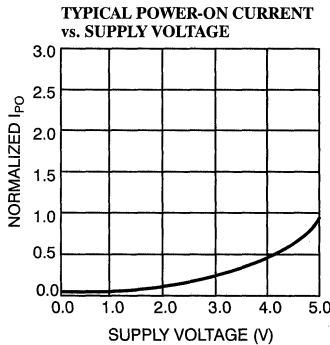
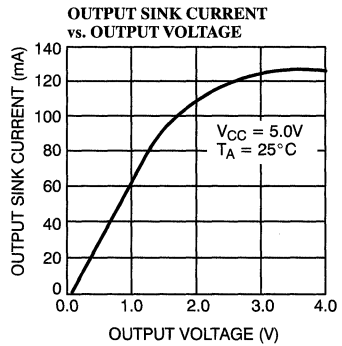
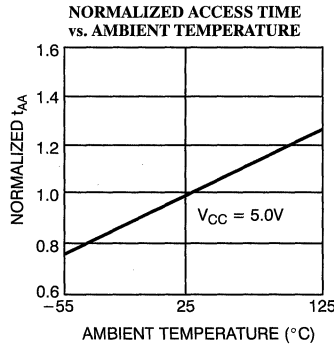
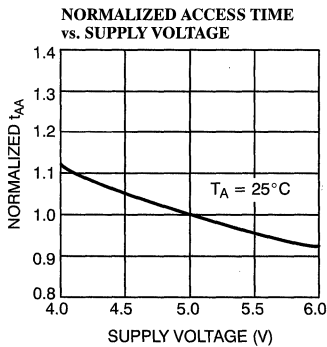
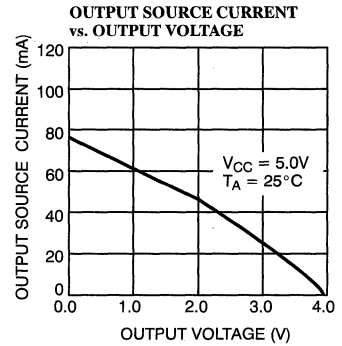
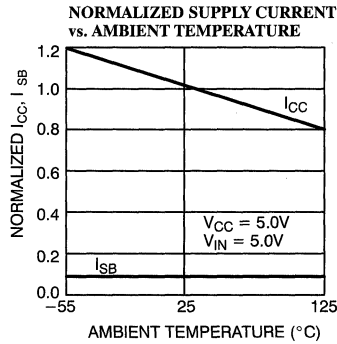
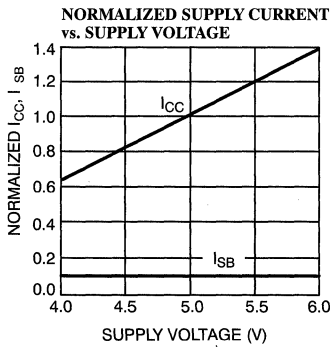
Parameters	Description	7C187-25		7C187-35		Units
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	25		35		ns
t_{AA}	Address to Data Valid		25		35	ns
t_{OHA}	Output Hold from Address Change	5		5		ns
t_{ACE}	\overline{CE} LOW to Data Valid		25		35	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[7]	5		5		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[8, 9]		10		15	ns
t_{PU}	\overline{CE} LOW to Power Up	0		0		ns
t_{PD}	\overline{CE} HIGH to Power Down		20		20	ns
WRITE CYCLE^[9]						
t_{WC}	Write Cycle Time	20		25		ns
t_{SCE}	\overline{CE} LOW to Write End	20		25		ns
t_{AW}	Address Set-Up to Write End	20		25		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	\overline{WE} Pulse Width	15		20		ns
t_{SD}	Data Set-Up to Write End	10		15		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low	5		5		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[10]		7		10	ns

Switching Waveforms
Read Cycle No. 1^[10, 11]


C187-6

Note:

 11. Device is continuously selected, $\overline{CE} = V_{IL}$.

Typical DC and AC Characteristics




64K x 1 Static RAM

Features

- High speed
— 20 ns
- CMOS for optimum speed/power
- Low active power
— 495 mW
- Low standby power
— 220 mW
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

Functional Description

The CY7C187A is a high-performance CMOS static RAM organized as 65,536 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}) and three-state drivers. The CY7C187A has an automatic power-down feature, reducing the power consumption by 55% when deselected.

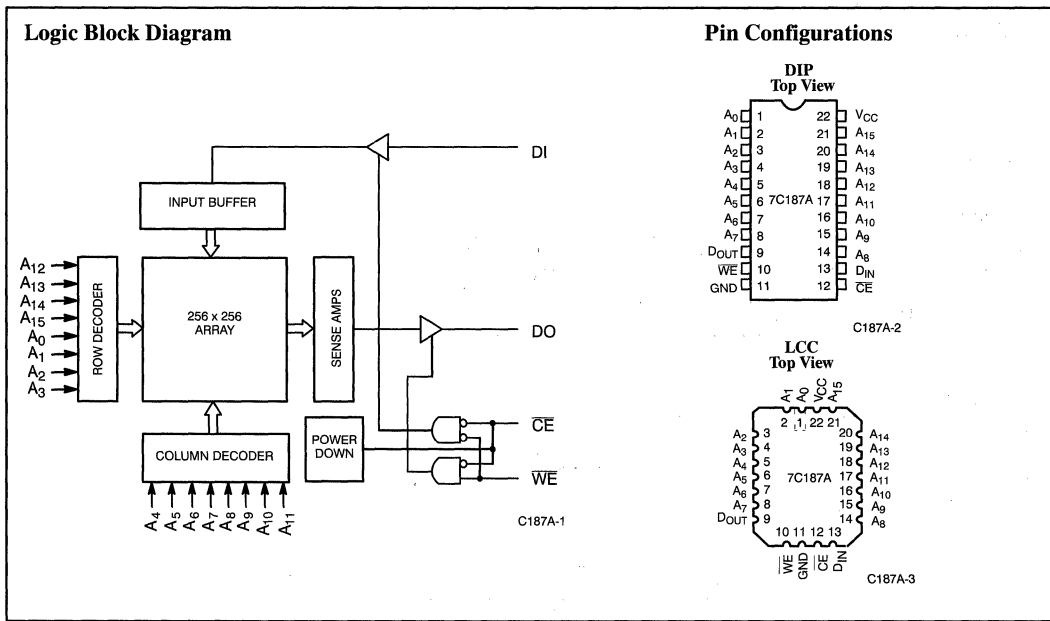
Writing to the device is accomplished when the chip enable (\overline{CE}) and write enable (\overline{WE}) inputs are both LOW. Data on the input pin (DI) is written into the memory

location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable (\overline{CE}) LOW, while write enable (\overline{WE}) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high-impedance state when chip enable (\overline{CE}) is HIGH or write enable (\overline{WE}) is LOW.

The CY7C187A utilizes a die coat to insure alpha immunity.



Selection Guide^[1]

		7C187A-15	7C187A-20	7C187A-25	7C187A-35
Maximum Access Time (ns)		15	20	25	35
Maximum Operating Current (mA)	Military	160	90	80	80
Maximum Standby Current (mA)	Military	40/20	40/20	40/20	30/20

Shaded area contains preliminary information.

Note:

1. For commercial specifications, see CY7C187 datasheet.

Electrical Characteristics Over the Operating Range^[4] (continued)

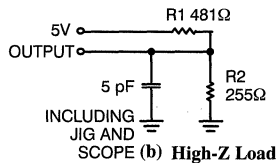
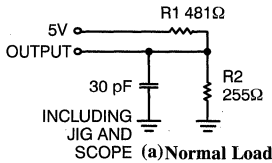
Parameter	Description	Test Conditions	7C187A-25		7C187A-35		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[2]		-3.0	0.8	-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		80		80	mA
I _{SB1}	Automatic \overline{CE} Power-Down Current ^[6]	Max. V _{CC} , $\overline{CE} \geq V_{IH}$		40		30	mA
I _{SB2}	Automatic \overline{CE} Power-Down Current ^[6]	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20		20	mA

Capacitance^[7]

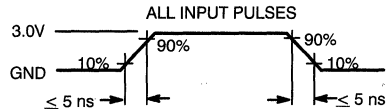
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Note:

7. Tested initially and after any design or process changes that may affect these parameters.

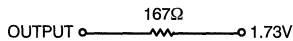
AC Test Loads and Waveforms


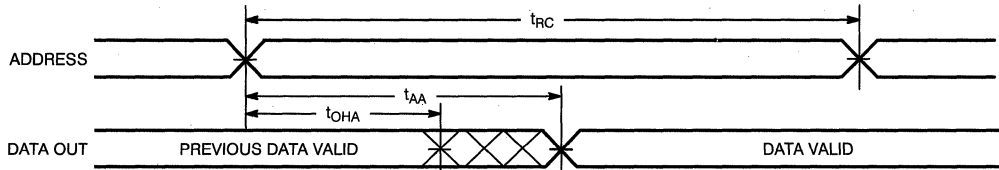
C187A-4



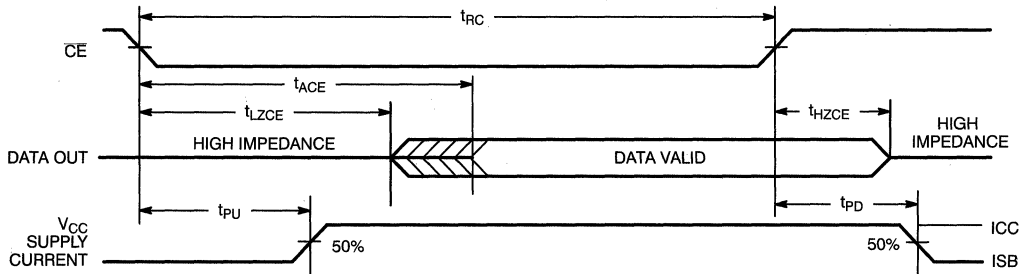
C187A-5

Equivalent to: THÉVENIN EQUIVALENT

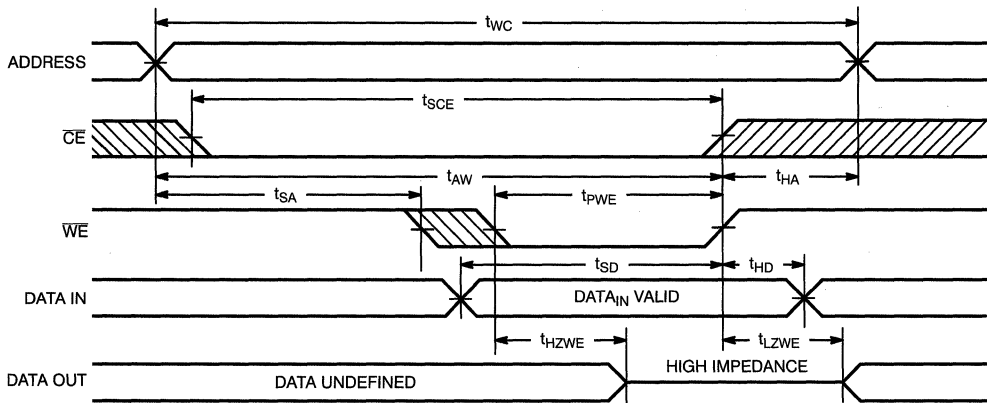


Switching Waveforms
Read Cycle No. 1^[12, 13]


C187A-6

Read Cycle No. 2^[12, 14]


C187A-7

Write Cycle No. 1 (\overline{WE} Controlled)^[11]


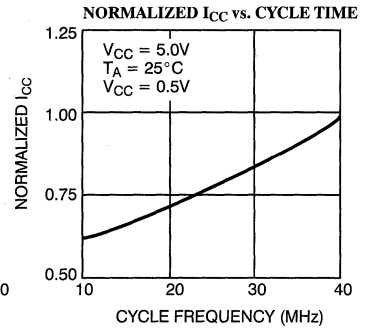
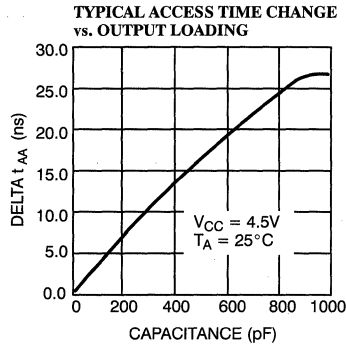
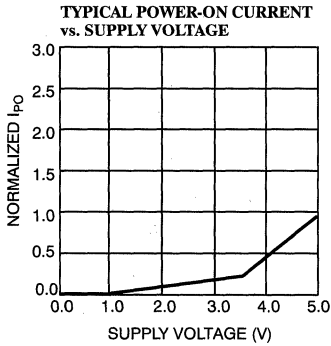
C187A-8

Notes:

 12. \overline{WE} is HIGH for read cycle.

 13. Device is continuously selected, $\overline{CE} = V_{IL}$.

 14. Address valid prior to or coincident with \overline{CE} transition LOW.

Typical DC and AC Characteristics (continued)

Address Designators

Address Name	Address Function	Pin Number
A0	X3	1
A1	X4	2
A2	X5	3
A3	X6	4
A4	X7	5
A5	Y7	6
A6	Y6	7
A7	Y2	8
A8	Y3	14
A9	Y1	15
A10	Y0	16
A11	Y4	17
A12	Y5	18
A13	X0	19
A14	X1	20
A15	X2	21

Truth Table

\overline{CE}	\overline{WE}	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

32K x 9 Static RAM
Features

- High speed
— 20 ns
- Automatic power-down when deselected
- Low active power
— 965 mW
- Low standby power
— 220 mW
- CMOS for optimum speed/power
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE}_1 , \overline{CE}_2 , and \overline{OE} features

Functional Description

The CY7C188 is a high-performance CMOS static RAM organized as 32,768 words by 9 bits. Easy memory expansion is provided by an active-LOW chip enable (\overline{CE}_1), an active-HIGH chip enable (\overline{CE}_2), an active-LOW output enable (\overline{OE}), and three-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

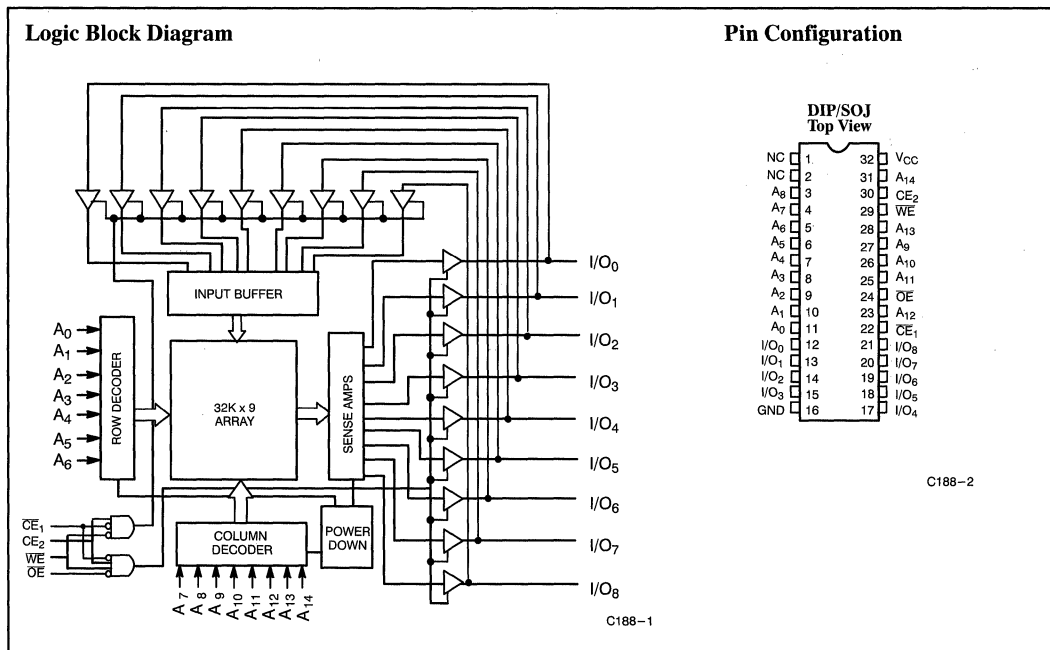
Writing to the device is accomplished by taking \overline{CE}_1 and write enable (\overline{WE}) inputs LOW and \overline{CE}_2 input HIGH. Data on the nine I/O pins ($I/O_0 - I/O_8$) is then written into the location specified on the address pins ($A_0 - A_{14}$).

Reading from the device is accomplished by taking \overline{CE}_1 and \overline{OE} LOW while forcing \overline{WE} and \overline{CE}_2 HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The nine input/output pins ($I/O_0 - I/O_8$) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH or \overline{CE}_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE}_1 LOW, \overline{CE}_2 HIGH, and \overline{WE} LOW).

The CY7C188 is available in standard 300-mil-wide DIPs and SOJs.

A die coat is used to ensure alpha immunity.


Selection Guide

		7C188-20	7C188-25	7C188-35
Maximum Access Time (ns)		20	25	35
Maximum Operating Current (mA)	Commercial	170	165	160
	Military		175	160
Maximum Standby Current (mA)		35	35	30

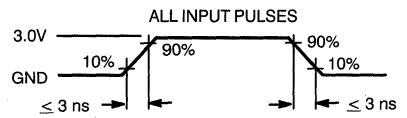
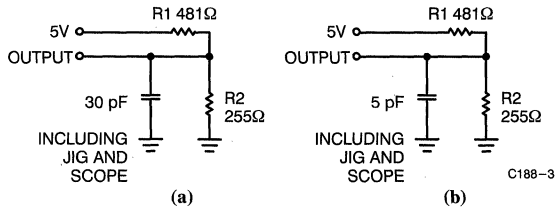
Shaded area contains preliminary information.

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN} : Addresses	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	6	pF
C _{IN} : Controls			8	pF
C _{OUT}			8	pF

Note:

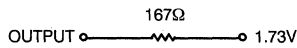
5. Tested initially and after any design or process changes that may affect these parameters.

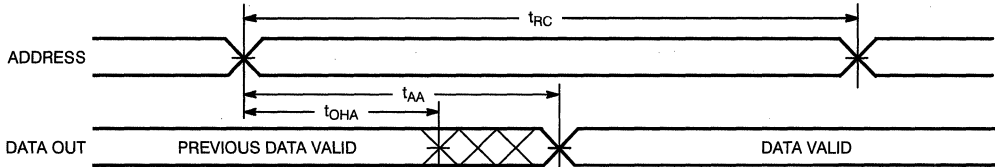
AC Test Loads and Waveforms^[6, 7]


C188-3

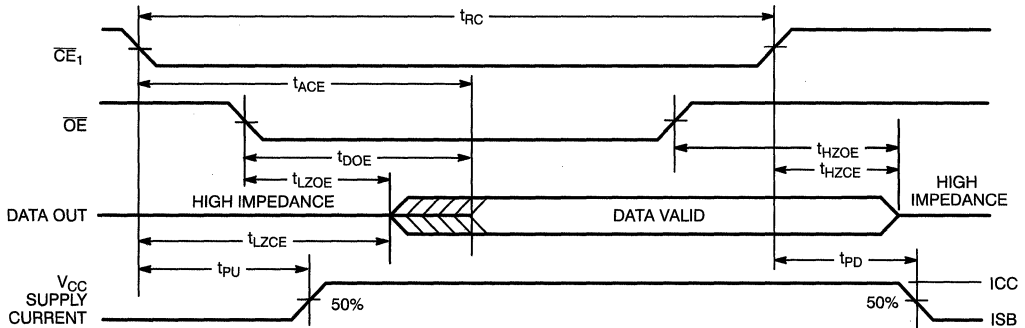
C188-4

Equivalent to: THÉVENIN EQUIVALENT

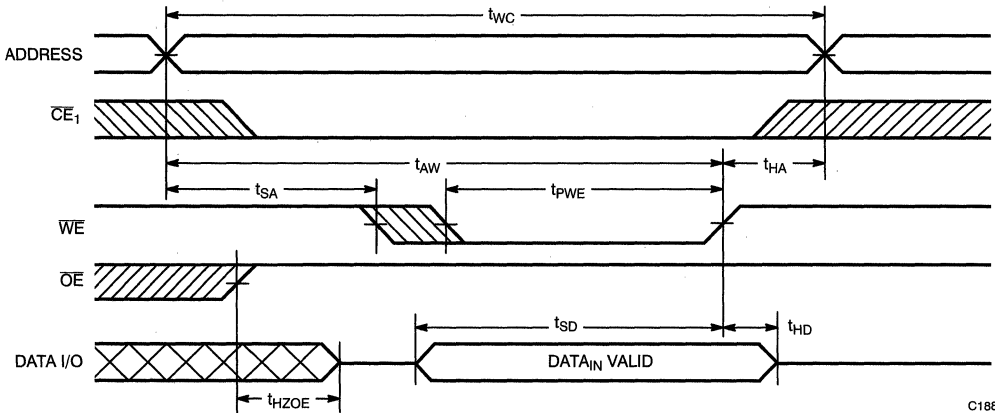


Switching Waveforms
Read Cycle No. 1^[11, 12]


C188-5

Read Cycle No. 2 (Chip-Enable Controlled)^[12, 13, 14]


C188-6

Write Cycle No. 1 (\overline{WE} Controlled)^[9, 14, 15, 16]


C188-7

Notes:

 11. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.

 12. \overline{WE} is HIGH for read cycle.

 13. Address valid prior to or coincident with \overline{CE} transition LOW.

 14. Timing parameters are the same for all chip enable signals (\overline{CE}_1 and \overline{CE}_2), so only the timing for \overline{CE}_1 is shown.

 15. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

 16. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Truth Table

CE	WE	OE	Input/Output	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C188-20PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C188-20VC	V32	32-Lead (300-Mil) Molded SOJ	
25	CY7C188-25PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C188-25VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C188-25DMB	D32	32-Lead (300-Mil) CerDIP	Military
35	CY7C188-35PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C188-35VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C188-35DMB	D32	32-Lead (300-Mil) CerDIP	Military

Shaded areas contain preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
$V_{IL Max.}$	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 28 to Pin 14)	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ^[1]	-0.5V to V _{CC} + 0.5V
DC Input Voltage ^[1]	-0.5V to V _{CC} + 0.5V
Output Current into Outputs (LOW)	20 mA

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military ^[2]	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	7C191-12 7C192-12		7C191-15 7C192-15		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3V	2.2	V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage ^[1]		-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com'l	155		145	mA
			Mil			160	
I _{SB1}	Automatic \overline{CE} Power-Down Current—TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		30		30	mA
I _{SB2}	Automatic \overline{CE} Power-Down Current—CMOS Inputs	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0	Com'l	10		10	mA
			Mil			15	

Shaded area contains preliminary information.

Notes:

- Minimum voltage is equal to -2.0V for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

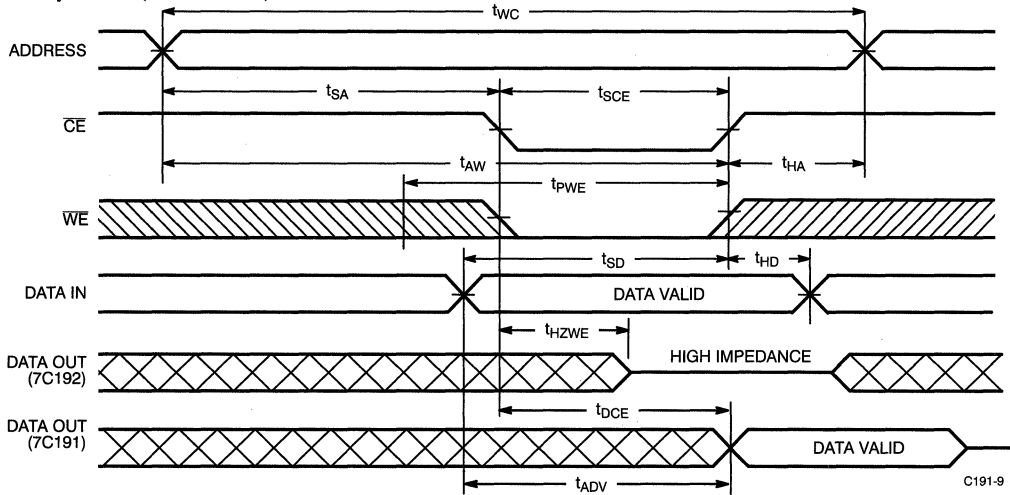
Switching Characteristics Over the Operating Range^[3,7]

Parameter	Description	7C191-12 7C192-12		7C191-15 7C192-15		7C191-20 7C192-20		7C191-25 7C192-25		7C191-35 7C192-35		7C192-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t _{RC}	Read Cycle Time	12		15		20		25		35		45		ns
t _{AA}	Address to Data Valid		12		15		20		25		35		45	ns
t _{OHA}	Output Hold from Address Change	3		3		3		3		3		3		ns
t _{ACE}	\overline{CE} LOW to Data Valid		12		15		20		25		35		45	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[8]	3		3		3		3		3		3		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[8,9]		5		7		9		11		15		15	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		12		15		20		25		35		45	ns
WRITE CYCLE^[10]														
t _{WC}	Write Cycle Time	12		15		20		25		35		45		ns
t _{SCE}	\overline{CE} LOW to Write End	9		10		15		18		22		22		ns
t _{AW}	Address Set-Up to Write End	9		10		15		20		25		35		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	8		9		15		18		22		22		ns
t _{SD}	Data Set-Up to Write End	8		9		10		10		15		15		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		0		ns
t _{LZWE}	\overline{WE} HIGH to Low Z (7C192) ^[8]	3		3		3		3		3		3		ns
t _{HZWE}	\overline{WE} LOW to High Z (7C192) ^[8,9]		7		7		10		11		15		15	ns
t _{DWE}	\overline{WE} LOW to Data Valid (7C191)		12		15		20		25		30		35	ns
t _{ADV}	Data Valid to Output Valid (7C191)		12		15		20		20		30		35	ns
t _{DCE}	\overline{CE} LOW to Data Valid (7C191)		12		15		20		25		35		45	ns

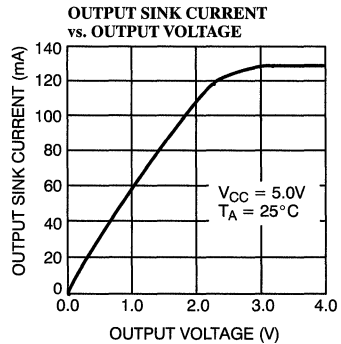
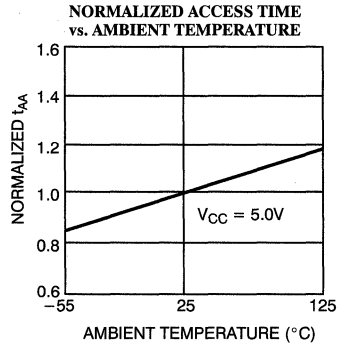
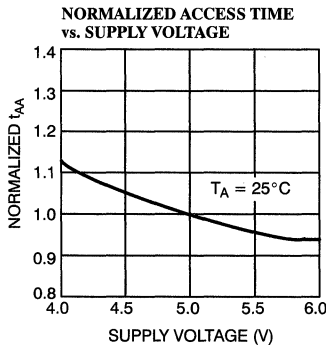
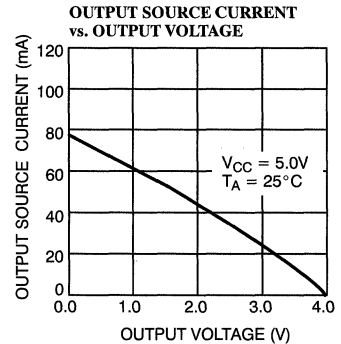
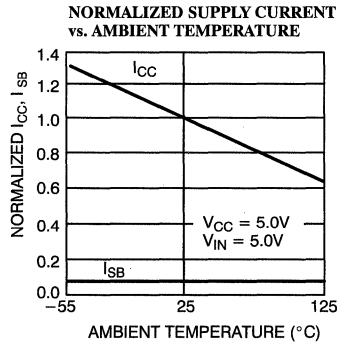
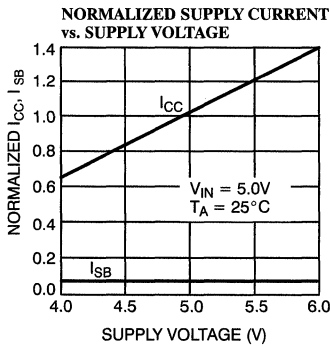
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Notes:

- Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 through -45 speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZWE} is less than t_{LZWE} for any given device. These parameters are guaranteed by design and not 100% tested.
- t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms (continued)
Write Cycle No. 2 (CE Controlled)^[10, 14]


C191-9

Typical DC and AC Characteristics


Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C192-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192-12VC	V21	28-Lead Molded SOJ	
15	CY7C192-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192-15VC	V21	28-Lead Molded SOJ	
	CY7C192-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7C192-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192-20VC	V21	28-Lead Molded SOJ	
	CY7C192-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
25	CY7C192-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192-25VC	V21	28-Lead Molded SOJ	
	CY7C192-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C192-25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C192-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192-35VC	V21	28-Lead Molded SOJ	
	CY7C192-35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C192-35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C192-45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C192-45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3

Document #: 38-00076-J

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11
t _{AWE} ^[15]	7, 8, 9, 10, 11
t _{ADV} ^[15]	7, 8, 9, 10, 11

Note:
15. CY7C191 only

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 28 to Pin 14)	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage	-0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V
Latch-Up Current	>200 mA

Operating Range

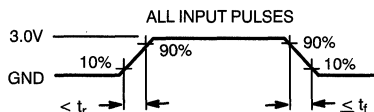
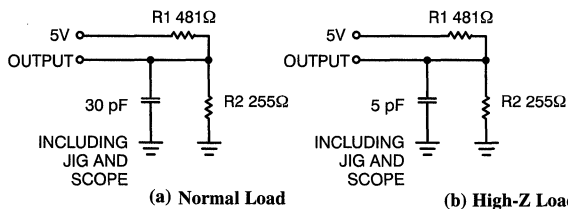
Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C193-20		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.3V$	V
V_{IL}	Input LOW Voltage		-0.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-5	+5	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-5	+5	μA
I_{OS}	Output Short Circuit Current ^[1]	$V_{CC} = \text{Max.}, V_{OUT} = GND$		-300	mA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$		160	mA

Capacitance^[2]

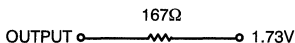
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 5.0V$	8	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms


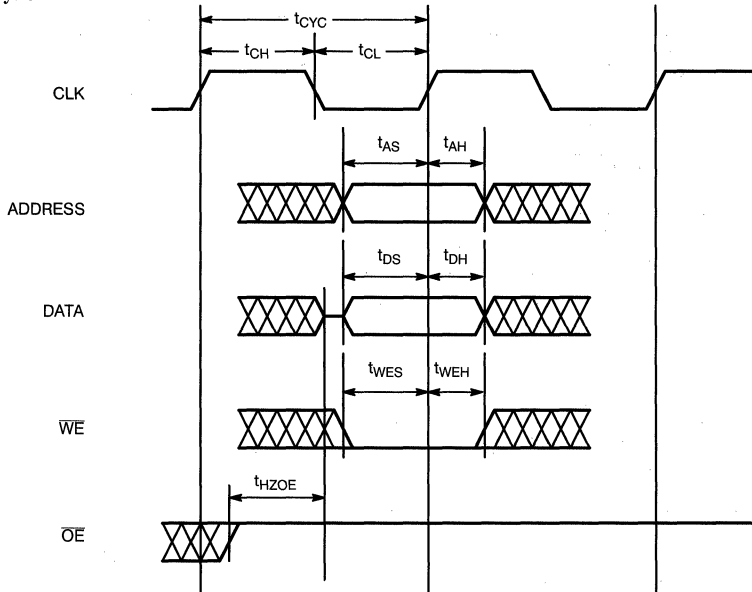
C193-3

C193-4

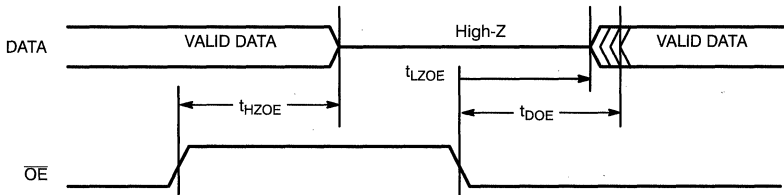
Equivalent to: THÉVENIN EQUIVALENT


Notes:

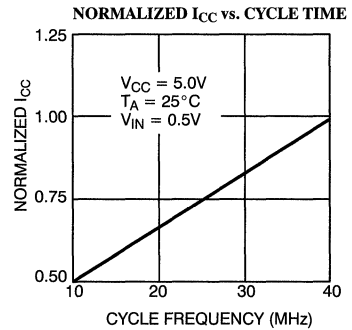
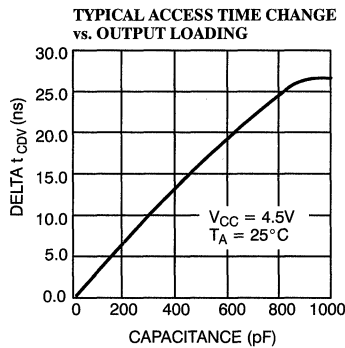
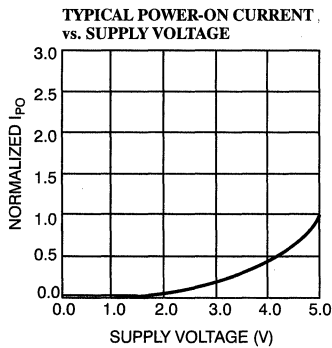
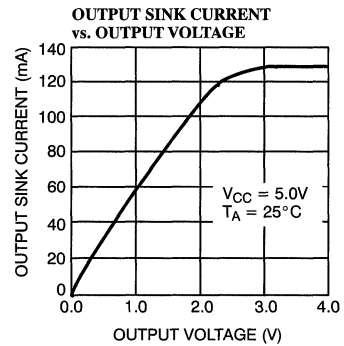
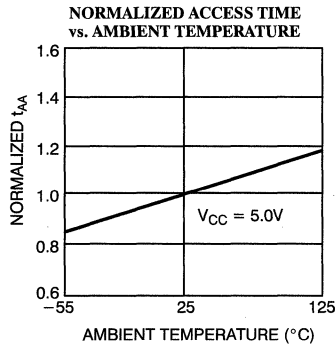
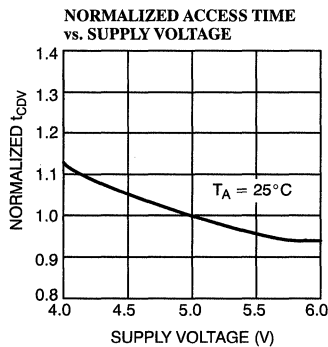
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

Switching Waveforms (continued)
Write Cycle


C193-6

 \overline{OE} Timing


C193-7

Typical DC and AC Characteristics (continued)

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C193-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C193-20VC	V21	28-Lead Molded SOJ	

Shaded area contains preliminary information.

Document #: 38-00254-A



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied -55°C to +125°C
 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Voltage Applied to Outputs in High Z State^[1] -0.5V to V_{CC} + 0.5V
 DC Input Voltage^[1] -0.5V to V_{CC} + 0.5V
 Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)
 Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military ^[2]	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	7C194-12 7C195-12 7C196-12		7C194-15 7C195-15 7C196-15		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3V	2.2	V _{CC} + 0.3V	V
V _{IL} ^[1]	Input LOW Voltage		-0.5	0.8	-0.5	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	µA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	µA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com'l	155		145	mA
			Mil			160	
I _{SB1}	Automatic \overline{CE} Power-Down Current —TTL Inputs ^[5]	Max. V _{CC} , $\overline{CE}_{1,2} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		30		30	mA
I _{SB2}	Automatic \overline{CE} Power-Down Current —CMOS Inputs ^[5]	Max. V _{CC} , $\overline{CE}_{1,2} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0	Com'l	10		10	mA
			Mil			15	

Shaded area contains preliminary information.

Notes:

- Minimum voltage is equal to -2.0V for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V_{CC} on the \overline{CE} input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.



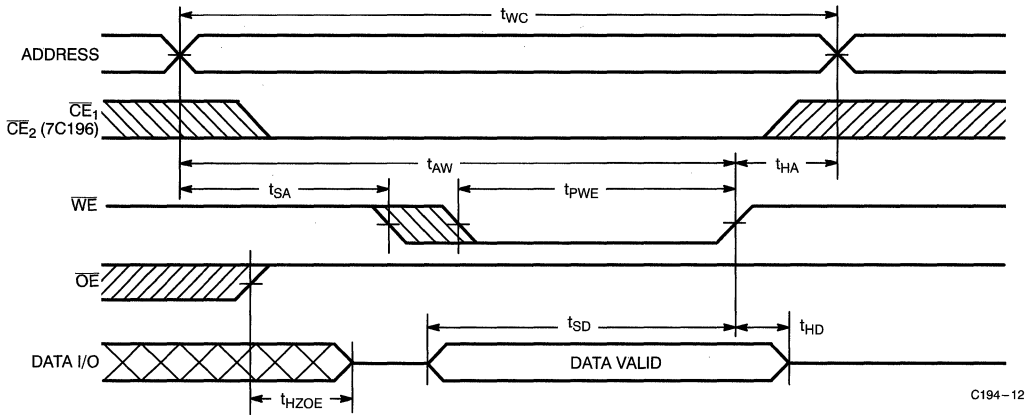
Switching Characteristics Over the Operating Range^[3, 8]

Parameter	Description	7C194-12 7C195-12 7C196-12		7C194-15 7C195-15 7C196-15		7C194-20 7C195-20 7C196-20		7C194-25 7C195-25 7C196-25		7C194-35 7C195-35 7C196-35		7C194-45 7C196-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t _{RC}	Read Cycle Time	12		15		20		25		35		45		ns
t _{AA}	Address to Data Valid		12		15		20		25		35		45	ns
t _{OHA}	Output Hold from Address Change	3		3		3		3		3		3		ns
t _{ACE1} , t _{ACE2}	CE LOW to Data Valid		12		15		20		25		35		45	ns
t _{DOE}	OE LOW to Data Valid		5		7		9		10		16		16	ns
t _{LZOE}	OE LOW to Low Z	0		0		0		3		3		3		ns
t _{HZOE}	OE HIGH to High Z ^[10]		5		7		9		11		15		15	ns
t _{LZCE1} , t _{LZCE2}	CE LOW to Low Z ^[9]	3		3		3		3		3		3		ns
t _{HZCE1} , t _{HZCE2}	CE HIGH to High Z ^[9,10]		5		7		9		11		15		15	ns
t _{PU}	CE LOW to Power-Up	0		0		0		0		0		0		ns
t _{PD}	CE HIGH to Power-Down		12		15		20		25		35		45	ns
WRITE CYCLE^[11]														
t _{WC}	Write Cycle Time	12		15		20		25		35		45		ns
t _{SCE}	CE LOW to Write End	9		10		15		18		22		22		ns
t _{AW}	Address Set-Up to Write End	9		10		15		20		25		35		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t _{PWE}	WE Pulse Width	8		9		15		18		22		22		ns
t _{SD}	Data Set-Up to Write End	8		9		10		10		15		15		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		0		ns
t _{LZWE}	WE HIGH to Low Z ^[9]	3		3		3		3		3		3		ns
t _{HZWE}	WE LOW to High Z ^[9, 8]		7		7		10	0	13	0	15	0	20	ns

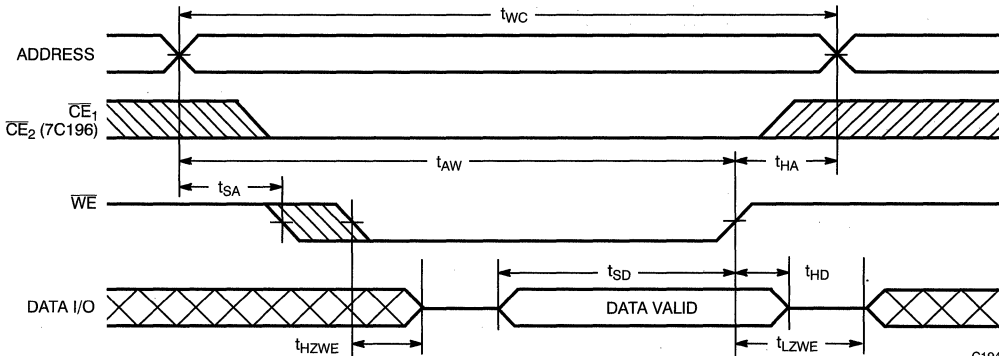
Shaded area contains preliminary information.

Notes:

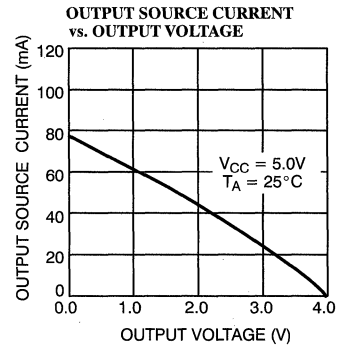
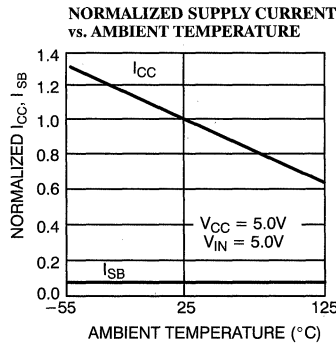
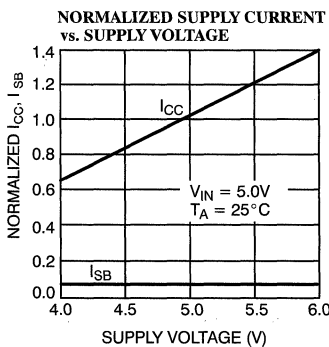
- Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of CE₁ LOW, CE₂ LOW, and WE LOW. All signals must be LOW to initiate a write and any signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write for 7C195 and 7C196 only)^[11, 15, 16]


C194-12

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[16, 17]


C194-11

Typical DC and AC Characteristics




Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C194-12PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-12VC	V13	24-Lead Molded SOJ	
15	CY7C194-15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-15VC	V13	24-Lead Molded SOJ	
	CY7C194-15DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C194-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-20VC	V13	24-Lead Molded SOJ	
	CY7C194-20DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C194-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-25VC	V13	24-Lead Molded SOJ	
	CY7C194-25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194-25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C194-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-35VC	V13	24-Lead Molded SOJ	
	CY7C194-35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194-35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C194-45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194-45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C195-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-12VC	V21	28-Lead Molded SOJ	
15	CY7C195-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-15VC	V21	28-Lead Molded SOJ	
20	CY7C195-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-20VC	V21	28-Lead Molded SOJ	
25	CY7C195-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-25VC	V21	28-Lead Molded SOJ	
35	CY7C195-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-35VC	V21	28-Lead Molded SOJ	

Shaded areas contain preliminary information.



256K x 1 Static RAM

Features

- High speed
 - 12 ns
- CMOS for optimum speed/power
- Low active power
 - 880 mW
- Low standby power
 - 220 mW
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

Functional Description

The CY7C197 is a high-performance CMOS static RAM organized as 256K words by 1 bit. Easy memory expansion is provided by an active LOW chip enable (CE) and three-state drivers. The CY7C197 has an automatic power-down feature, reducing the power consumption by 75% when deselected.

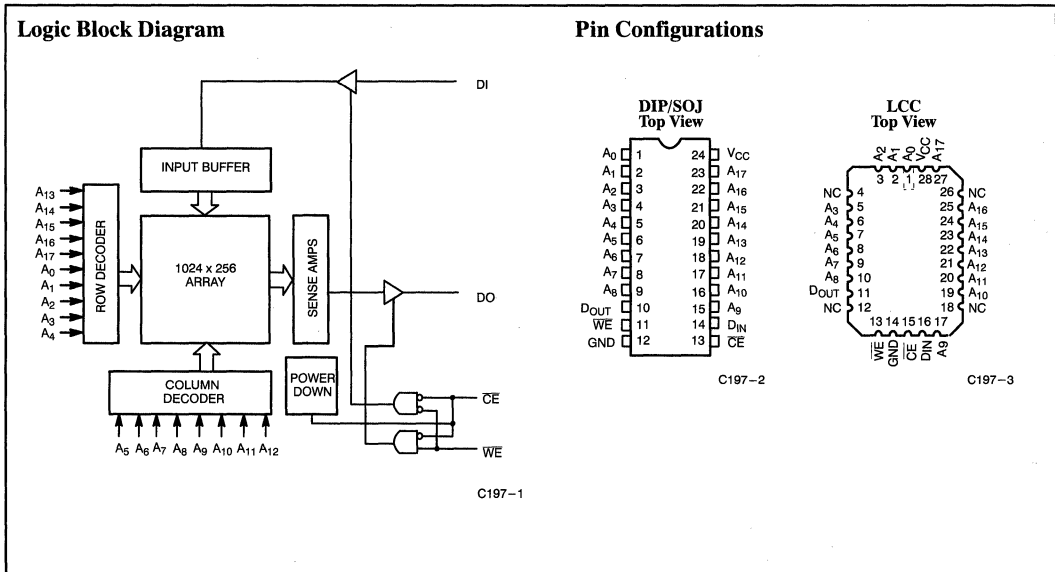
Writing to the device is accomplished when the chip enable (CE) and write enable (WE) inputs are both LOW. Data on the input pin (D_{IN}) is written into the memory

location specified on the address pins (A₀ through A₁₇).

Reading the device is accomplished by taking chip enable (CE) LOW while write enable (WE) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (D_{OUT}) pin.

The output pin stays in a high-impedance state when chip enable (CE) is HIGH or write enable (WE) is LOW.

The CY7C197 utilizes a die coat to ensure alpha immunity.



Selection Guide

		7C197-12	7C197-15	7C197-20	7C197-25	7C197-35	7C197-45
Maximum Access Time (ns)		12	15	20	25	35	45
Maximum Operating Current (mA)	Commercial	150	140	135	95	95	
	Military		160	150	105	105	105
Maximum Standby Current (mA)		30	30	30	30	30	30

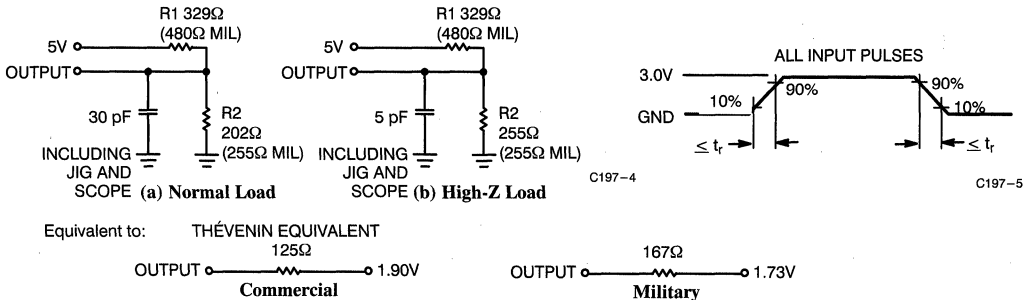
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Electrical Characteristics Over the Operating Range^[3] (continued)

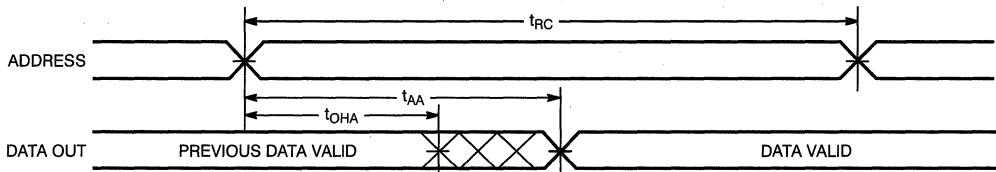
Parameter	Description	Test Conditions	7C197-20		7C197-25, 35, 45		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min. I _{OL} = 8.0 mA I _{OL} = 12.0 mA		0.4		0.4	V
			Mil		0.4		0.4
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3V	2.2	V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage ^[1]		-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com'l	135		95	mA
			Mil		150		
I _{SB1}	Automatic \overline{CE} Power Down Current—TTL Inputs ^[5]	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		30		30	mA
I _{SB2}	Automatic \overline{CE} Power-Down Current—CMOS Inputs ^[5]	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} < 0.3V		15		15	mA

Capacitance^[6]

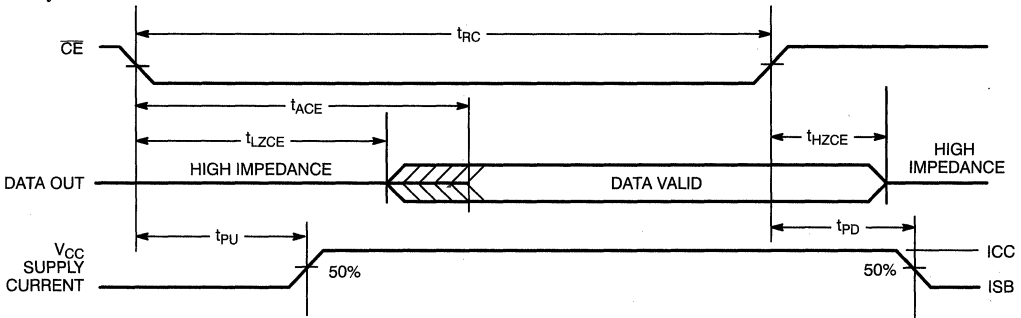
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	8	pF
C _{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms^[7]

Notes:

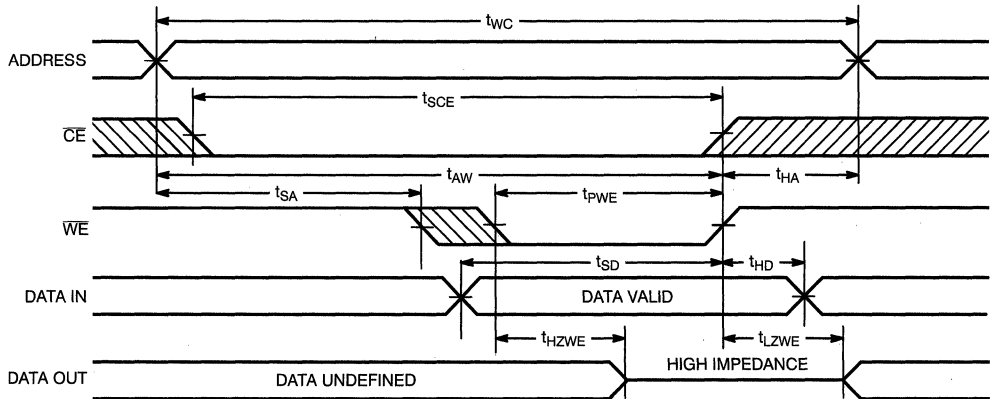
- Tested initially and after any design or process changes that may affect these parameters.
- t_r = ≤ 3 ns for the -12 and -15 speeds. t_r = ≤ 5 ns for the -20 and slower speeds.

Switching Waveforms
Read Cycle No. 1^[12, 13]


C197-6

Read Cycle No. 2^[12]


C197-7

Write Cycle No. 1 (\overline{WE} Controlled)^[11]


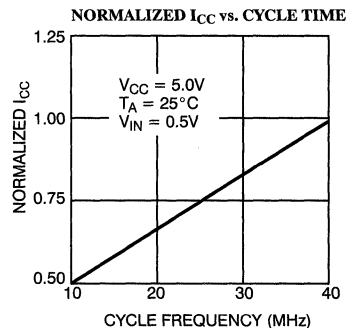
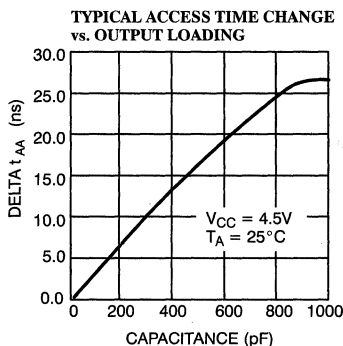
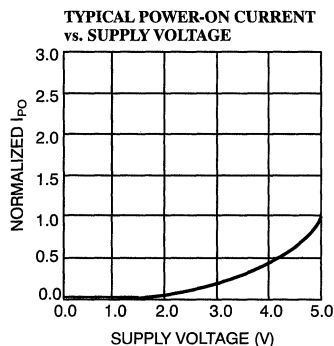
C197-8

Notes:

 12. \overline{WE} is HIGH for read cycle.

 13. Device is continuously selected, $\overline{CE} = V_{IL}$.

 14. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics (continued)

7C197 Truth Table

CE	WE	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C197-12PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197-12VC	V13	24-Lead Molded SOJ	
15	CY7C197-15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197-15VC	V13	24-Lead Molded SOJ	
	CY7C197-15DMB	D14	24-Lead (300-Mil) CerDIP	Military
20	CY7C197-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197-20VC	V13	24-Lead Molded SOJ	
	CY7C197-20DMB	D14	24-Lead (300-Mil) CerDIP	Military
25	CY7C197-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197-25VC	V13	24-Lead Molded SOJ	
	CY7C197-25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C197-25LMB	L54	24-Pin Rectangular Leadless Chip Carrier	
35	CY7C197-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197-35VC	V13	24-Lead Molded SOJ	
	CY7C197-35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C197-35LMB	L54	24-Pin Rectangular Leadless Chip Carrier	
45	CY7C197-45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C197-45LMB	L54	24-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

32K x 8 Static RAM

Features

- **High speed**
— 12 ns
- **Fast t_{DOE}**
- **CMOS for optimum speed/power**
- **Low active power**
— 880 mW
- **Low standby power**
— 165 mW
- **Easy memory expansion with \overline{CE} and \overline{OE} features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

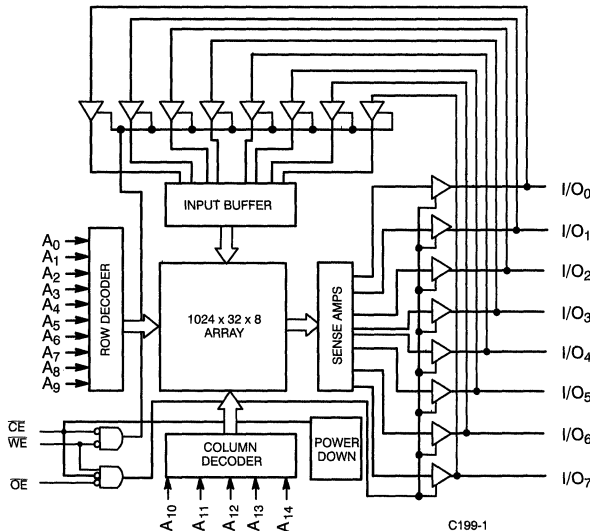
The CY7C199 is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}) and active LOW output enable (\overline{OE}) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 81% when deselected. The CY7C199 is in the standard 300-mil-wide DIP, SOJ, and LCC packages.

An active LOW write enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE} and \overline{WE} inputs are both LOW, data on the eight data input/

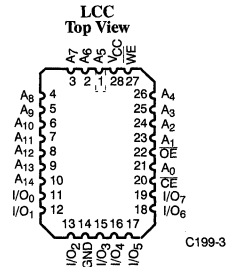
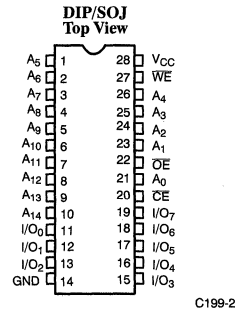
output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE} and \overline{OE} active LOW, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH. A die coat is used to ensure alpha immunity.

Logic Block Diagram



Pin Configurations



Electrical Characteristics Over the Operating Range^[3] (continued)

Parameter	Description	Test Conditions	7C199-10		7C199-12		7C199-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com ¹	160		160		155	mA
			L			130		110	
			Mil					180	
			L					150	
I _{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		30		30		30	mA
			L			20		20	mA
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0	Com ¹	10		10		10	mA
			L			500		500	μA
			Mil					15	mA
			L					5	

Shaded area contains preliminary information.

Electrical Characteristics Over the Operating Range^[3] (continued)

Parameter	Description	Test Conditions	7C199-20		7C199-25		7C199-35, 45		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V	
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3V	2.2	V _{CC} + 0.3V	2.2	V _{CC} + 0.3V	V	
V _{IL}	Input LOW Voltage		-0.5	0.8	-3.0	0.8	-3.0	0.8	V	
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	-5	+5	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	μA	
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300		-300	mA	
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com ¹	150		150		140	mA	
			L		100		100			100
			Mil		170		150			150
			L		130		130			130
I _{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		30		30		25	mA	
			L		15		15			15
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0	Com ¹	15		15		15	mA	
			L		500		500		500	μA
			Mil		15		15		15	mA
			L		5		5		5	

Note:

4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

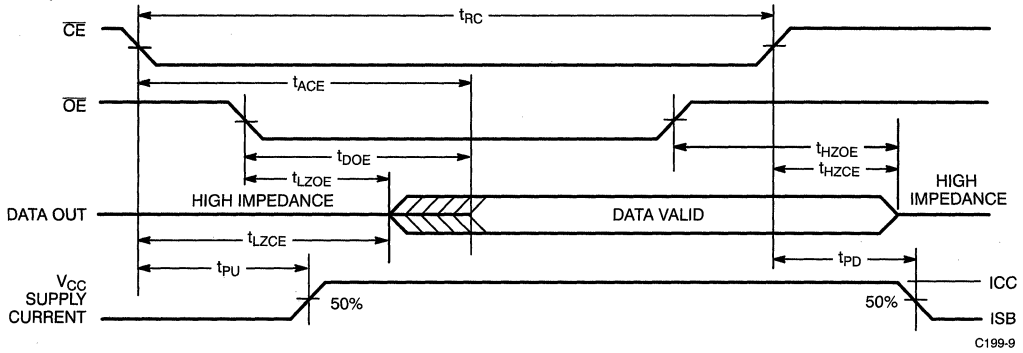
Switching Characteristics Over the Operating Range^[3, 8]

Parameter	Description	7C199-10		7C199-12		7C199-15		7C199-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t _{RC}	Read Cycle Time	10		12		15		20		ns
t _{AA}	Address to Data Valid		10		12		15		20	ns
t _{OHA}	Data Hold from Address Change	3		3		3		3		ns
t _{ACE}	\overline{CE} LOW to Data Valid		10		12		15		20	ns
t _{DOE}	\overline{OE} LOW to Data Valid		5		5		7		9	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[9]	0		0		0		0		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[9, 10]		5		5		7		9	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[9]	3		3		3		3		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[9, 10]		5		5		7		9	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		10		12		15		20	ns
WRITE CYCLE ^[11, 12]										
t _{WC}	Write Cycle Time	10		12		15		20		ns
t _{SCE}	\overline{CE} LOW to Write End	7		9		10		15		ns
t _{AW}	Address Set-Up to Write End	7		9		10		15		ns
t _{HA}	Address Hold from Write End	0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	7		8		9		15		ns
t _{SD}	Data Set-Up to Write End	5		8		9		10		ns
t _{HD}	Data Hold from Write End	0		0		0		0		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[10]		5		7		7		10	ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[9]	3		3		3		3		ns

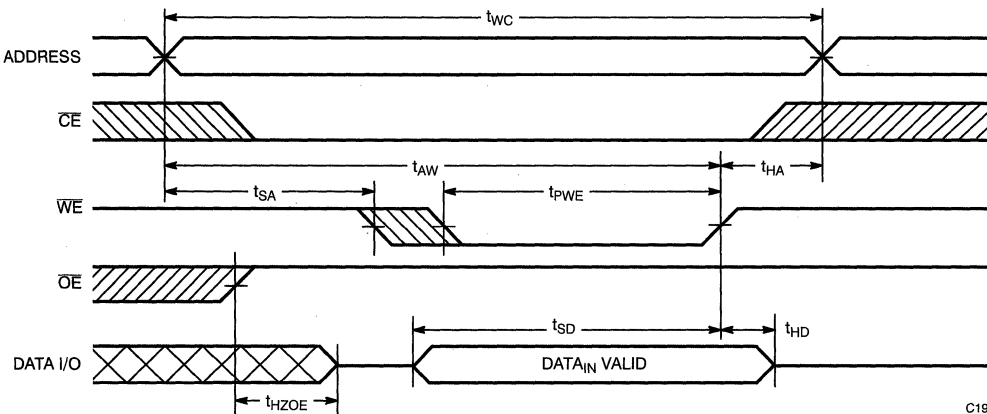
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Notes:

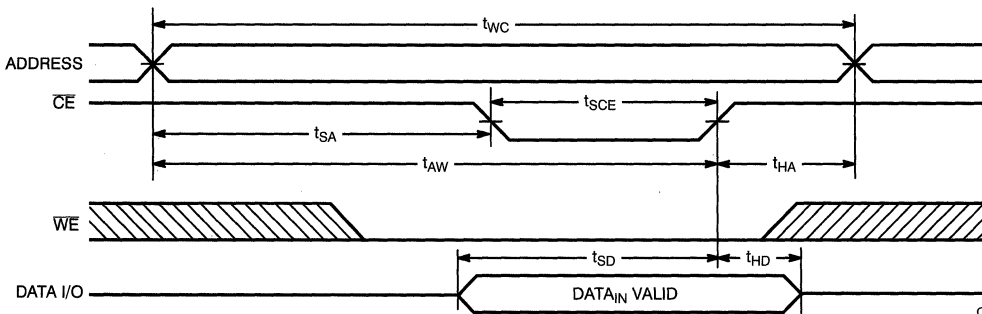
- Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms (continued)
Read Cycle No. 2^[14, 15]


C199-9

Write Cycle No. 1 (WE Controlled)^[11, 16, 17]


C199-10

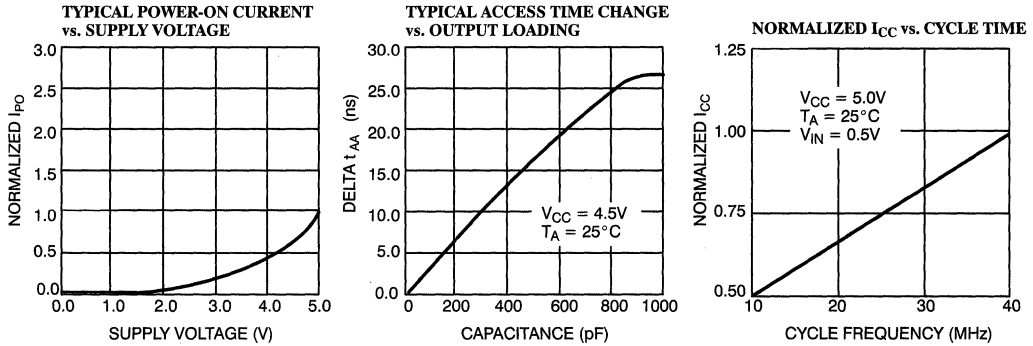
Write Cycle No. 2 (CE Controlled)^[11, 16, 17]


C199-11

Notes:

 15. Address valid prior to or coincident with \overline{CE} transition LOW.
 16. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

 17. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics (continued)

Truth Table

\overline{CE}	\overline{WE}	\overline{OE}	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range	
10	CY7C199-10VC	V21	28-Lead Molded SOJ	Commercial	
12	CY7C199-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial	
	CY7C199L-12PC	P21	28-Lead (300-Mil) Molded DIP		
	CY7C199-12VC	V21	28-Lead Molded SOJ		
	CY7C199L-12VC	V21	28-Lead Molded SOJ		
	CY7C199-12ZC	Z28	28-Lead Thin Small Outline Package		
15	CY7C199L-12ZC	Z28	28-Lead Thin Small Outline Package	Commercial	
	CY7C199-15PC	P21	28-Lead (300-Mil) Molded DIP		
	CY7C199L-15PC	P21	28-Lead (300-Mil) Molded DIP		
	CY7C199-15VC	V21	28-Lead Molded SOJ		
	CY7C199L-15VC	V21	28-Lead Molded SOJ		
	CY7C199-15ZC	Z28	28-Lead Thin Small Outline Package		
	CY7C199L-15ZC	Z28	28-Lead Thin Small Outline Package		
	CY7C199-15DMB	D22	28-Lead (300-Mil) CerDIP		Military
	CY7C199L-15DMB	D22	28-Lead (300-Mil) CerDIP		
	CY7C199-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier		
20	CY7C199L-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	Commercial	
	CY7C199-20PC	P21	28-Lead (300-Mil) Molded DIP		
	CY7C199L-20PC	P21	28-Lead (300-Mil) Molded DIP		
	CY7C199-20VC	V21	28-Lead Molded SOJ		
	CY7C199L-20VC	V21	28-Lead Molded SOJ		
20	CY7C199-20ZC	Z28	28-Lead Thin Small Outline Package	Commercial	
	CY7C199L-20ZC	Z28	28-Lead Thin Small Outline Package		
	CY7C199-20ZC	Z28	28-Lead Thin Small Outline Package		

**MILITARY SPECIFICATIONS
Group A Subgroup Testing**
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

Document #: 38-00239-B



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature -65°C to +150°C
- Ambient Temperature with Power Applied -55°C to +125°C
- Supply Voltage on V_{CC} Relative to GND^[1] . . -0.5V to +7.0V
- DC Voltage Applied to Outputs in High Z State^[1] -0.5V to V_{CC} + 0.5V
- DC Input Voltage^[1] -0.5V to V_{CC} + 0.5V
- Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	7C1001-12 7C1002-12		7C1001-15 7C1002-15		7C1001-20 7C1002-20		7C1001-25 7C1002-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com ¹	165		155		140		130	mA
			Mil			165		150		140	
I _{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Com ¹	50		40		30		30	mA
			Mil			40		30		30	
I _{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f=0	Com ¹	2		2		2		2	mA
			Mil			2		2		2	

Capacitance^[5]

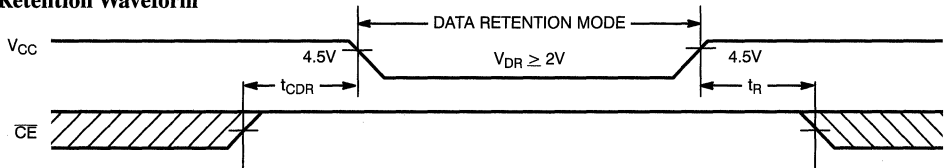
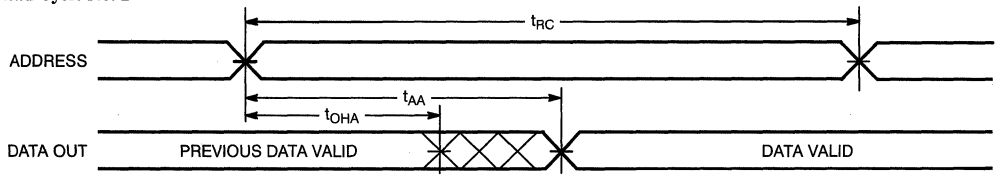
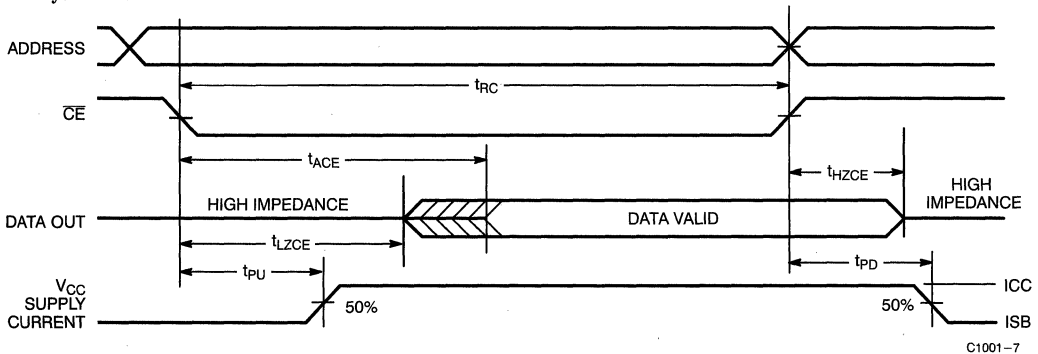
Parameter	Description	Test Conditions	Max.	Unit
C _{IN} : Addresses	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	7	pF
C _{IN} : Controls			10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

1. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
2. T_A is the “instant on” case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

Data Retention Characteristics Over the Operating Range (L Version Only)

Parameters	Description	Conditions ^[10]	Commercial		Military		Units
			Min.	Max.	Min.	Max.	
V _{DR}	V _{CC} for Retention Data		2.0		2.0		V
I _{CCDR}	Data Retention Current	V _{CC} = V _{DR} = 2.0V, CE ≥ V _{CC} - 0.3V,		50		70	μA
t _{CDR} ^[5]	Chip Deselect to Data Retention Time	V _{IN} ≥ V _{CC} - 0.3V or	0		0		ns
t _r ^[5]	Operation Recovery Time	V _{IN} ≤ 0.3V	t _{RC}		t _{RC}		ns

Data Retention Waveform

Switching Waveforms
Read Cycle No. 1^[11, 12]

Read Cycle No. 2^[12, 13]

Notes:

 10. No input may exceed V_{CC} + 0.5V.

 11. Device is continuously selected, CE = V_{IL}.

12. WE is HIGH for read cycle.

13. Address valid prior to or coincident with CE transition LOW.

Truth Table

CE	WE	O ₀ - O ₃	Mode	Power
H	X	High Z	Power-Down	Standby (I _{SB})
L	H	Data Out	Read	Active (I _{CC})
L	L	High Z	7C1002: Standard Write	Active (I _{CC})
L	L	Input Tracking	7C1001: Transparent Write ^[15]	Active (I _{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1001-12PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1001-12VC	V32	32-Lead (300-Mil) Molded SOJ	
15	CY7C1001-15PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1001-15VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1001-15DMB	D32	32-Lead (300-Mil) CerDIP	Military
20	CY7C1001-20PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1001-20VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1001-20DMB	D32	32-Lead (300-Mil) CerDIP	Military
25	CY7C1001-25DC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1001-25VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1001-25DMB	D32	32-Lead (300-Mil) CerDIP	Military

Contact factory for "L" version availability.

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1002-12PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1002-12VC	V32	32-Lead (300-Mil) Molded SOJ	
15	CY7C1002-15PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1002-15VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1002-15DMB	D32	32-Lead (300-Mil) CerDIP	Military
20	CY7C1002-20PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1002-20VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1002-20DMB	D32	32-Lead (300-Mil) CerDIP	Military
25	CY7C1002-25PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1002-25VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1002-25DMB	D32	32-Lead (300-Mil) CerDIP	Military

Contact factory for "L" version availability.

Note:

15. Outputs track inputs after specified delay.

256K x 4 Static RAM

Features

- **High speed**
— $t_{AA} = 12$ ns
- **CMOS for optimum speed/power**
- **Low active power**
— 910 mW
- **Low standby power**
— 275 mW
- **2.0V data retention (optional)**
— 100 μ W
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C1006 is a high-performance CMOS static RAM organized as 262,144 words by 4 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}), an active LOW output enable (\overline{OE}), and three-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 65% when deselected.

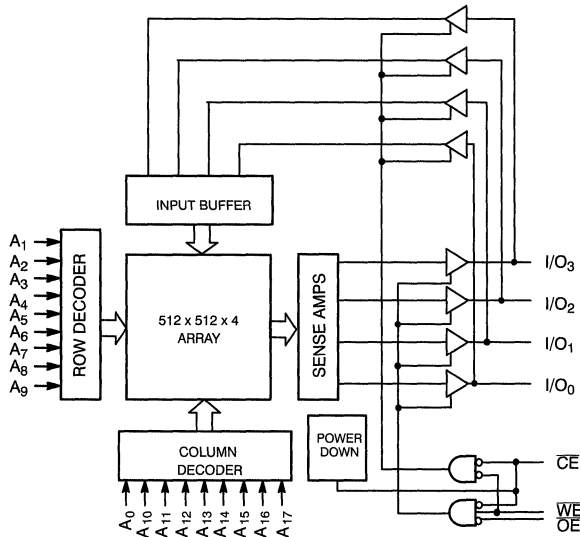
Writing to the device is accomplished by taking chip enable (\overline{CE}) and write enable (\overline{WE}) inputs LOW. Data on the four I/O pins (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking chip enable (\overline{CE}) and output enable (\overline{OE}) LOW while forcing write enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the four I/O pins.

The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE} and \overline{WE} LOW).

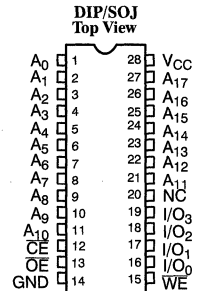
The CY7C1006 is available in standard 300-mil-wide DIPs and SOJs.

Logic Block Diagram



C1006-1

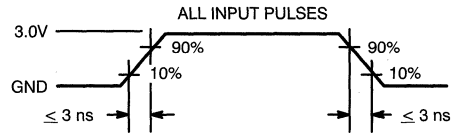
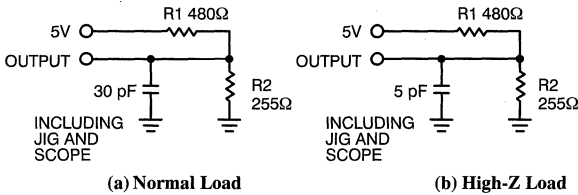
Pin Configuration



C1006-2

Selection Guide

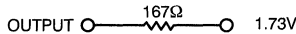
		7C1006-12	7C1006-15	7C1006-20	7C1006-25
Maximum Access Time (ns)		12	15	20	25
Maximum Operating Current (mA)	Commercial	165	155	140	130
	Military		165	150	140
Maximum Standby Current (mA)	Commercial	50	40	30	30
	Military		40	30	30

AC Test Loads and Waveforms


C1006-3

C1006-4

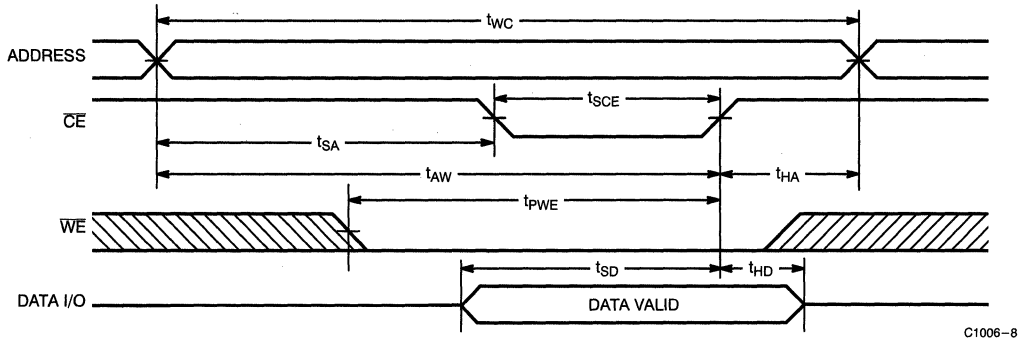
Equivalent to: THÉVENIN EQUIVALENT


Switching Characteristics Over the Operating Range^[3, 6]

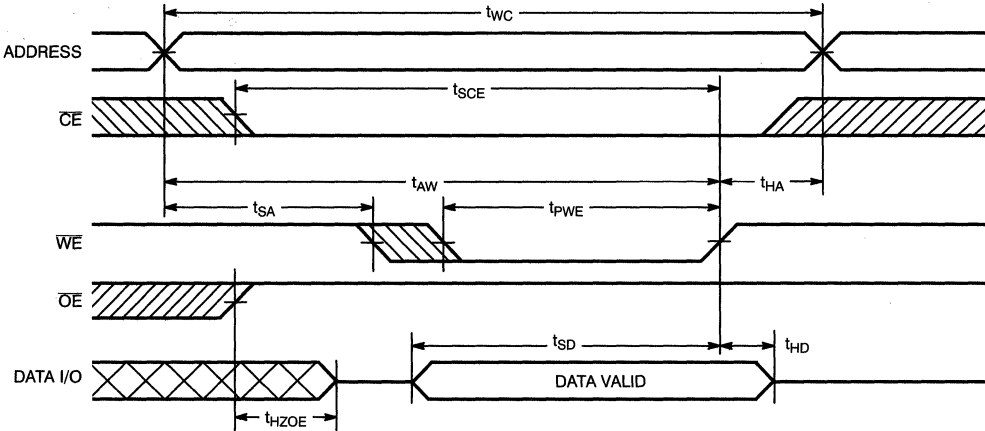
Parameter	Description	7C1006-12		7C1006-15		7C1006-20		7C1006-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t _{RC}	Read Cycle Time	12		15		20		25		ns
t _{AA}	Address to Data Valid		12		15		20		25	ns
t _{OHA}	Data Hold from Address Change	3		3		3		3		ns
t _{ACE}	\overline{CE} LOW to Data Valid		12		15		20		25	ns
t _{DOE}	\overline{OE} LOW to Data Valid		6		7		8		10	ns
t _{LZOE}	\overline{OE} LOW to Low Z	0		0		0		0		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[7, 8]		6		7		8		10	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[7]	3		3		3		3		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[7, 8]		6		7		8		10	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		12		15		20		25	ns
WRITE CYCLE^[9, 10]										
t _{WC}	Write Cycle Time	12		15		20		25		ns
t _{SCE}	\overline{CE} LOW to Write End	10		12		15		20		ns
t _{AW}	Address Set-Up to Write End	10		12		15		20		ns
t _{HA}	Address Hold from Write End	0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	10		12		15		20		ns
t _{SD}	Data Set-Up to Write End	7		8		10		15		ns
t _{HD}	Data Hold from Write End	0		0		0		0		ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[8]	3		3		3		3		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[7, 8]		6		7		8		10	ns

Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{CE} Controlled)^[15, 16]


C1006-8

Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[15, 16]


C1006-9

Notes:

15. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.
16. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1006-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1006-12VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C1006-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1006-15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C1006-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7C1006-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1006-20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C1006-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
25	CY7C1006-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1006-25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C1006-25DMB	D22	28-Lead (300-Mil) CerDIP	Military

Contact factory for "L" version availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{Ix}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

Document #: 38-00201-B



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature -65°C to +150°C
- Ambient Temperature with Power Applied -55°C to +125°C
- Supply Voltage on V_{CC} Relative to GND^[1] -0.5V to +7.0V
- DC Voltage Applied to Outputs in High Z State^[1] -0.5V to V_{CC} + 0.5V
- DC Input Voltage^[1] -0.5V to V_{CC} + 0.5V
- Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	7C1007-12		7C1007-15		7C1007-20		7C1007-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0mA, f = f _{MAX} = 1/t _{RC}	Com'l	150		135		125		120	mA
			Mil			145		135		130	
I _{SB1}	Automatic \overline{CE} Power-Down Current - TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Com'l	50		40		30		30	mA
			Mil			40		30		30	
I _{SB2}	Automatic \overline{CE} Power-Down Current - CMOS Inputs	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0	Com'l	2		2		2		2	mA
			Mil			2		2		2	

Capacitance^[5]

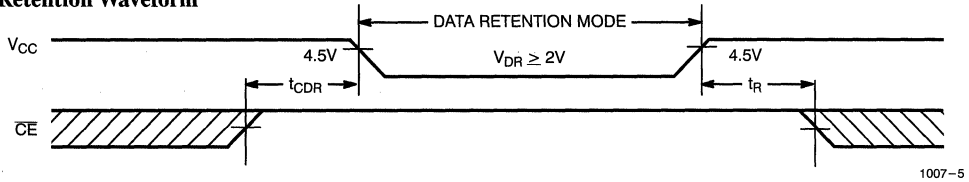
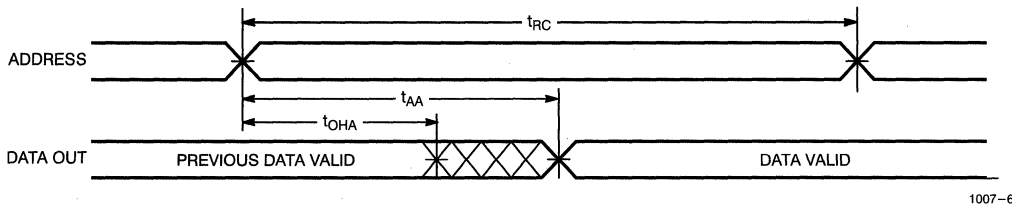
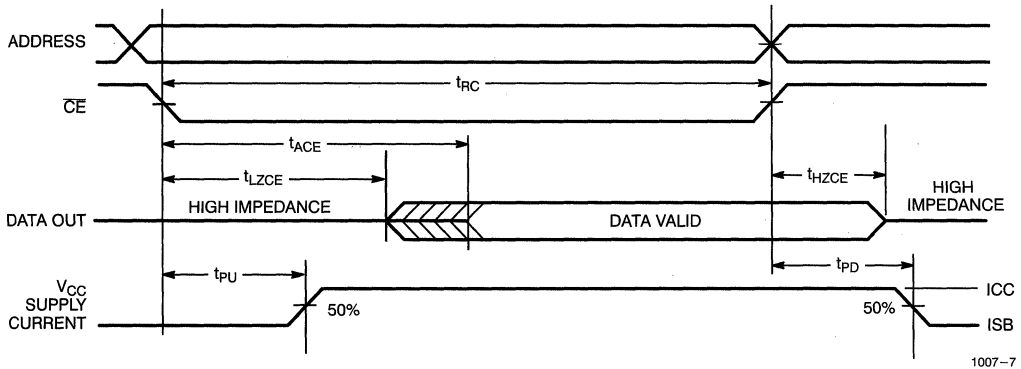
Parameter	Description	Test Conditions	Max.	Unit
C _{IN} : Addresses	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	7	pF
C _{IN} : Controls			10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

1. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

Data Retention Characteristics Over the Operating Range (L Version Only)

Parameter	Description	Conditions ^[10]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V _{DR}	V _{CC} for Data Retention		2.0		2.0		V
I _{CCDR}	Data Retention Current	V _{CC} = V _{DR} = 2.0V, CE ≥ V _{CC} - 0.3V,		50		70	μA
t _{CDR} ^[5]	Chip Deselect to Data Retention Time	V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V	0		0		ns
t _R ^[5]	Operation Recovery Time		t _{RC}		t _{RC}		ns

Data Retention Waveform

Switching Waveforms
Read Cycle No. 1^[11, 12]

Read Cycle No. 2^[12, 13]

Notes:

10. No input may exceed V_{CC} + 0.5V.

11. Device is continuously selected, CE = V_{IL}.

12. WE is HIGH for read cycle.

13. Address valid prior to or coincident with CE transition LOW.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1007-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1007-12VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C1007-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1007-15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C1007-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7C1007-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1007-20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C1007-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
25	CY7C1007-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1007-25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C1007-25DMB	D22	28-Lead (300-Mil) CerDIP	Military

Contact factory for "L" version availability.

**MILITARY SPECIFICATIONS
Group A Subgroup Testing**
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _I X	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3

Document #: 38-00198-B

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage on V _{CC} to Relative GND ^[1] ..	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ^[1]	-0.5V to V _{CC} + 0.5V
DC Input Voltage ^[1]	-0.5V to V _{CC} + 0.5V
Current into Outputs (LOW)	20 mA

Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature ^[2]	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	7C1009-12		7C1009-15		7C1009-20		7C1009-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com ¹	185		170		155		145	mA
			Mil			180		170		160	
I _{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V _{CC} , CE ₁ ≥ V _{IH} or CE ₂ ≤ V _{IL} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Com ¹	45		40		30		30	mA
			Mil			40		30		30	
I _{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V _{CC} , CE ₁ ≥ V _{CC} - 0.3V, or CE ₂ ≤ 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f=0	Com ¹	2		2		2		2	mA
			Mil			2		2		2	

Capacitance^[5]

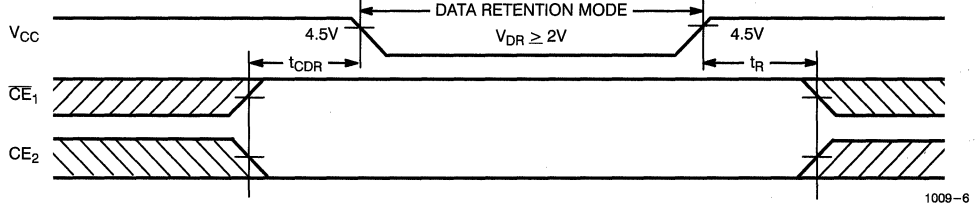
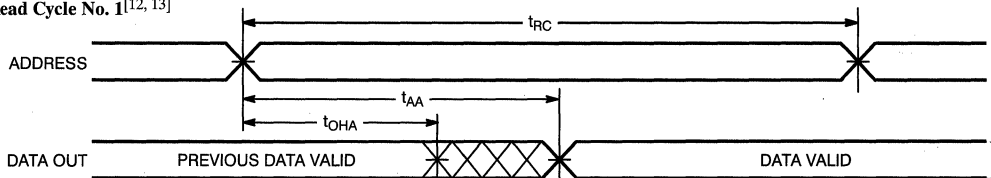
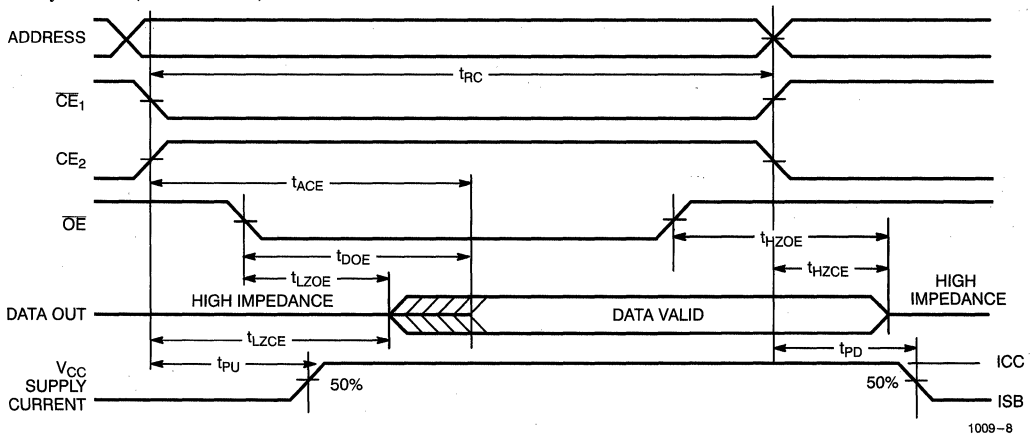
Parameter	Description	Test Conditions	Max.	Unit
C _{IN} : Address	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	7	pF
C _{IN} : Controls			10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

Data Retention Characteristics Over the Operating Range (L Version Only)

Parameter	Description	Conditions ^[11]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Data Retention		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $CE_1 \leq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$		50		70	μA
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		0		ns
$t_R^{[5]}$	Operation Recovery Time		t_{RC}		t_{RC}		ns

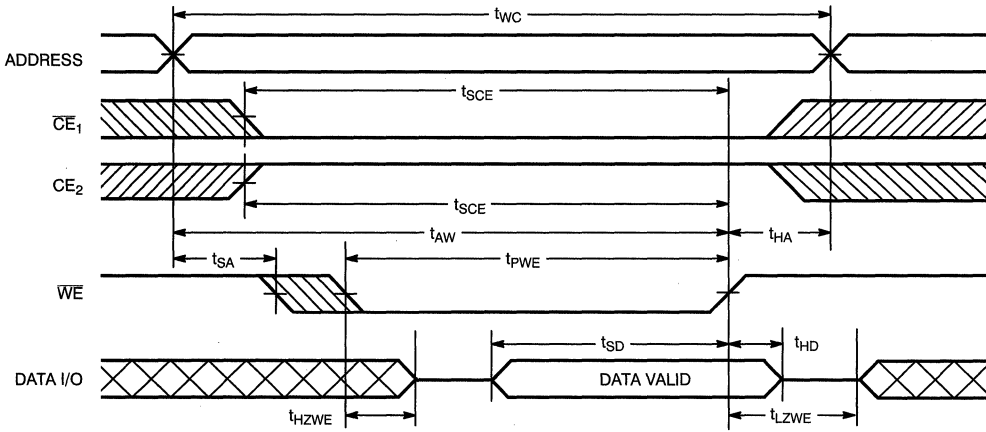
Data Retention Waveform

Switching Waveforms
Read Cycle No. 1^[12, 13]

Read Cycle No. 2 (\overline{OE} Controlled)^[13, 14]

Notes:

11. No input may exceed $V_{CC} + 0.5V$.

12. Device is continuously selected. \overline{OE} , $CE_1 = V_{IL}$, $CE_2 = V_{IH}$.

13. \overline{WE} is HIGH for read cycle.

14. Address valid prior to or coincident with \overline{CE}_1 transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)
Write Cycle No. 3 (WE Controlled, OE LOW)^[10, 16]


1009-11

Truth Table

CE ₁	CE ₂	OE	WE	I/O ₀ - I/O ₇	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I _{SB})
X	L	X	X	High Z	Power-Down	Standby (I _{SB})
L	H	L	H	Data Out	Read	Active (I _{CC})
L	H	X	L	Data In	Write	Active (I _{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I _{CC})



256K x 4 Static RAM

Features

- High speed
— $t_{AA} = 10$ ns
- CMOS for optimum speed/power
- Center power/ground pinout
- Automatic power-down when deselected
- TTL-compatible inputs and outputs

Functional Description

The CY7C1014 is a high-performance CMOS static RAM organized as 262,144

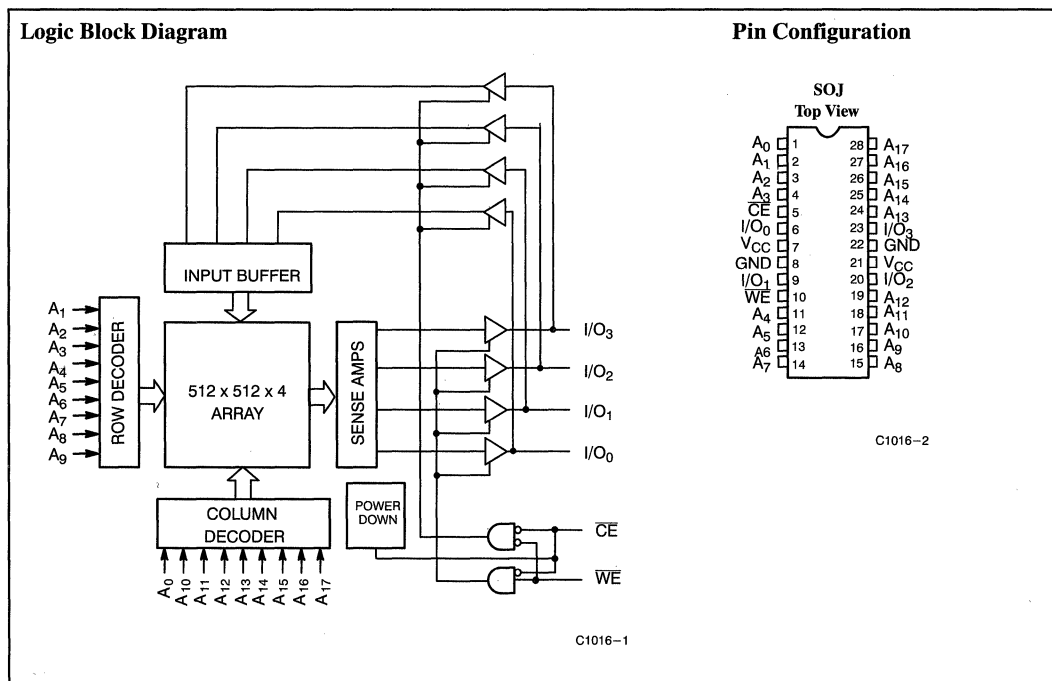
words by 4 bits. Easy memory expansion is provided by an active LOW chip enable (CE), and three-state drivers. The device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking chip enable (CE) and write enable (WE) inputs LOW. Data on the four I/O pins (I/O₀ through I/O₃) is then written into the location specified on the address pins (A₀ through A₁₇).

Reading from the device is accomplished by taking chip enable (CE) LOW while forcing write enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the four I/O pins.

The four input/output pins (I/O₀ through I/O₃) are placed in a high-impedance state when the device is deselected (CE HIGH), or during a write operation (CE and WE LOW).

The CY7C1014 is available in standard 400-mil-wide SOJs.



Selection Guide

		7C1014-10	7C1014-12	7C1014-15
Maximum Access Time (ns)		10	12	15
Maximum Operating Current (mA)	Commercial	175	165	155
	Military		175	165
Maximum Standby Current (mA)	Commercial	55	50	40
	Military		50	40



128K x 8 Static RAM

Features

- High speed
— $t_{AA} = 10$ ns
- CMOS for optimum speed/power
- Center power/ground pinout
- Automatic power-down when deselected
- Easy memory expansion with \overline{CE} and \overline{OE} options

Functional Description

The CY7C1019 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}), an active LOW output enable (\overline{OE}), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption significantly when deselected.

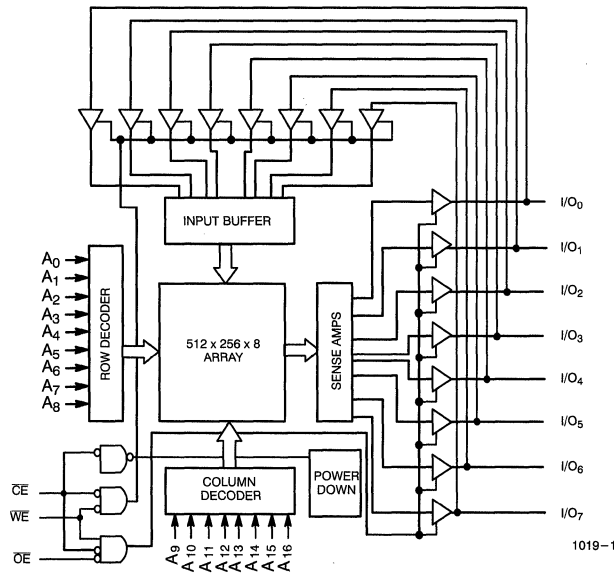
Writing to the device is accomplished by taking chip enable (\overline{CE}) and write enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable (\overline{CE}) and output enable (\overline{OE}) LOW while forcing write enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

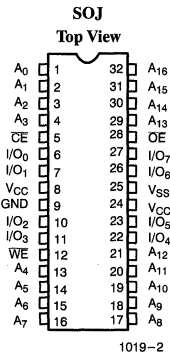
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1019 is available in standard 400-mil-wide SOJs.

Logic Block Diagram



Pin Configurations



Selection Guide

	7C1019-10	7C1019-12	7C1019-15
Maximum Access Time (ns)	10	12	15
Maximum Operating Current (mA)	Commercial	195	170
	Military	185	180
Maximum Standby Current (mA)	Commercial	50	40
	Military	50	40

64K x 18 Synchronous Cache RAM

Features

- Supports 66-MHz Pentium™ micro-processor cache systems with zero wait states
- 64K by 18 common I/O
- Fast clock-to-output times — 8.5 ns
- Two-bit wraparound counter supporting Pentium microprocessor and 486 burst sequence (CY7C1031)
- Two-bit wraparound counter supporting linear burst sequence (CY7C1032)
- Separate processor and controller address strobes
- Synchronous self-timed write

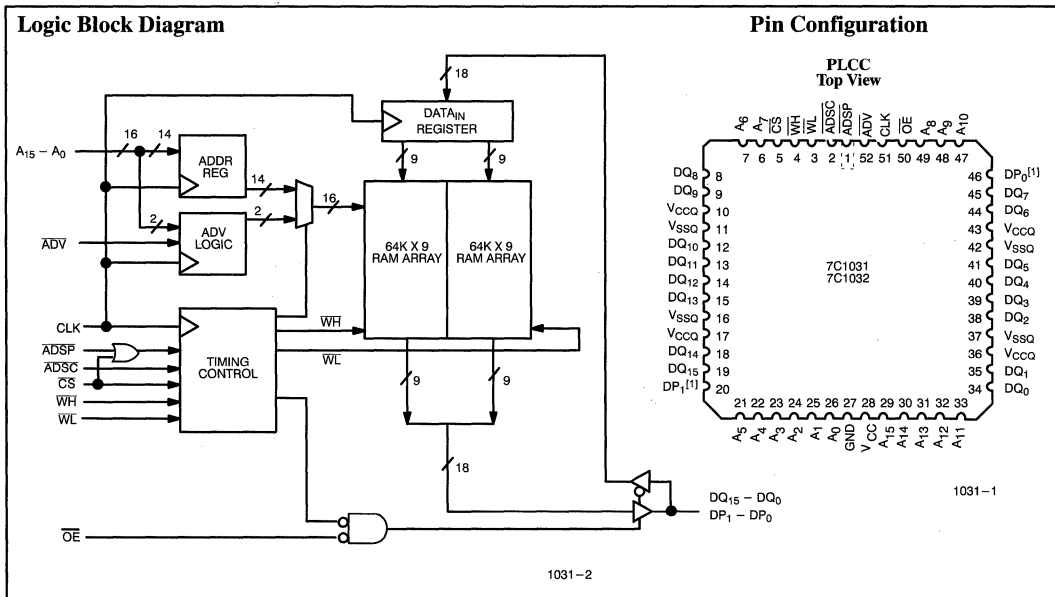
- Direct interface with the processor and external cache controller
- Asynchronous output enable
- I/Os capable of 3.3V operation
- JEDEC-standard pinout
- 52-pin PLCC and PQFP packaging

Functional Description

The CY7C1031 and CY7C1032 are 64K by 18 synchronous cache RAMs designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 8.5 ns. A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

The CY7C1031 is designed for Intel Pentium and i486 CPU-based systems; its counter follows the burst sequence of the Pentium and the i486 processors. The CY7C1032 is architected for processors with linear burst sequences. Burst accesses can be initiated with the processor address strobe (ADSP) or the cache controller address strobe (ADSC) inputs. Address advancement is controlled by the address advancement (ADV) input.

A synchronous self-timed write mechanism is provided to simplify the write interface. A synchronous chip select input and an asynchronous output enable input provide easy control for bank selection and output three-state control.


Selection Guide

		7C1031-7 7C1032-7	7C1031-8 7C1032-8	7C1031-10 7C1032-10	7C1031-12 7C1032-12
Maximum Access Time (ns)		7	8.5	10	12
Maximum Operating Current (mA)	Commercial	300	280	280	230
	Military				235

Shaded area contains preliminary information.
Pentium is a trademark of Intel Corporation.

Note:

1. DP₀ and DP₁ are functionally equivalent to DQ_x.

Pin Definitions

Signal Name	Type	# of Pins	Description
V _{CC}	Input	1	+5V Power
V _{CCQ}	Input	4	+5V or 3.3V (Outputs)
GND	Input	1	Ground
V _{SSQ}	Input	4	Ground (Outputs)
CLK	Input	1	Clock
A ₁₅ – A ₀	Input	16	Address
ADSP	Input	1	Address Strobe from Processor
ADSC	Input	1	Address Strobe from Cache Controller
WH	Input	1	Write Enable – High Byte
WL	Input	1	Write Enable – Low Byte
ADV	Input	1	Advance
OE	Input	1	Output Enable
CS	Input	1	Chip Select
DQ ₁₅ –DQ ₀	Input/Output	16	Regular Data
DP ₁ –DP ₀	Input/Output	2	Parity Data

Pin Descriptions

Signal Name	I/O	Description
Input Signals		
CLK	I	Clock signal. It is used to capture the address, the data to be written, and the following control signals: ADSP, ADSC, CS, WH, WL, and ADV. It is also used to advance the on-chip auto-address-increment logic (when the appropriate control signals have been set).
A ₁₅ –A ₀	I	Sixteen address lines used to select one of 64K locations. They are captured in an on-chip register on the rising edge of CLK if ADSP or ADSC is LOW. The rising edge of the clock also loads the lower two address lines, A ₁ – A ₀ , into the on-chip auto-address-increment logic if ADSP or ADSC is LOW.
ADSP	I	Address strobe from processor. This signal is sampled at the rising edge of CLK. When this input and/or ADSC is asserted, A ₀ –A ₁₅ will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. If both ADSP and ADSC are asserted at the rising edge of CLK, only ADSP will be recognized. The ADSP input should be connected to the ADS output of the processor. ADSP is ignored when CS is HIGH.
ADSC	I	Address strobe from cache controller. This signal is sampled at the rising edge of CLK. When this input and/or ADSP is asserted, A ₀ –A ₁₅ will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. The ADSC input should <i>not</i> be connected to the ADS output of the processor.

Signal Name	I/O	Description
WH	I	Write signal for the high-order half of the RAM array. This signal is sampled by the rising edge of CLK. If WH is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of DQ ₁₅ – DQ ₈ and DP ₁ from the on-chip data register into the selected RAM location. There is one exception to this. If ADSP, WH, and CS are asserted (LOW) at the rising edge of CLK, the write signal, WH, is ignored. Note that ADSP has no effect on WH if CS is HIGH.
WL	I	Write signal for the low-order half of the RAM array. This signal is sampled by the rising edge of CLK. If WL is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of DQ ₇ – DQ ₀ and DP ₀ from the on-chip data register into the selected RAM location. There is one exception to this. If ADSP, WL, and CS are asserted (LOW) at the rising edge of CLK, the write signal, WL, is ignored. Note that ADSP has no effect on WL if CS is HIGH.
ADV	I	Advance. This signal is sampled by the rising edge of CLK. When it is asserted, it automatically increments the 2-bit on-chip auto-address-increment counter. In the CY7C1032, the address will be incremented linearly. In the CY7C1031, the address will be incremented according to the Pentium/486 burst sequence. This signal is ignored if ADSP or ADSC is asserted concurrently with CS. Note that ADSP has no effect on ADV if CS is HIGH.
CS	I	Chip select. This signal is sampled by the rising edge of CLK. If CS is HIGH and ADSC is LOW, the SRAM is deselected. If CS is LOW and ADSC or ADSP is LOW, a new address is captured by the address register. If CS is HIGH, ADSP is ignored.

Electrical Characteristics (continued)

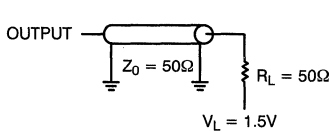
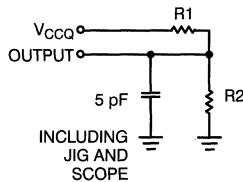
Parameter	Description	Test Conditions	7C1031-7 7C1032-7		7C1031-8 7C1032-8		7C1031-10 7C1032-10		7C1031-12 7C1032-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} =Max., V _{OUT} =GND		-300		-300		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} =Max., I _{out} =0mA, f=f _{MAX} =1/t _{CYC}	Com'1	300		280		280		230	mA
			Mil							250	
I _{SB1}	Automatic CE Power-Down Current-TTL Inputs	Max. V _{CC} , CS ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f=f _{MAX}	Com'1	90		80		80		60	mA
			Mil							70	
I _{SB2}	Automatic CE Power-Down Current-CMOS Inputs	Max. V _{CC} , CS ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f=0 ^[6]	Com'1	30		30		30		30	mA
			Mil							50	

Shaded areas contain preliminary information

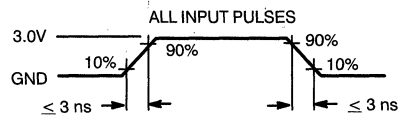
Capacitance^[7]

Parameter	Description	Test Conditions	Max.	Unit	
C _{IN} : Addresses	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	Com'1	4.5	pF
			Mil	6	
C _{IN} : Other Inputs			Com'1	5	pF
			Mil	8	
C _{OUT}	Output Capacitance		Com'1	8	pF
			Mil	10	

Shaded areas contain advanced information

AC Test Loads and Waveforms

(a) Normal Load

(b)^[8] High-Z Load

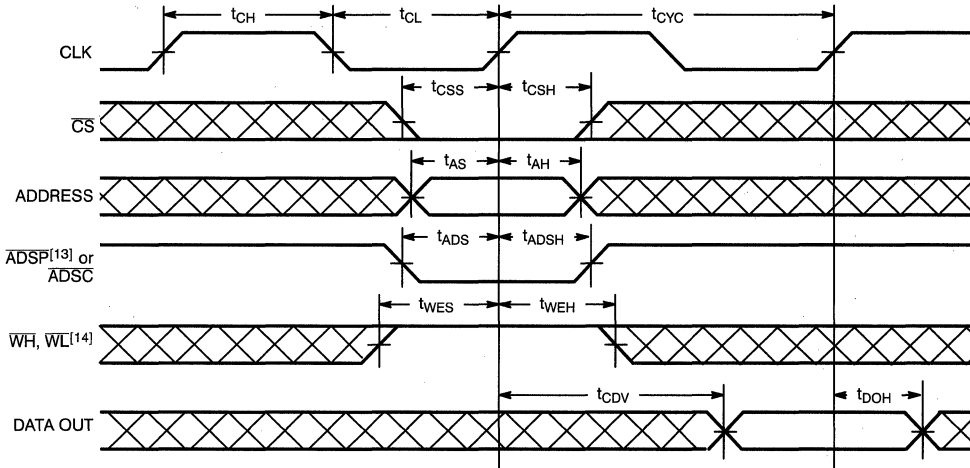
1031-3



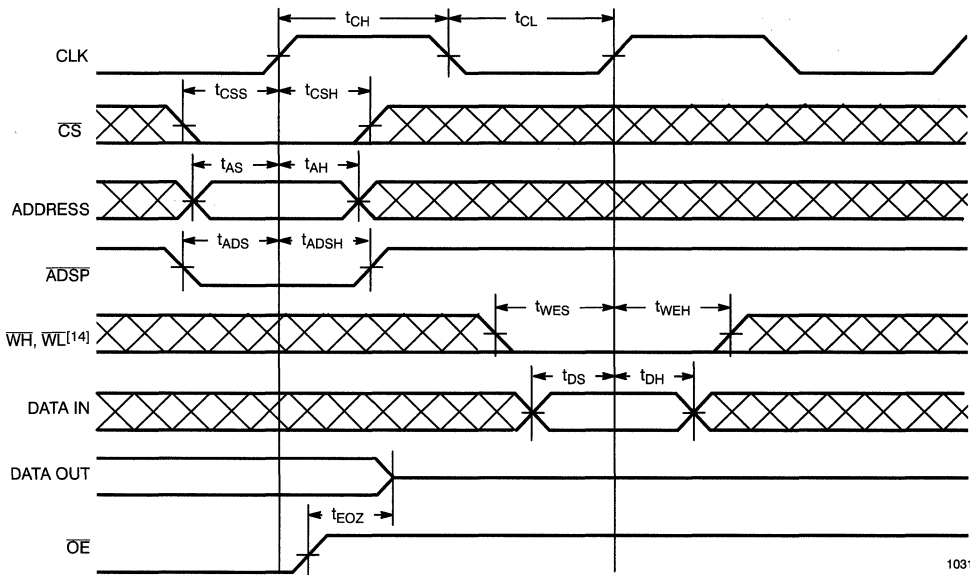
1031-4

Notes:

- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Inputs are disabled, clock is allowed to run at speed.
- Tested initially and after any design or process changes that may affect these parameters.
- Resistor values for V_{CC}=5V are: R1=1179Ω and R2=868Ω Resistor values for V_{CC}=3.3V are R1=317Ω and R2=348Ω

Switching Waveforms
Single Read^[12]


1031-6

Single Write Timing: Write Initiated by $\overline{\text{ADSP}}$


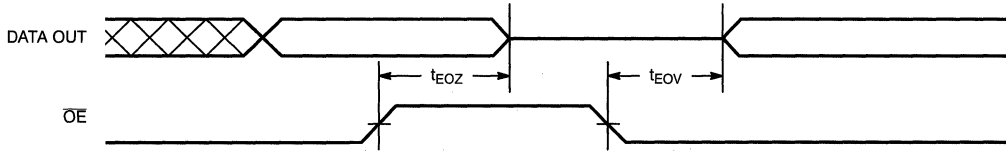
1031-5

Notes:

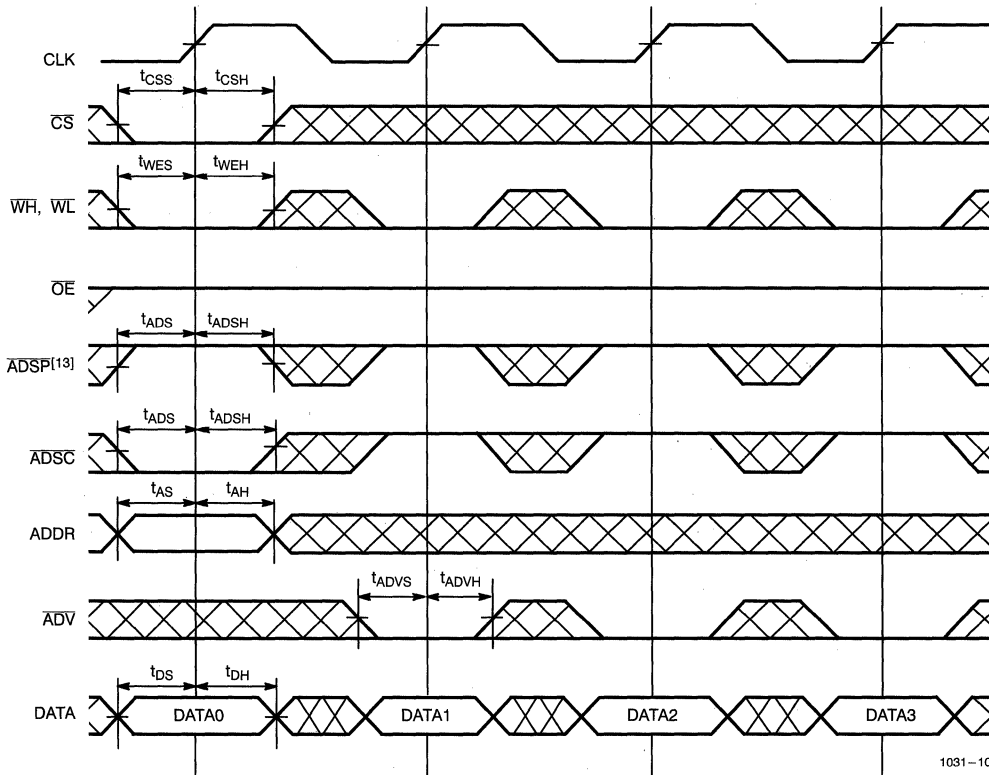
 12. $\overline{\text{OE}}$ is LOW throughout this operation.

 13. If $\overline{\text{ADSP}}$ is asserted while $\overline{\text{CS}}$ is HIGH, $\overline{\text{ADSP}}$ will be ignored.

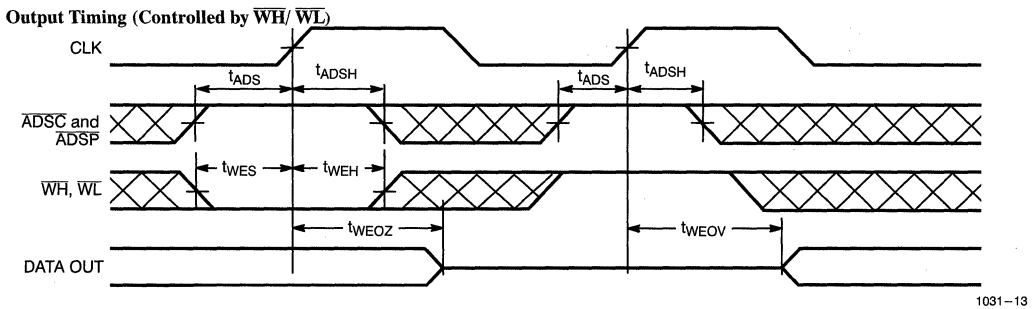
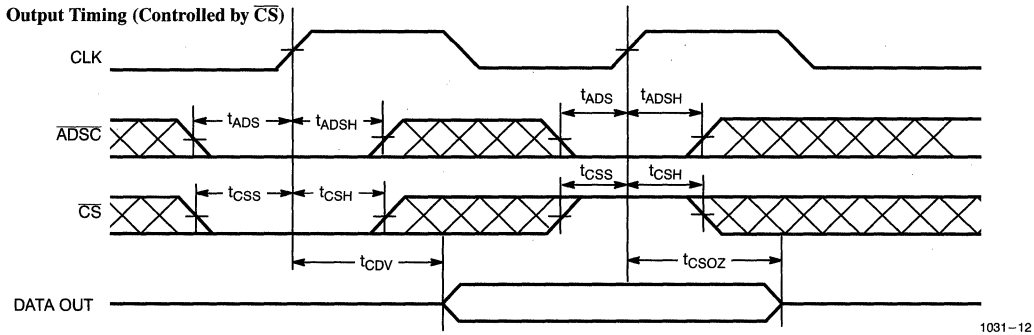
 14. $\overline{\text{ADSP}}$ has no effect on $\overline{\text{ADV}}$, $\overline{\text{WL}}$, and $\overline{\text{WH}}$ if $\overline{\text{CS}}$ is HIGH.

Switching Waveforms (continued)
Output (Controlled by \overline{OE})


1031-9

Write Burst Timing: Write Initiated by \overline{ADSC}


1031-10

Switching Waveforms (continued)

Truth Table

Input						Address	Operation
\overline{CS}	\overline{ADSP}	\overline{ADSC}	\overline{ADV}	\overline{WH} or \overline{WL}	CLK		
H	X	L	X	X	L→H	N/A	Chip deselected
H	L	H	H	H	L→H	Same address as previous cycle	Read cycle (\overline{ADSP} ignored)
H	L	H	L	H	L→H	Incremented burst address	Read cycle, in burst sequence (\overline{ADSP} ignored)
H	L	H	H	L	L→H	Same address as previous cycle	Write cycle (\overline{ADSP} ignored)
H	L	H	L	L	L→H	Incremented burst address	Write cycle, in burst sequence (\overline{ADSP} ignored)
L	L	X	X	X	L→H	External	Read cycle, begin burst
L	H	L	X	H	L→H	External	Read cycle, begin burst
L	H	L	X	L	L→H	External	Write cycle, begin burst
X	H	H	L	L	L→H	Incremented burst address	Write cycle, in burst sequence
X	H	H	L	H	L→H	Incremented burst address	Read cycle, in burst sequence
X	H	H	H	L	L→H	Same address as previous cycle	Write cycle
X	H	H	H	H	L→H	Same address as previous cycle	Read cycle



128K x 9 Static RAM

Features

- High speed
— $t_{AA} = 12$ ns
- CMOS for optimum speed/power
- Low active power
— 1020 mW
- Low standby power
— 250 mW
- 2.0V data retention
— 100 μ W
- Available in plastic 32-pin 400-mil SOJ
- Automatic power-down when deselected
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} options

Functional Description

The CY7C1088 is a high-performance CMOS static RAM organized as 131,072 words by 9 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}_1), an active HIGH chip enable (CE_2), an active LOW output enable (\overline{OE}), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

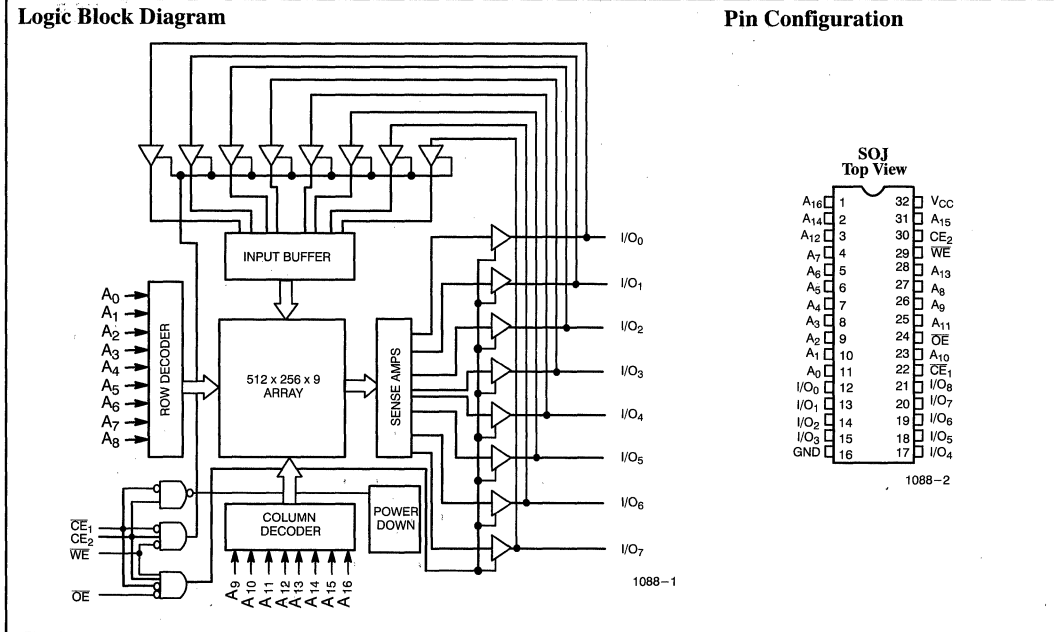
Writing to the device is accomplished by taking chip enable one (\overline{CE}_1) and write enable (\overline{WE}) inputs LOW and chip enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written

into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable one (\overline{CE}_1) and output enable (\overline{OE}) LOW while forcing write enable (\overline{WE}) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH or CE_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW).

The CY7C1088 is available in standard 32-pin 400-mil-wide SOJs.



Selection Guide

		7C1088-12	7C1088-15	7C1088-20	7C1088-25
Maximum Access Time (NS)		12	15	20	25
Maximum Operating Current (mA)	Commercial	185	170	155	145
	Military		180	170	160
Maximum Standby Current (mA)	Commercial	45	40	30	30
	Military		40	30	30

Functional Description (continued)
Single Write Accesses Initiated by ADSP

This access is initiated when the following conditions are satisfied at clock rise: (1) \overline{CS} is LOW and (2) ADSP is LOW. ADSP-triggered write cycles are completed in two clock periods. The address at A_0 through A_{15} is loaded into the address register and address advancement logic and delivered to the RAM core. The write signal is ignored in this cycle because the cache tag or other external logic uses this clock period to perform address comparisons or protection checks. If the write is allowed to proceed, the write input to the CY7C1331 and CY7C1332 will be pulled LOW before the next clock rise. ADSP is ignored if \overline{CS} is HIGH.

If \overline{WH} , \overline{WL} , or both are LOW at the next clock rise, information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. \overline{WL} controls the writing of $DQ_0 - DQ_7$ and DP_0 while \overline{WH} controls the writing of $DQ_8 - DQ_{15}$ and DP_1 . Because the CY7C1331 and CY7C1332 are common-I/O devices, the output enable signal (\overline{OE}) must be deasserted before data from the CPU is delivered to $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$. As a safety precaution, the appropriate data lines are three-stated in the cycle where \overline{WH} , \overline{WL} , or both are sampled LOW, regardless of the state of the \overline{OE} input.

Single Write Accesses Initiated by ADSC

This write access is initiated when the following conditions are satisfied at rising edge of the clock: (1) \overline{CS} is LOW, (2) ADSC is LOW, and (3) \overline{WH} or \overline{WL} are LOW. ADSC triggered accesses are completed in a single clock cycle.

The address at A_0 through A_{15} is loaded into the address register and address advancement logic and delivered to the RAM core. Information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. \overline{WL} controls the writing of $DQ_0 - DQ_7$ and DP_0 while \overline{WH} controls the writing of $DQ_8 - DQ_{15}$ and DP_1 . Since the CY7C1331 and the CY7C1332 are common-I/O devices, the output enable signal (\overline{OE}) must be deasserted before data from the cache controller is delivered to the data lines. As a safety precaution, the appropriate data lines are three-stated in the cycle where \overline{WH} , \overline{WL} , or both are sampled LOW, regardless of the state of the \overline{OE} input.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) \overline{CS} is LOW, (2) ADSP or ADSC is LOW, and (3) \overline{WH} and \overline{WL} are HIGH. The address at A_0 through A_{15} is stored into the address advancement logic and delivered to the RAM core. If the output enable (\overline{OE}) signal is asserted (LOW), data will be available at the data outputs a maximum of 8.5 ns after clock rise.

Burst Sequences

The CY7C1331 provides a 2-bit wraparound counter, fed by pins $A_0 - A_1$, that implements the Intel 80486 and Pentium processor address burst sequence (see Table 1). Note that the burst sequence depends on the first burst address.

Table 1. Counter Implementation for the Intel Pentium/80486 Processor's Sequence

First Address	Second Address	Third Address	Fourth Address
$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

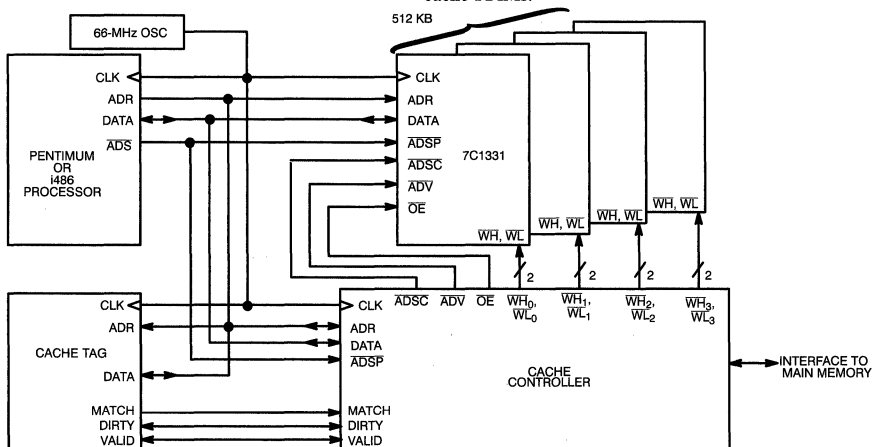
The CY7C1332 provides a two-bit wraparound counter, fed by pins $A_0 - A_1$, that implements a linear address burst sequence (see Table 2).

Table 2. Counter Implementation for a Linear Sequence

First Address	Second Address	Third Address	Fourth Address
$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Application Example

Figure 1 shows a 512-Kbyte secondary cache for a hypothetical 3.3V, 66-MHz Pentium or i486 processor using four CY7C1331 cache RAMs.


Figure 1. Cache Using Four CY7C1331s

1331-3

Pin Descriptions (continued)

Signal Name	I/O	Description
\overline{OE}	I	Output enable. This signal is an asynchronous input that controls the direction of the data I/O pins. If \overline{OE} is asserted (LOW), the data pins are outputs, and the SRAM can be read (as long as \overline{CS} is asserted when it was sampled at the beginning of the cycle). If \overline{OE} is deasserted (HIGH), the data I/O pins will be three-stated, functioning as inputs, and the SRAM can be written.

Bidirectional Signals

DQ₁₅-DQ₀ I/O Sixteen bidirectional data I/O lines. DQ₁₅ - DQ₈ are inputs to and outputs from the high-order half of the RAM array, while DQ₇ - DQ₀ are inputs to and outputs from the low-order half of the RAM array. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they carry the data read from the selected location in the RAM array. The direction of the data pins is controlled by \overline{OE} : when \overline{OE} is high, the data pins are three-stated and can be used as inputs; when \overline{OE} is low, the data pins are driven by the output buffers and are outputs. DQ₁₅ - DQ₈ and DQ₇ - DQ₀ are also three-stated when \overline{WH} and \overline{WL} , respectively, are sampled LOW at clock rise.

Signal Name	I/O	Description
DP ₁ -DP ₀	I/O	Two bidirectional data I/O lines. These operate in exactly the same manner as DQ ₁₅ - DQ ₀ , but are named differently because their primary purpose is to store parity bits, while the DQs' primary purpose is to store ordinary data bits. DP ₁ is an input to and an output from the high-order half of the RAM array, while DP ₀ is an input to and an output from the lower-order half of the RAM array.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with
 Power Applied -55°C to +125°C
 Supply Voltage on V_{CC} Relative to GND -0.5V to +3.6V
 DC Voltage Applied to Outputs
 in High Z State^[2] -0.5V to V_{CC} + 0.3V
 DC Input Voltage^[2] -0.5V to V_{CC} + 0.3V
 Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)
 Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature ^[3]	V _{CC} , V _{CCQ}
Com'l	0°C to +70°C	3.3V ± 0.3V
Mil	-55°C to +125°C	3.3V ± 0.3V

Electrical Characteristics Over the Operating Range^[4]

Parameter	Description	Test Conditions	7C1331-8 7C1332-8		7C1331-10 7C1332-10		7C1331-12 7C1332-12		Unit
			Min.	Max.	Min.	Max.	Min.	Min.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -2.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3V	2.0	V _{CC} + 0.3V	2.0	V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage ^[2]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _X	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND		-300		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{out} = 0mA, f = f _{MAX} = 1/t _{CYC}	Com'l	200		200		170	mA
			Mil					200	

Notes:

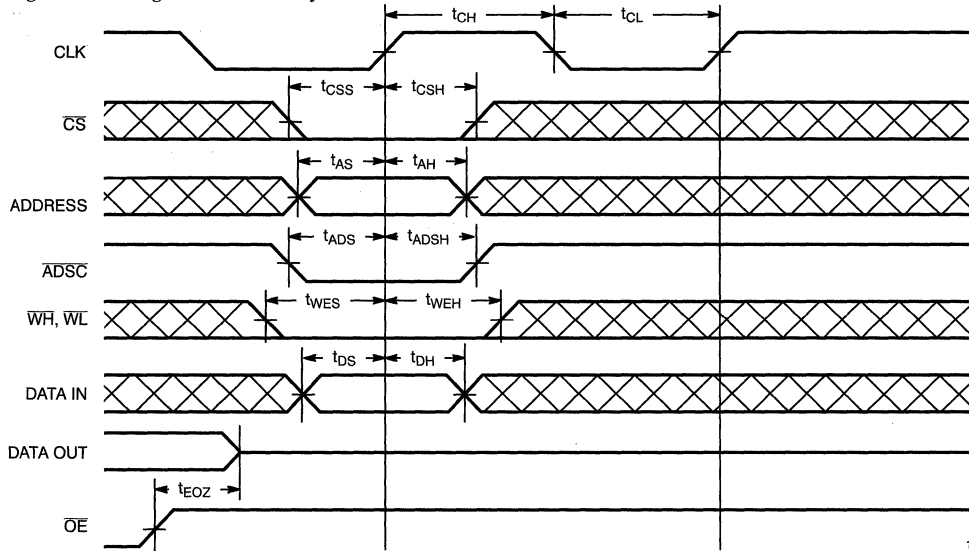
- Minimum voltage equals -2.0V for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Switching Characteristics Over the Operating Range^[8]

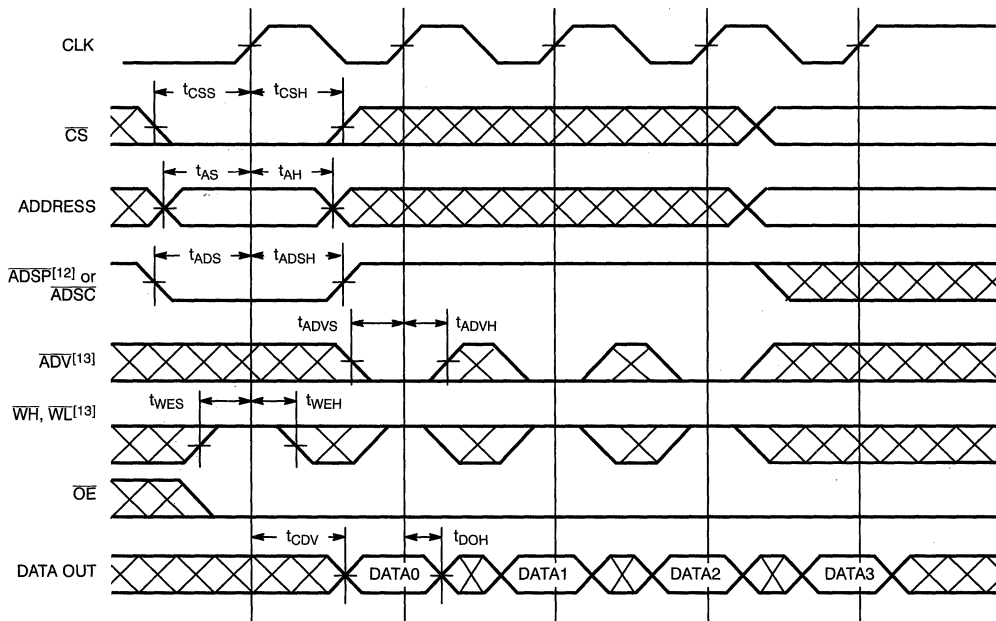
Parameter	Description	7C1331-8 7C1332-8		7C1331-10 7C1332-10		7C1331-12 7C1332-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC}	Clock Cycle Time	15		15		20		ns
t _{CH}	Clock HIGH	5		6		8		ns
t _{CL}	Clock LOW	5		6		8		ns
t _{AS}	Address Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t _{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		ns
t _{CDV}	Data Output Valid After CLK Rise		8.5		10		12	ns
t _{DOH}	Data Output Hold After CLK Rise	3		3		3		ns
t _{ADS}	\overline{ADSP} , \overline{ADSC} Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t _{ADSH}	\overline{ADSP} , \overline{ADSC} Hold After CLK Rise	0.5		0.5		0.5		ns
t _{WES}	\overline{WH} , \overline{WL} Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t _{WEH}	\overline{WH} , \overline{WL} Hold After CLK Rise	0.5		0.5		0.5		ns
t _{ADVS}	\overline{ADV} Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t _{ADVH}	\overline{ADV} Hold After CLK Rise	0.5		0.5		0.5		ns
t _{DS}	Data Input Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t _{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		ns
t _{CSS}	Chip Select Set-Up	2.5		2.5		2.5		ns
t _{CSH}	Chip Select Hold After CLK Rise	0.5		0.5		0.5		ns
t _{CSOZ}	Chip Select Sampled to Output High Z ^[9]	2	6	2	6	2	7	ns
t _{EOZ}	\overline{OE} HIGH to Output High Z ^[9]	2	6	2	6	2	7	ns
t _{EOV}	\overline{OE} LOW to Output Valid		5		5		6	ns
t _{WEOZ}	\overline{WH} or \overline{WL} Sampled LOW to Output High Z ^[9,10]		5		6		7	ns
t _{WEOV}	\overline{WH} or \overline{WL} Sampled HIGH to Output Valid ^[10]		8.5		10		12	ns

Notes:

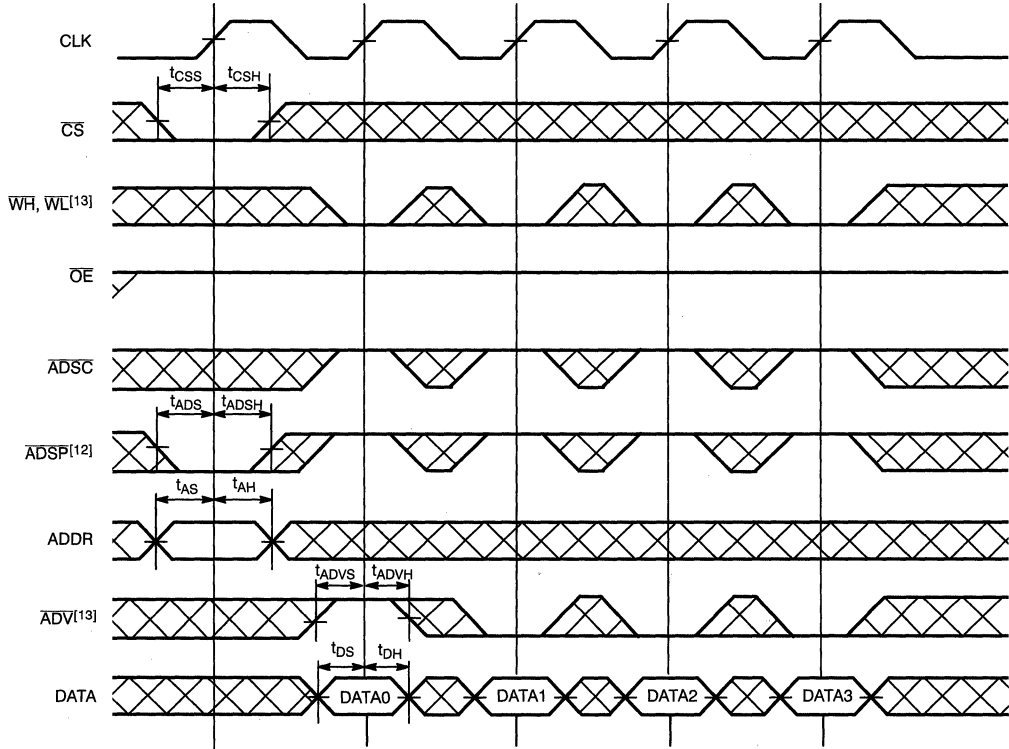
8. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance as shown in (a) and (b) of AC Test Loads.
9. t_{CSOZ}, t_{EOZ}, and t_{WEOZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
10. At any given voltage and temperature, t_{WEOZ} min. is less than t_{WEOV} min.

Switching Waveforms (continued)
Single Write Timing: Write Initiated by $\overline{\text{ADSC}}$


1331-8

Burst Read Sequence with Four Accesses


1331-9

Switching Waveforms (continued)
Write Burst Timing: Write Initiated by ADSP


1331-12

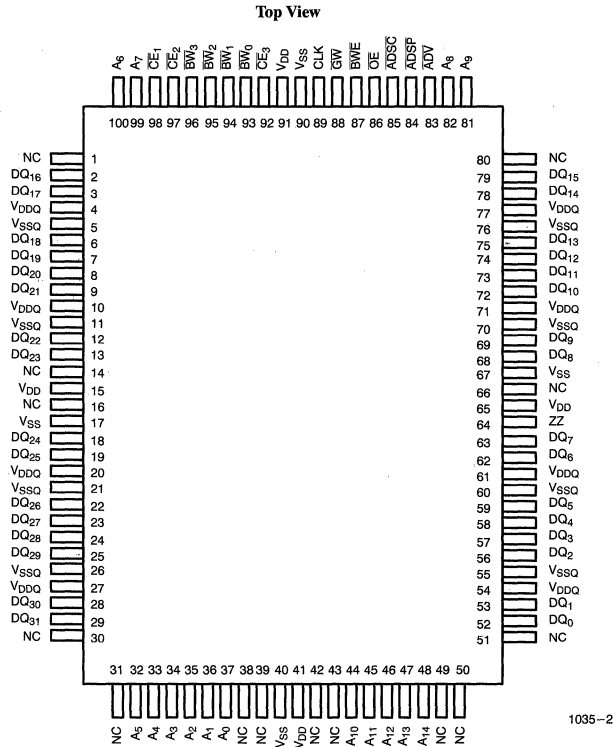


Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8.5	CY7C1331-8JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1331-8NC	N52	52-Lead Plastic Quad Flatpack	
10	CY7C1331-10JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1331-10NC	N52	52-Lead Plastic Quad Flatpack	
12	CY7C1331-12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1331-12NC	N52	52-Lead Plastic Quad Flatpack	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8.5	CY7C1332-8JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1332-8NC	N52	52-Lead Plastic Quad Flatpack	
10	CY7C1332-10JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1332-10NC	N52	52-Lead Plastic Quad Flatpack	
12	CY7C1332-12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1332-12NC	N52	52-Lead Plastic Quad Flatpack	

Document #: 38-00223-B

Pin Configuration

Selection Guide

	7C1335-7 7C1336-7	7C1335-8 7C1336-8	7C1335-10 7C1336-10
Maximum Access Time (ns) (0-pF load)	7.0	8.5	10
Maximum Operating Current (mA)	Commercial	180	170

32K x 8 3.3V Static RAM
Features

- Single 3.3V power supply
- Ideal for low-voltage cache memory applications
- High speed
 - 12 ns
- Low active power
 - 255 mW
- Low standby power
 - 90 mW
- 2.0V data retention
 - 100 μ W
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Plastic DIP, SOJ, and TSOP packaging

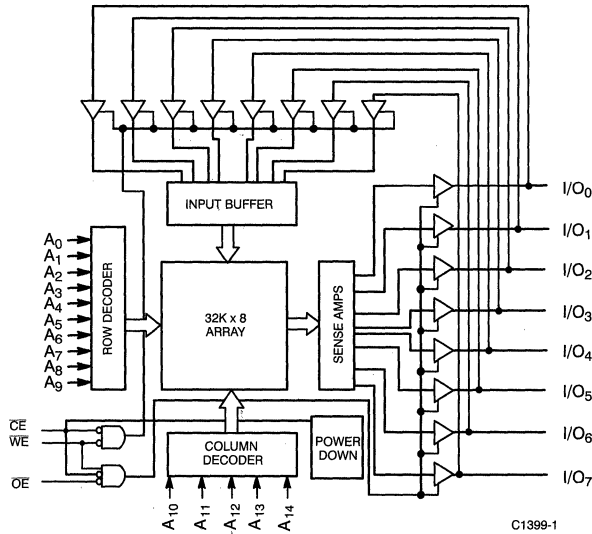
Functional Description

The CY7C1399 is a high-performance 3.3V CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}) and active LOW output enable (\overline{OE}) and three-state drivers. The device has an automatic power-down feature, reducing the power consumption by more than 60% when deselected.

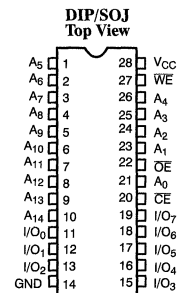
An active LOW write enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE} and \overline{WE} inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the

address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE} and \overline{OE} active LOW, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH. The CY7C1399 is available in standard 300-mil-wide DIP and SOJ packages. A die coat is used to ensure alpha immunity.

Logic Block Diagram


C1399-1

Pin Configurations


C1399-2

Selection Guide

	7C1399-12	7C1399-15	7C1399-20	7C1399-25	7C1399-35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	60	55	50	45	40
Maximum Standby Current (mA)	5	5	5	5	5

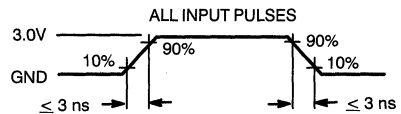
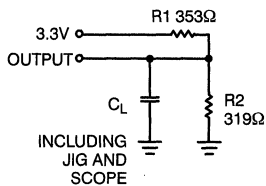
Shaded area contains advanced information.

Electrical Characteristics Over the Operating Range^[2] (continued)

Parameter	Description	Test Conditions	7C1399-25		7C1399-35		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -2.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3V	2.0	V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage ^[2]		-0.3	0.8	-0.3	0.8	V
I _{IX}	Input Load Current		-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}		45		40	mA
I _{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V _{CC} , $\overline{CE}_1 \geq V_{IH}$ or CE ₂ ≤ V _{IL} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		5		5	mA
I _{SB2}	Automatic CE Power-Down Current — TTL Inputs	Max. V _{CC} , $\overline{CE}_1 \geq V_{CC} - 0.3V$ or CE ₂ ≤ 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0		50		50	μA

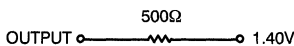
Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN} : Addresses	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V	5	pF
C _{IN} : Controls			6	pF
C _{OUT}	Output Capacitance		6	pF

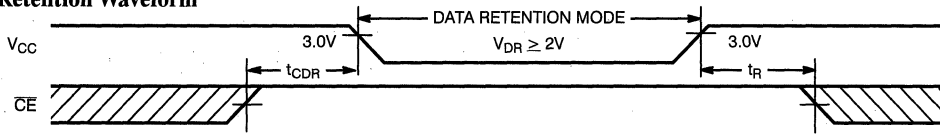
AC Test Loads and Waveforms


C1399-4

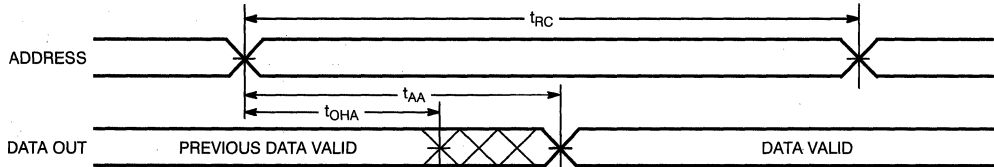
Equivalent to: THÉVENIN EQUIVALENT


Note:

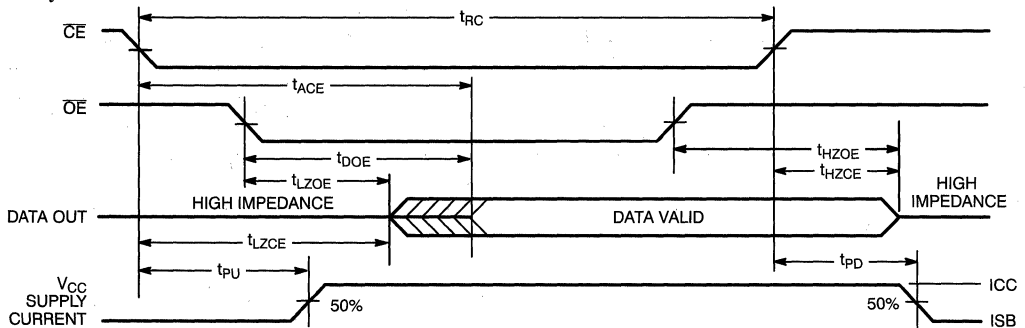
- Tested initially and after any design or process changes that may affect these parameters.

Data Retention Waveform


C1399-5

Switching Waveforms
Read Cycle No. 1^[11, 12]


C1399-6

Read Cycle No. 2^[12, 13]


C1399-7

Notes:

 11. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
 12. \overline{WE} is HIGH for read cycle.

 13. Address valid prior to or coincident with \overline{CE} transition LOW.



Truth Table

CE	WE	OE	Input/Output	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (ISB)
L	H	L	Data Out	Read	Active (ICC)
L	L	X	Data In	Write	Active (ICC)
L	H	H	High Z	Deselect, Output Disabled	Active (ICC)

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1399-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1399-12VC	V21	28-Lead Molded SOJ	
	CY7C1399-12ZC	Z28	28-Lead Thin Small Outline Package	
15	CY7C1399-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1399-15VC	V21	28-Lead Molded SOJ	
	CY7C1399-15ZC	Z28	28-Lead Thin Small Outline Package	
20	CY7C1399-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1399-20VC	V21	28-Lead Molded SOJ	
	CY7C1399-20ZC	Z28	28-Lead Thin Small Outline Package	
25	CY7C1399-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1399-25VC	V21	28-Lead Molded SOJ	
	CY7C1399-25ZC	Z28	28-Lead Thin Small Outline Package	
35	CY7C1399-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1399-35VC	V21	28-Lead Molded SOJ	
	CY7C1399-35ZC	Z28	28-Lead Thin Small Outline Package	

Shaded area contains advanced information.

**MILITARY SPECIFICATIONS
Group A Subgroup Testing**

DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{Ix}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

Document #: 38-00222-C

Modules	Page Number
Custom Module Capabilities	3-1
Device	Description
CYM1420	128K x 8 Static RAM Module 3-5
CYM1441	256K x 8 Static RAM Module 3-11
CYM1464	512K x 8 Static RAM Module 3-16
CYM1465	512K x 8 SRAM Module 3-22
CYM1471	1024K x 8 SRAM Module 3-28
CYM1481	2048K x 8 SRAM Module 3-28
CYM1622	64K x 16 Static RAM Module 3-34
CYM1720	32K x 24 Static RAM Module 3-39
CYM1730	64K x 24 Static RAM Module 3-44
CYM1821	16K x 32 Static RAM Module 3-49
CYM1828	32K x 32 Static RAM Module 3-55
CYM1831	64K x 32 Static RAM Module 3-62
CYM1832	64K x 32 Static RAM Module 3-67
CYM1836	128K x 32 Static RAM Module 3-72
CYM1838	128K x 32 Static RAM Module 3-77
CYM1840	256K x 32 Static RAM Module 3-82
CYM1841	256K x 32 Static RAM Module 3-88
CYM1841A	256K x 32 Static RAM Module 3-88
CYM1846	512K x 32 Static RAM Module 3-97
CYM1851	1,024K x 32 Static RAM Module 3-102
CYM7232	DRAM Accelerator Module 3-107
CYM7264	DRAM Accelerator Module 3-107
CYM7420	82420 PCIsset-Compatible Level II Cache Module 3-108
CYM7421	82420 PCIsset-Compatible Level II Cache Module 3-108
CYM7424	128K Cache Module for the Intel™ 82420EX PCIsset 3-109
CYM7425	256K Cache Module for the Intel 82420EX PCIsset 3-109
CYM7427	82420 PCIsset-Compatible Level II Cache Module Family 3-114
CYM7428	82420 PCIsset-Compatible Level II Cache Module Family 3-114
CYM7432	256K Pentium™ -Compatible Cache Module 3-115
CYM7450	128K Cache Module for VLSI VL82C483 Chip Set 3-118
CYM7451	256K Cache Module for VLSI VL82C483 Chip Set 3-118
CYM7490	i486™ Level II Cache Module 3-119
CYM7491	i486 Level II Cache Module 3-119
CYM7492	i486 Level II Cache Module 3-119
CYM74AP54	Intel 82430NX Chip Set Level II Cache Module 3-120
CYM74SP54	Intel 82430NX Chip Set Level II Cache Module 3-120
CYM74SP55	Intel 82430NX Chip Set Level II Cache Module 3-120
CYM74A430	Intel 82430FX PCIsset Level II Cache Module 3-125
CYM74S430	Intel 82430FX PCIsset Level II Cache Module 3-125
CYM74S431	Intel 82430FX PCIsset Level II Cache Module 3-125
CYM74A550	OPTi Viper™ Chip Set Level II Cache Module 3-130
CYM74A551	OPTi Viper Chip Set Level II Cache Module 3-130
CYM74S550	OPTi Viper Chip Set Level II Cache Module 3-130
CYM74S551	OPTi Viper Chip Set Level II Cache Module 3-130
CYM74A590	VLSI 82C590 Chip Set Level II Cache Module 3-135
CYM74S590	VLSI 82C590 Chip Set Level II Cache Module 3-135
CYM74S591	VLSI 82C590 Chip Set Level II Cache Module 3-135
CYM9230	82420 PCIsset-Compatible Level II Cache Module 3-140
CYM9231	82420 PCIsset-Compatible Level II Cache Module 3-140
CYM9236	128K Cache Module for the UMC491 Chip Set 3-141
CYM9237	256K Cache Module for the UMC491 Chip Set 3-141

VDIP

The VDIP, or vertical dual in-line pin package, is a vertically mounted module with two rows of pins on 100-mil centers. Row to row spacing is 100 mils, with pins of the two rows aligned directly across from one another. The dual row of pins allows a higher connection density than that of the SIP while maintaining 100-mil minimum spacing between any adjacent pins. VDIP may be either plastic or ceramic. The VDIP is useful in large pin count devices where the host board is designed with through-hole design rules.

DIP

The DIP, or dual in-line pin module, is a low-profile package with excellent mechanical ruggedness. The ceramic DIP is ideally suited for military applications. Plastic DIPs are often used when a low vertical profile is required. In some cases, the DIP device is intended to have an identical footprint and similar form factor to standard integrated circuit components and can provide larger memory capacity in the same footprint.

PGA

The PGA, or pin grid array, has an array of pins that are perpendicular to the package plane. These pins are arranged in a matrix on a

100-mil grid. Most of the matrix is filled with pins except for a central square that is normally devoid of pins.

QUIP

The QUIP, or quad in-line pin package, is very similar to the DIP package except that there is a dual row of pins along the package edge. In-row and row-to-row pin spacing is 100 mils with pins in adjacent rows aligned directly across from one another. The QUIP is a low-profile package with excellent mechanical ruggedness, with the added advantage of higher pin density for the same package length.

QFP

The QFP, or quad flat pack, is a surface-mounted module. Gull wing pins extend out from the square package on all four sides and are formed to be coplanar with the package bottom. Lead pitches are typically 50 mils or smaller.

Package Summary

Table 1 summarizes the various characteristics of the packages discussed above.

Table 1. Package Types

Package Type	Typical Pin Count		Typical Height ^[1]		Mil ^[2]	Advantages	Disadvantages	Board Space (sq. in.) ^[3]	
	Min.	Max.	Min.	Max.				FR4	Cer
SIP	24	50	0.5	0.9	N	Vertical orientation. FR4 or ceramic technology.	Limited pin count.	1.2	0.9
FSIP	24	50	0.2	0.4	N	Very low profile. Mechanical stability. FR4 or ceramic technology.	Lower density due to horizontal orientation.	2.7	2.4
ZIP	24	100	0.5	0.9	N	Vertical orientation. JEDEC-standard pinouts. Pinout compatible with SIMM.		1.2	N/A
SIMM	24	100	0.5	0.9	N	Vertical orientation. Socket mounting. Pinout compatible with ZIP.		1.2	N/A
VDIP	36	104	0.5	0.95	Y	Vertical orientation.		1.2	0.9
DIP	24	60	0.17	0.37	Y	Low profile. Excellent mechanical ruggedness.	Horizontal orientation.	2.9	2.9
QUIP	48	200			Y	Low profile. Excellent mechanical ruggedness. Increased number of pins.	Horizontal orientation.	2.9	2.9
QFP	68	144			Y	Surface mount. Low profile. Excellent mechanical ruggedness. Large number of pins in small area.	Surface-mount technology required. Horizontal orientation. Components on one side only.	3.1	3.1
PGA	68	144			Y	Large number of pins in through-hole technology. Low profile. Excellent mechanical ruggedness.	Multilayer boards. Horizontal orientation. Components on one side only.	2.9	2.9

Notes:

1. Minimum and maximum height are given in inches.
2. The Mil entry contains a Y(es) or N(o) indicating if the package type is suitable for military applications.
3. Board space roughly quantifies the main board area, in square inches, taken up by the module when the module contains eight, 28-pin components.

Custom Module Development Flow (continued)

During simulation, several types of analyses are performed. A function simulation is used to ensure that the module's logic is designed properly. Timing simulation is run to verify that the module will function when subjected to the worst-case timing delays of the components. Finally, thermal analysis may be performed to determine the thermal characteristics of the module.

The layout of the module is also netlist driven. An autorouter may be used, depending on the complexity and density of the module. Design rule checks are run to ensure that the layout does not violate any electrical or mechanical design rules. Finally, the layout output is used to generate the module substrate.

The layout output is also used to drive the pick and place equipment. This ensures consistency between design and manufacturing. While the module prototypes are being assembled, the test program is generated and the test fixture is constructed. Test program generation is largely automated, using as inputs the simulation outputs and pre-defined test program subroutines for common configurations.

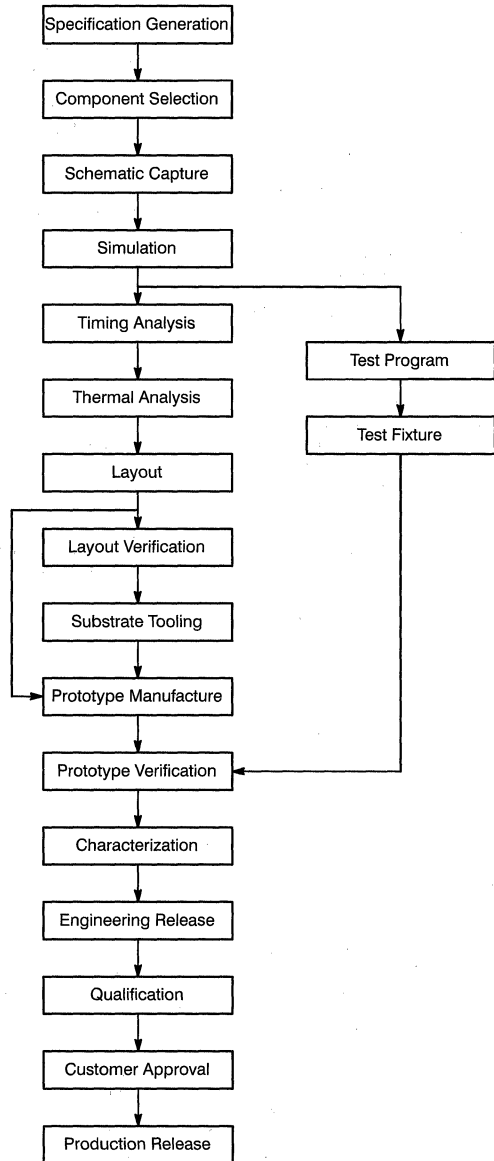
Once prototypes have been generated, the standard release procedure is initiated. This procedure includes steps such as bench testing, module characterization and qualification, and fine tuning of the test program. Following customer approval of the module, it is released to production.

Quoting Information

In order to prepare a quotation or proposal, we need as much as possible of the following information:

- Circuit schematic
- Functional description
- Mechanical dimensions required
- Speed and power requirements
- Prototype and production deadlines
- Production quantity estimates
- An engineering contact to answer questions

Once the above information is received, a budgetary quotation will typically be provided within one to two weeks.


Figure 1. Custom Module Flow

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature	- 65°C to +150°C
Ambient Temperature with ..	- 10°C to +85°C (Commercial)
Supply Voltage to Ground Potential	- 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	- 0.5V to +7.0V
DC Input Voltage	- 0.5V to +7.0V

Output Current into Outputs (LOW) 20 mA

Operating Range

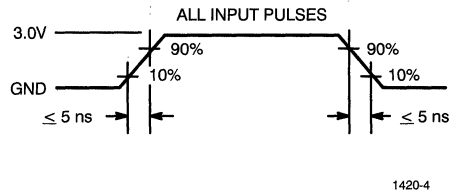
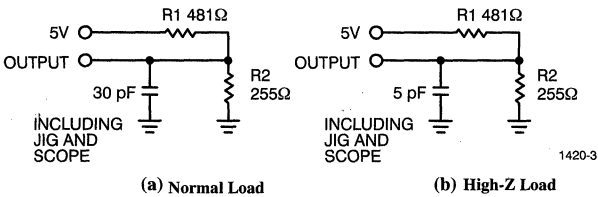
Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

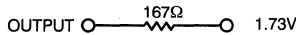
Parameters	Description	Test Conditions	Min.	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	V
V _{IL}	Input LOW Voltage		- 0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	- 10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	- 10	+10	μA
I _{OS}	Output Short Circuit Current ^[1, 2]	V _{CC} = Max., V _{OUT} = GND		- 300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, CS ≤ V _{IL}		210	mA
I _{SB1}	Automatic CS Power-Down Current ^[3]	V _{CC} = Max., CS ≥ V _{IH} , Min. Duty Cycle = 100%		140	mA
I _{SB2}	Automatic CS Power-Down Current ^[3]	V _{CC} = Max., CS ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		80	mA

Capacitance^[2]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	35	pF
C _{OUT}	Output Capacitance		40	pF

AC Test Loads and Waveforms


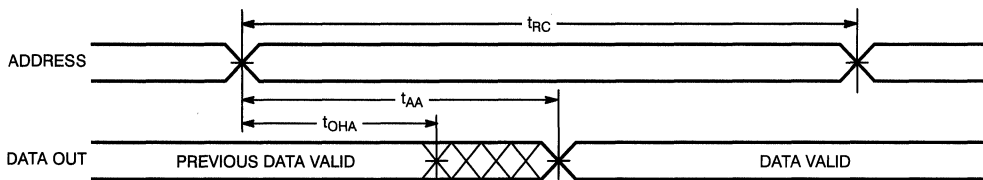
Equivalent to: THÉVENIN EQUIVALENT


Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested on a sample basis.
- A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

Switching Characteristics Over the Operating Range (continued)^[4]

Parameters	Description	1420-35		1420-45		1420-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	\overline{CS} LOW to Data Valid		35		45		55	ns
t_{DOE}	\overline{OE} LOW to Data Valid		18		25		30	ns
t_{LZOE}	\overline{OE} LOW to Low Z	0		0		0		ns
t_{HZOE}	\overline{OE} HIGH to High Z		20		20		25	ns
t_{LZCS}	\overline{CS} LOW to Low Z ^[5]	3		5		5		ns
t_{HZCS}	\overline{CS} HIGH to High Z ^[5, 6]		20		20		25	ns
WRITE CYCLE^[7]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCS}	\overline{CS} LOW to Write End	30		40		45		ns
t_{AW}	Address Set-Up to Write End	30		40		45		ns
t_{HA}	Address Hold from Write End	5		5		5		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		ns
t_{PWE}	\overline{WE} Pulse Width	25		25		30		ns
t_{SD}	Data Set-Up to Write End	18		20		25		ns
t_{HD}	Data Hold from Write End	3		5		5		ns
t_{LZWE}	\overline{WE} HIGH to Low Z	5		5		5		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[6]	0	15	0	15	0	25	ns

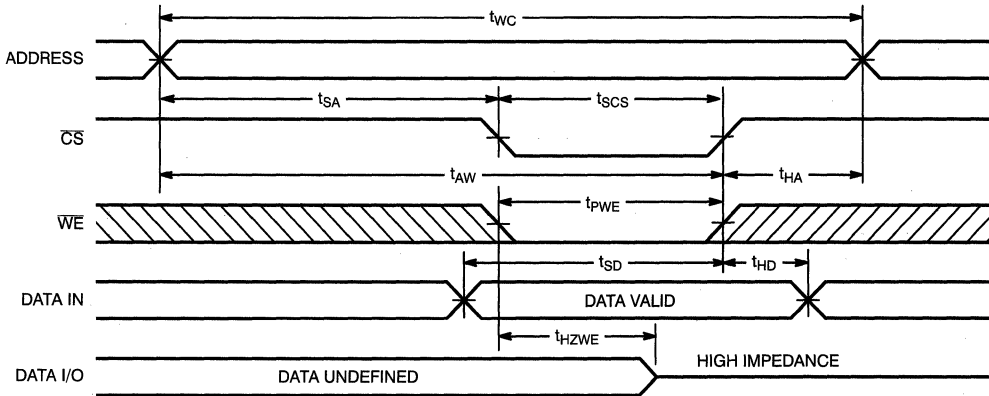
Switching Waveforms
Read Cycle No. 1^[8, 9]


1420-5

Notes:

 8. \overline{WE} is HIGH for read cycle.

 9. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.

Switching Waveforms (continued)
Write Cycle No. 2 ($\overline{\text{CS}}$ Controlled)^[7, 11, 12]


1420-8

Note:
 12. If $\overline{\text{CS}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.

Truth Table

CS	OE	WE	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	L	H	Data Out	Read
L	X	L	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CYM1420PD-20C	PD05	32-Pin DIP Module	Commercial
25	CYM1420PD-25C	PD05	32-Pin DIP Module	Commercial
30	CYM1420PD-30C	PD05	32-Pin DIP Module	Commercial
35	CYM1420PD-35C	PD05	32-Pin DIP Module	Commercial
45	CYM1420PD-45C	PD05	32-Pin DIP Module	Commercial
55	CYM1420PD-55C	PD05	32-Pin DIP Module	Commercial

Document #: 38-M-00001-E

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature -55°C to $+125^{\circ}\text{C}$
 Ambient Temperature with
 Power Applied -10°C to $+85^{\circ}\text{C}$
 Supply Voltage to Ground Potential -0.5V to $+7.0\text{V}$
 DC Voltage Applied to Outputs
 in High Z State -0.5V to $+7.0\text{V}$
 DC Input Voltage -0.5V to $+7.0\text{V}$

Operating Range

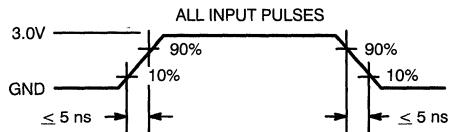
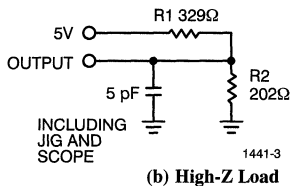
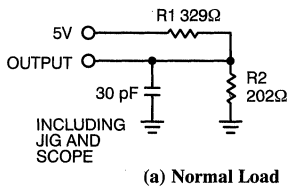
Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 12.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[1]		-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-80	+80	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-50	+50	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, $\overline{\text{CS}} \leq \text{V}_{\text{IL}}$		960	mA
I _{SB1}	Automatic CS Power-Down Current	Max. V _{CC} , $\overline{\text{CS}} \geq \text{V}_{\text{IH}}$, Min. Duty Cycle = 100%		320	mA
I _{SB2}	Automatic CS Power-Down Current	Max. V _{CC} , $\overline{\text{CS}} \geq \text{V}_{\text{CC}} - 0.2\text{V}$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V		160	mA

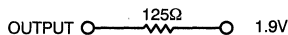
Capacitance^[2]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	60	pF
C _{OUT}	Output Capacitance		15	pF

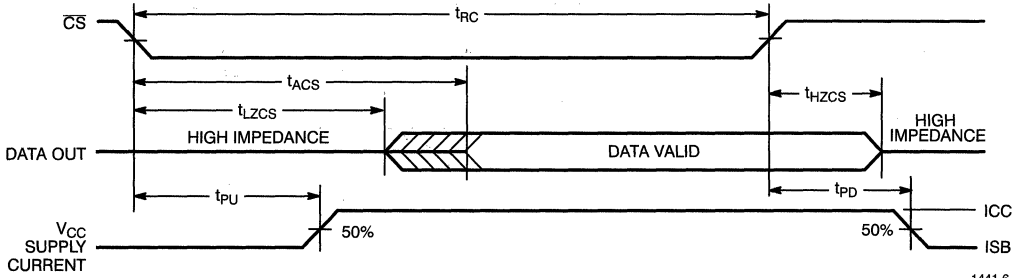
AC Test Loads and Waveforms


1441-4

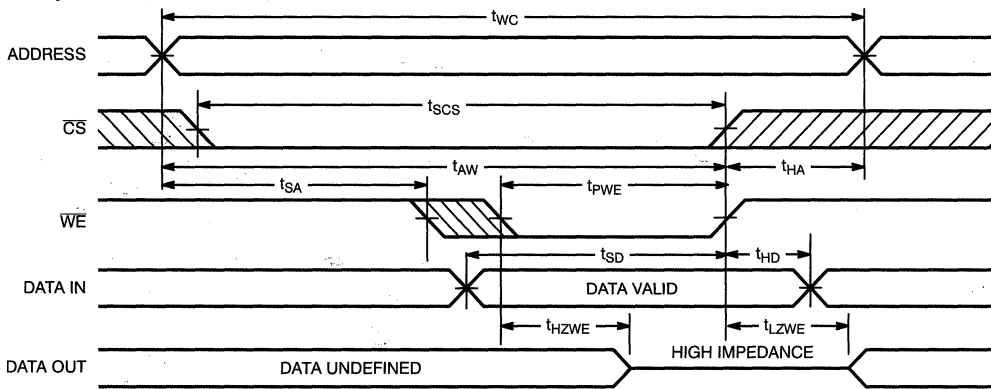
Equivalent to: THÉVENIN EQUIVALENT


Notes:

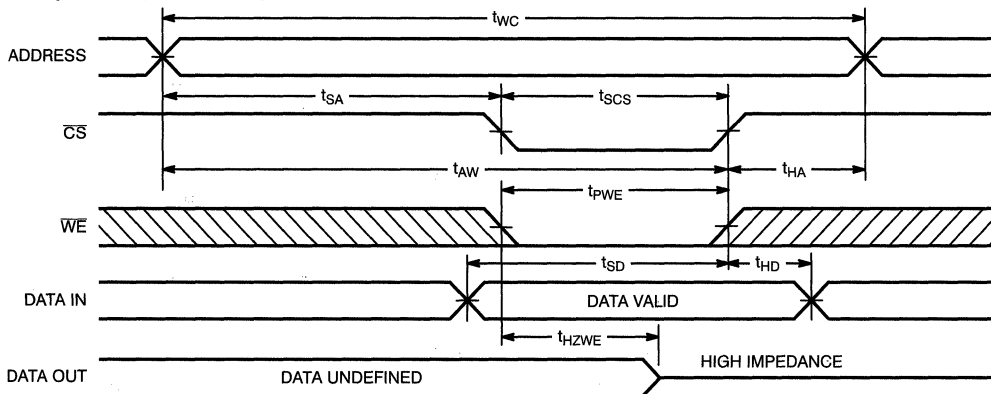
- V_{IN} (min.) = - 3.0V for pulse widths less than 20 ns.
- Tested on a sample basis.

Switching Waveforms (continued)
Read Cycle No. 2^[6, 8]


1441-6

Write Cycle No. 1 (\overline{WE} Controlled)^[5]


1441-7

Write Cycle No. 2 (\overline{CS} Controlled)^[5, 9]


1441-8

Notes:

 8. Address valid prior to or coincident with \overline{CS} transition LOW.

 9. If \overline{CS} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.



512K x 8 Static RAM Module

Features

- High-density 4-megabit SRAM module
- High-speed CMOS SRAMs
— Access time of 20 ns
- Low active power
— 1.93W (max.)
- JEDEC-compatible pinout
- 32-pin, 0.6-inch-wide DIP package
- TTL-compatible inputs and outputs
- Low profile
— Max. height of 0.34 inches

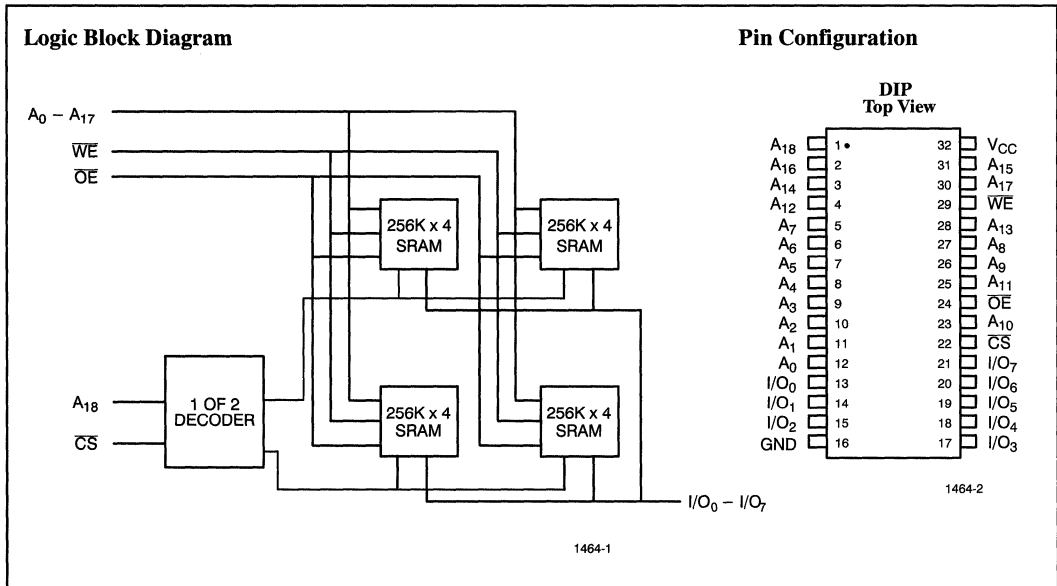
Functional Description

The CYM1464 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is constructed using four 256K x 4 static RAMs in SOJ packages mounted on an epoxy laminate substrate with pins.

Writing to the module is accomplished when the chip select (\overline{CS}) and write enable (\overline{WE}) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address

pins (A_0 through A_{18}). Reading the device is accomplished by taking chip select and output enable (\overline{OE}) LOW, while write enable (\overline{WE}) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{18}) will appear on the eight appropriate data input/output pins (I/O_0 through I/O_7).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH.



Selection Guide

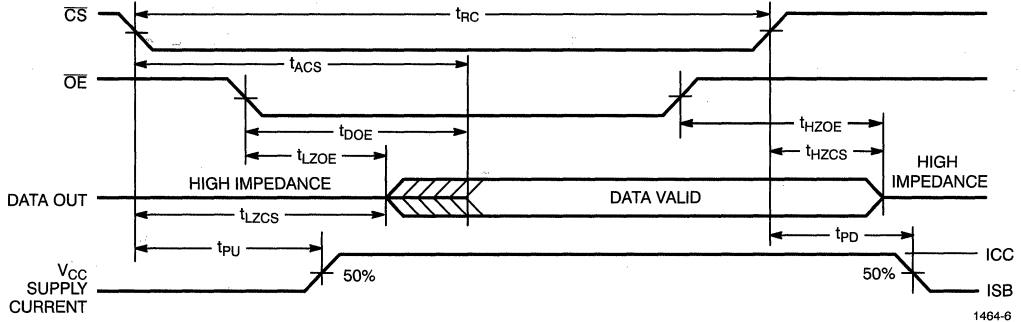
	1464-20	1464-22	1464-25	1464-30	1464-35	1464-45	1464-55
Maximum Access Time (ns)	20	22	25	30	35	45	55
Maximum Operating Current (mA)	350	350	350	300	300	300	300
Maximum Standby Current (mA)	240	240	240	240	240	240	240

Switching Characteristics Over the Operating Range^[3]

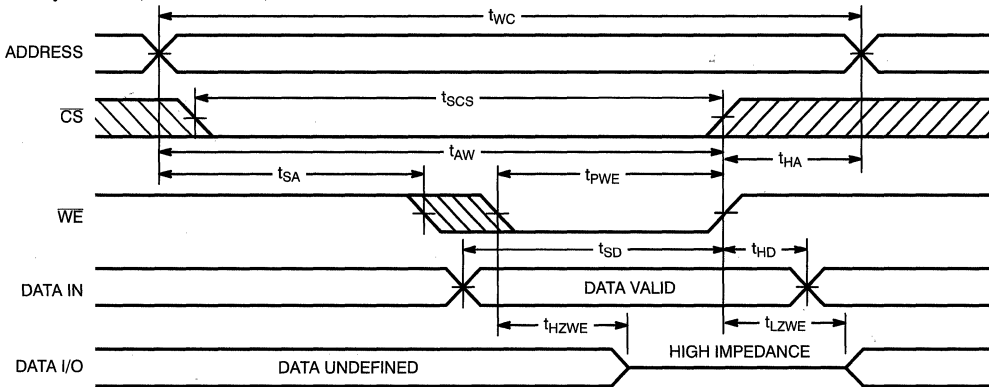
Parameter	Description	1464-20		1464-22		1464-25		1464-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t _{RC}	Read Cycle Time	20		22		25		30		ns
t _{AA}	Address to Data Valid		20		22		25		30	ns
t _{OHA}	Data Hold from Address Change	5		5		5		5		ns
t _{ACS}	$\overline{\text{CS}}$ LOW to Data Valid		20		22		25		30	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		13		13		15		15	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z	0		0		0		0		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z	0	10	0	10	0	10	0	10	ns
t _{LZCS}	$\overline{\text{CS}}$ LOW to Low Z	5		5		5		10		ns
t _{HZCS}	$\overline{\text{CS}}$ HIGH to High Z ^[4]	0	15	0	15	0	15	0	20	ns
WRITE CYCLE^[5]										
t _{WC}	Write Cycle Time	20		22		25		30		ns
t _{SCS}	$\overline{\text{CS}}$ LOW to Write End	15		17		20		25		ns
t _{AW}	Address Set-Up to Write End	15		15		20		25		ns
t _{HA}	Address Hold from Write End	3		3		3		3		ns
t _{SA}	Address Set-Up to Write Start	5		5		5		5		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	15		15		15		20		ns
t _{SD}	Data Set-Up to Write End	12		12		15		15		ns
t _{HD}	Data Hold from Write End	2		2		2		2		ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z	0		0		0		0		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[4]		15		15		15		15	ns

Notes:

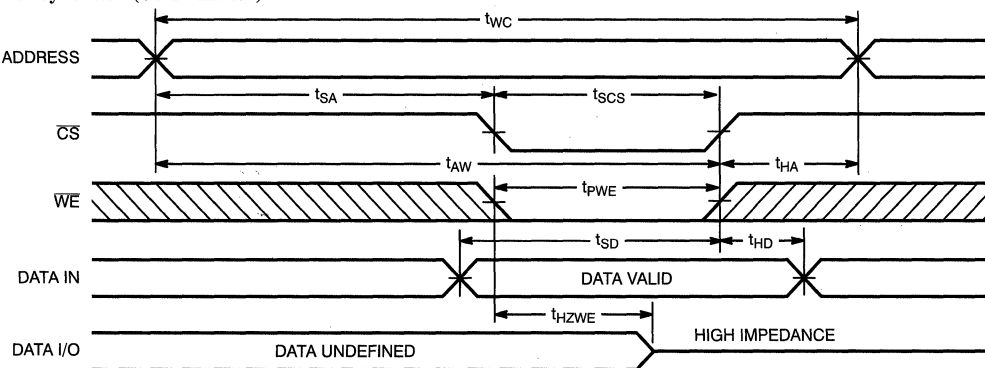
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{\text{CS}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms (continued)
Read Cycle No. 2^[6, 8]


1464-6

Write Cycle No. 1 (\overline{WE} Controlled)^[5]


1464-7

Write Cycle No. 2 (\overline{CS} Controlled)^[5, 9]


1464-8

Notes:

 8. Address valid prior to or coincident with \overline{CS} transition LOW.

 9. If \overline{CS} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.



512K x 8 SRAM Module

Features

- High-density 4-megabit SRAM module
- High-speed CMOS SRAMs
 - Access time of 70 ns
- Low active power
 - 605 mW (max.)
- 2V data retention (L Version)
- JEDEC-compatible pinout
- 32-pin, 0.6-inch-wide DIP package
- TTL-compatible inputs and outputs
- Low profile
 - Max. height of 0.27 in.

- Small PCB footprint
 - 0.98 sq. in.

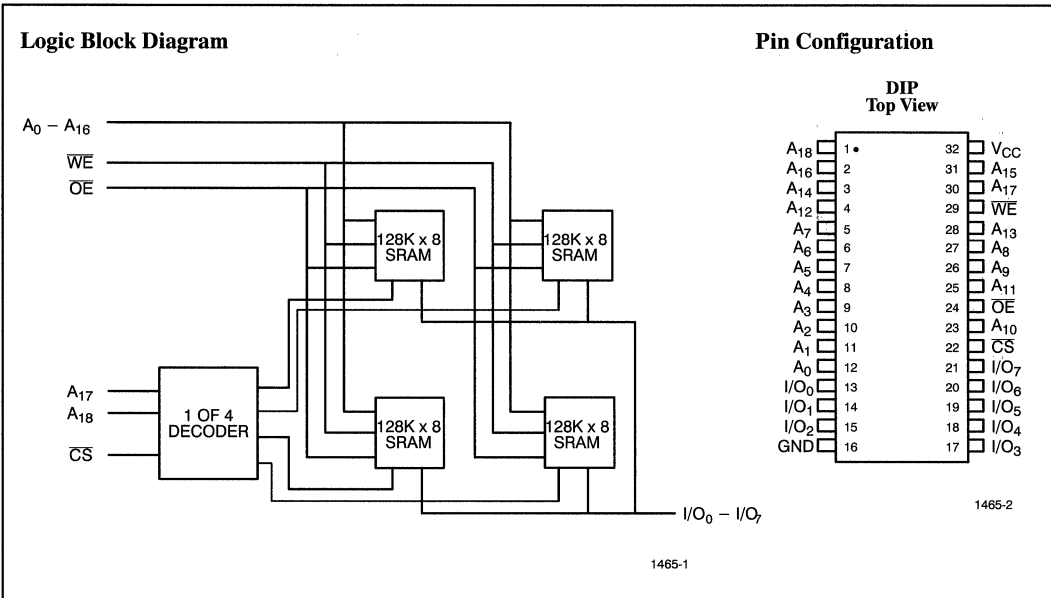
Functional Description

The CYM1465 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is constructed using four 128K x 8 RAMs mounted on a substrate with pins. A decoder is used to interpret the higher-order addresses (A₁₇ and A₁₈) and to select one of the four RAMs.

Writing to the module is accomplished when the chip select (CS) and write enable (WE) inputs are both LOW. Data on the eight input/output pins (I/O₀ through

I/O₇) of the device is written into the memory location specified on the address pins (A₀ through A₁₈). Reading the device is accomplished by taking chip select and output enable (OE) LOW while write enable remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A₀ through A₁₈) will appear on the eight appropriate data input/output pins (I/O₀ through I/O₇).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable is HIGH.



Selection Guide

	1465-70	1465-85	1465-100	1465-120	1465-150
Maximum Access Time (ns)	70	85	100	120	150
Maximum Operating Current (mA)	110	110	110	110	110
Maximum Standby Current (mA)	12	12	12	12	12

Switching Characteristics Over the Operating Range^[2]

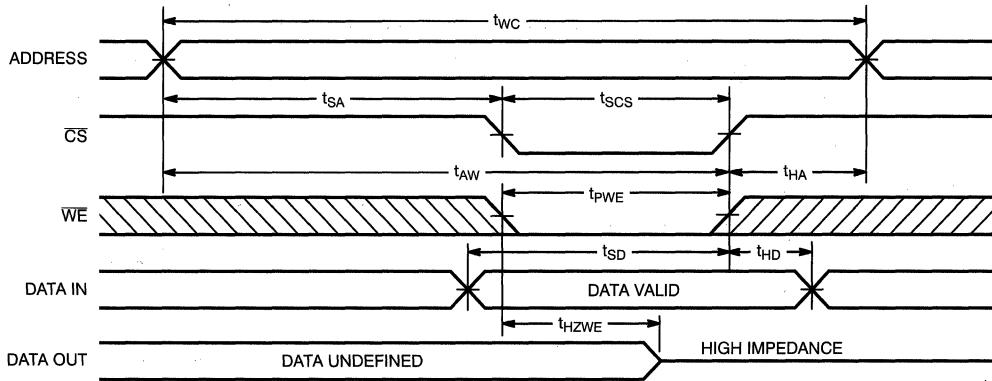
Parameter	Description	1465-70		1465-85		1465-100		1465-120		1465-150		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	70		85		100		120		150		ns
t _{AA}	Address to Data Valid		70		85		100		120		150	ns
t _{OHA}	Data Hold from Address Change	10		10		10		10		10		ns
t _{ACS}	CS LOW to Data Valid		70		85		100		120		150	ns
t _{DOE}	OE LOW to Data Valid		35		45		50		60		75	ns
t _{LZOE}	OE LOW to Low Z	5		5		5		5		5		ns
t _{HZOE}	OE HIGH to High Z ^[3]		25		30		35		45		55	ns
t _{LZCS}	CS LOW to Low Z	10		10		10		10		10		ns
t _{HZCS}	CS HIGH to High Z ^[3]		30		30		35		45		60	ns
WRITE CYCLE^[4]												
t _{WC}	Write Cycle Time	70		85		100		120		150		ns
t _{SCS}	CS LOW to Write End	65		75		90		100		115		ns
t _{AW}	Address Set-Up to Write End	65		75		90		100		110		ns
t _{HA}	Address Hold from Write End	0		5		5		5		5		ns
t _{SA}	Address Set-Up to Write Start	0		5		5		5		5		ns
t _{PWE}	WE Pulse Width	55		65		75		85		95		ns
t _{SD}	Data Set-Up to Write End	30		35		40		45		50		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{LZWE}	WE HIGH to Low Z	5		5		5		5		5		ns
t _{HZWE}	WE LOW to High Z ^[3]		25		30		35		40		45	ns

Data Retention Characteristics Over the Operating Range (L Version Only)

Parameter	Description	Test Conditions	Commercial		Industrial		Unit
			Min.	Max.	Min.	Max.	
V _{DR}	V _{CC} for Retention Data	CS ≥ V _{CC} - 0.2V	2		2		V
I _{CCDR3}	Data Retention Current	V _{DR} = 3.0V, CS ≥ V _{CC} - 0.2V,		50		150	μA
t _{CDR} ^[5]	Chip Deselect to Data Retention Time	V _{IN} ≥ V _{CC} - 0.2V or	0		0		ns
t _R ^[5]	Operation Recovery Time	V _{IN} ≤ 0.2V	5		5		ms

Notes:

- C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of CS LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- Guaranteed, not tested.

Switching Waveforms (continued)
Write Cycle No. 2 ($\overline{\text{CS}}$ Controlled)^[4, 9]


1465-9

Note:

9. If $\overline{\text{CS}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.

Truth Table

Inputs			Output	Mode
$\overline{\text{CS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$		
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

1024K x 8 SRAM Module
2048K x 8 SRAM Module

Features

- High-density 8-/16-megabit SRAM modules
- High-speed CMOS SRAMs
— Access time of 85 ns
- Low active power
— 605 mW (max.), 2M x 8
- Double-sided SMD technology
- TTL-compatible inputs and outputs
- Small footprint SIP
— PCB layout area of 0.72 sq. in.
- 2V data retention (L version)

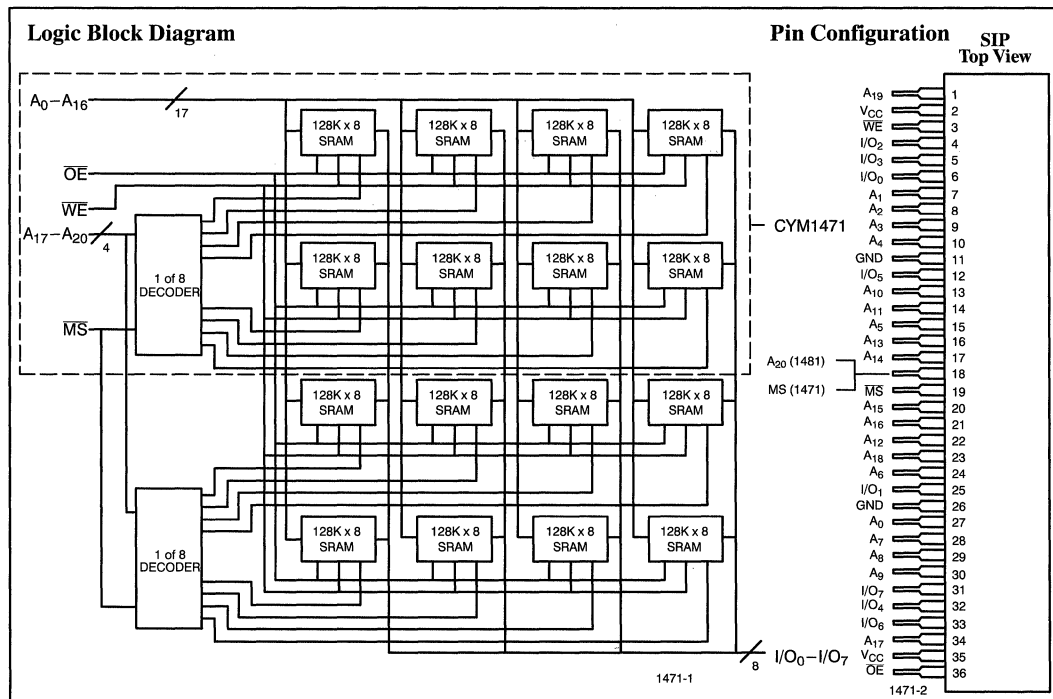
Functional Description

The CYM1471 and CYM1481 are high-performance 8-megabit and 16-megabit static RAM modules organized as 1024K words (1471) or 2048K words (1481) by 8 bits. These modules are constructed from eight (1471) or sixteen (1481) 128K x 8 SRAMs in plastic surface-mount packages on an epoxy laminate board with pins. On-board decoding selects one of the SRAMs from the high-order address lines, keeping the remaining devices in standby mode for minimum power consumption.

An active LOW write enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{MS} and \overline{WE} inputs are

both LOW, data on the eight data input/output pins is written into the memory location specified on the address pins. Reading the device is accomplished by selecting the device and enabling the outputs \overline{MS} and \overline{OE} active LOW while \overline{WE} remains inactive or HIGH. Under these conditions, the content of the location addressed by the information on the address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH.



Selection Guide

	CYM1471			CYM1481		
	85	100	120	85	100	120
Maximum Access Time (ns)	85	100	120	85	100	120
Maximum Operating Current (mA)	95	95	95	110	110	110
Maximum Standby Current (mA)	32	32	32	64	64	64

Switching Characteristics Over the Operating Range^[2]

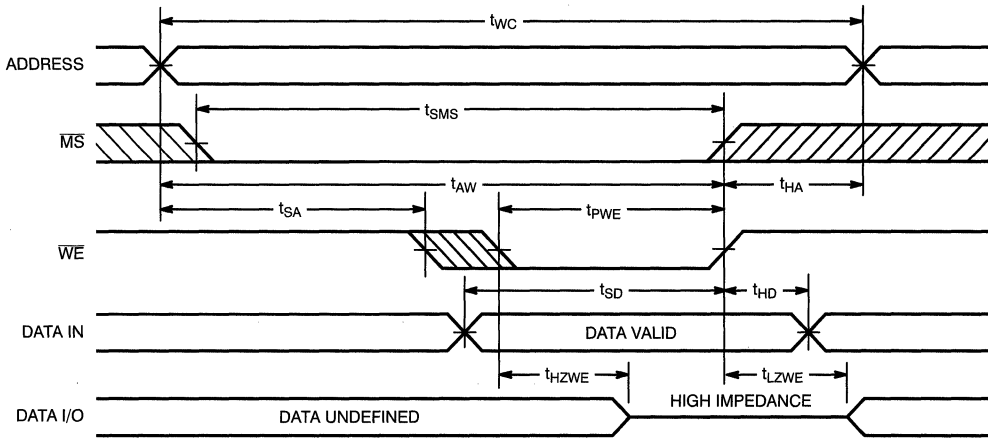
Parameter	Description	1471–85 1481–85		1471–100 1481–100		1471–120 1481–120		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	85		100		120		ns
t _{AA}	Address to Data Valid		85		100		120	ns
t _{OHA}	Data Hold from Address Change	10		10		10		ns
t _{AMS}	\overline{MS} LOW to Data Valid		85		100		120	ns
t _{DOE}	\overline{OE} LOW to Data Valid		45		50		60	ns
t _{LZOE}	\overline{OE} LOW to Low Z	5		5		5		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[3]		30		35		45	ns
t _{LZMS}	\overline{MS} LOW to Low Z ^[4]	10		10		10		ns
t _{HZMS}	\overline{MS} HIGH to High Z ^[3, 4]		30		35		45	ns
WRITE CYCLE^[5]								
t _{WC}	Write Cycle Time	85		100		120		ns
t _{SMS}	\overline{MS} LOW to Write End	75		90		100		ns
t _{AW}	Address Set-Up to Write End	75		90		100		ns
t _{HA}	Address Hold from Write End	7		7		7		ns
t _{SA}	Address Set-Up to Write Start	5		5		5		ns
t _{PWE}	\overline{WE} Pulse Width	65		75		85		ns
t _{SD}	Data Set-Up to Write End	35		40		45		ns
t _{HD}	Data Hold from Write End	5		5		5		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[3]		30		35		40	ns
t _{LZWE}	\overline{WE} HIGH to Low Z	5		5		5		ns

Data Retention Characteristics (L Version Only)

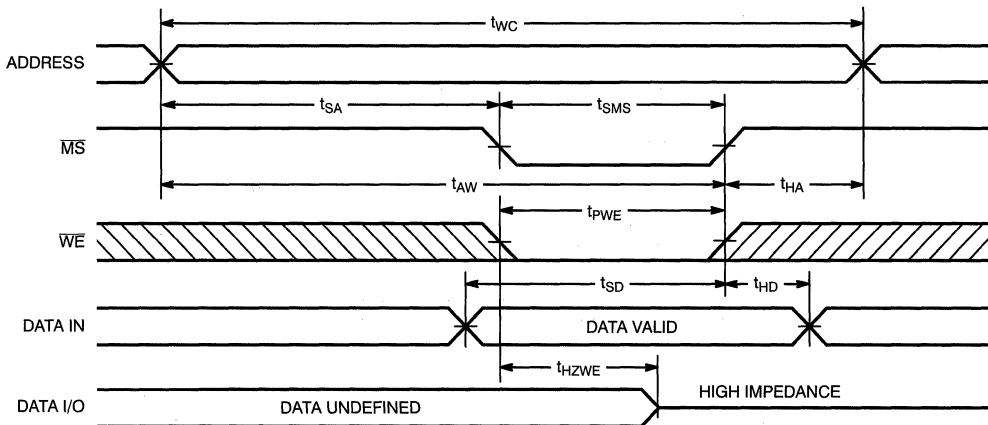
Parameter	Description	Test Conditions	1471–85		1471–100 1481–120		1481–85		1481–100 1481–120		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V _{DR}	V _{CC} for Retention Data		2		2		2		2		V
I _{CCDR}	Data Retention Current	V _{DR} = 3.0V, MS ≥ V _{CC} – 0.2V, V _{IN} ≥ V _{CC} – 0.2V or V _{IN} ≤ 0.2V		400		125		800		250	μA
t _{CDR} ^[6]	Chip Deselect to Data Retention Time		0		0		0		0		ns
t _R	Operation Recovery Time		5		5		5		5		ns

Notes:

- Test conditions assume signal transition time of 10 μs or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, output loading of 1 TTL load, and 100-pF load capacitance.
- t_{HZOE}, t_{HZMS}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZMS} is less than t_{LZMS} for any given device. These parameters are guaranteed and not 100% tested.
- The internal write time of the memory is defined by the overlap of \overline{MS} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- Guaranteed, not tested.

Switching Waveforms (continued)
Write Cycle No. 1^[5, 10]


1471-8

Write Cycle No. 2^[5, 10, 11]


1471-9

Notes:

10. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
11. If MS goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.



64K x 16 Static RAM Module

Features

- High-density 1-megabit SRAM module
- High-speed CMOS SRAMs
 - Access time of 15 ns
- Low active power
 - 2.2W (max.)
- SMD technology
- TTL-compatible inputs and outputs
- Pinout compatible with CYM1611
- Low profile
 - Max. height of .50 in.
- Small PCB footprint
 - 0.68 sq. in.

Functional Description

The CYM1622 is a very high performance 1-megabit static RAM module organized as 64K words by 16 bits. The module is constructed using four 64K x 4 static RAMs mounted onto a vertical substrate with pins. The pinout of this module is compatible with another Cypress module (CYM1611) to maximize system flexibility.

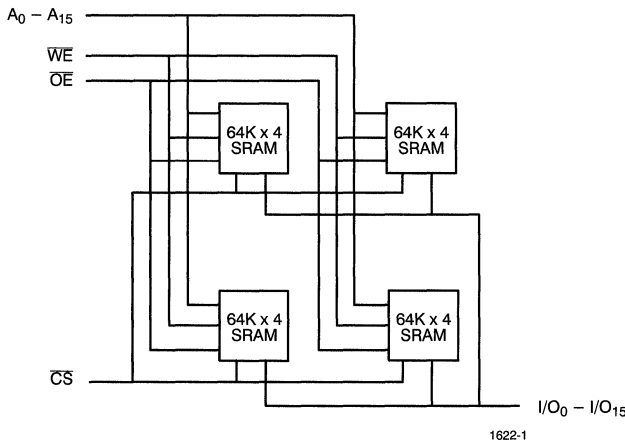
Writing to the memory module is accomplished when the chip select (CS) and write enable (WE) inputs are both LOW. Data on the sixteen input/output pins (I/O₀ through I/O₁₅) of the device is

written into the memory location specified on the address pins (A₀ through A₁₅).

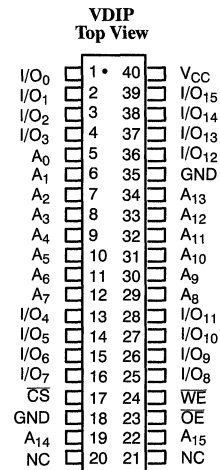
Reading the device is accomplished by taking chip select (CS) and output enable (OE) LOW, while write enable (WE) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable (WE) is HIGH.

Logic Block Diagram



Pin Configuration



Selection Guide

	1622-15	1622-20	1622-25	1622-30	1622-35	1622-45
Maximum Access Time (ns)	15	20	25	30	35	45
Maximum Operating Current (mA)	600	500	400	400	400	400
Maximum Standby Current (mA)	80	80	140	140	140	140

Shaded areas contain preliminary information.

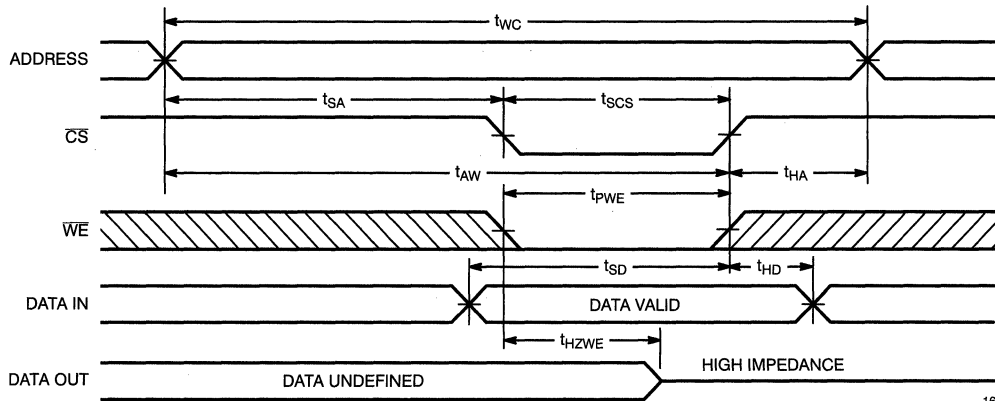
Switching Characteristics Over the Operating Range^[3]

Parameter	Description	1622-15		1622-20		1622-25		1622-30		1622-35		1622-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t _{RC}	Read Cycle Time	15		20		25		30		35		45		ns
t _{AA}	Address to Data Valid		15		20		25		30		35		45	ns
t _{OHA}	Data Hold from Address Change	3		3		3		3		3		3		ns
t _{ACS}	CS LOW to Data Valid		15		20		25		30		35		45	ns
t _{DOE}	OE LOW to Data Valid		8		10		15		20		25		30	ns
t _{LZOE}	OE LOW to Low Z	0		0		0		0		0		0		ns
t _{HZOE}	OE HIGH to High Z		8		10		15		20		20		20	ns
t _{LZCS}	CS LOW to Low Z	0		0		3		3		3		3		ns
t _{HZCS}	CS HIGH to High Z ^[4]		6		8		15		20		20		20	ns
t _{PU}	CS LOW to Power-Up	0		0		0	25	0	30	0	35	0	45	ns
t _{PD}	CS HIGH to Power-Down		15		20		25		30		35		45	ns
WRITE CYCLE^[5]														
t _{WC}	Write Cycle Time	15		20		25		30		35		45		ns
t _{SCS}	CS LOW to Write End	10		15		20		25		30		40		ns
t _{AW}	Address Set-Up to Write End	10		15		20		25		30		40		ns
t _{HA}	Address Hold from Write End	2		2		3		3		3		3		ns
t _{SA}	Address Set-Up to Write Start	2		2		2		2		2		2		ns
t _{PWE}	WE Pulse Width	10		15		20		25		25		30		ns
t _{SD}	Data Set-Up to Write End	8		12		15		20		20		25		ns
t _{HD}	Data Hold from Write End	2		2		2		2		2		2		ns
t _{LZWE}	WE HIGH to Low Z	3		3		0		0		0		0		ns
t _{HZWE}	WE LOW to High Z ^[4]	0	7	0	10	0	15	0	15	0	15	0	20	ns

Shaded areas contain preliminary information.

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of CS LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{CS} Controlled)^[5, 9]


1622-8

Note:

9. If \overline{CS} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Truth Table

\overline{CS}	\overline{OE}	\overline{WE}	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	L	H	Data Out	Read
L	X	L	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
15	CYM1622PV-15C	PV04	40-Pin Plastic VDIP Module	Commercial
20	CYM1622PV-20C	PV04	40-Pin Plastic VDIP Module	Commercial
25	CYM1622PV-25C	PV04	40-Pin Plastic VDIP Module	Commercial
30	CYM1622PV-30C	PV04	40-Pin Plastic VDIP Module	Commercial
35	CYM1622PV-35C	PV04	40-Pin Plastic VDIP Module	Commercial
45	CYM1622PV-45C	PV04	40-Pin Plastic VDIP Module	Commercial

Shaded areas contain preliminary information.

Document #: 38-M-00001-D

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-10°C to +85°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V

DC Input Voltage -0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM1720-15, 20		CYM1720-25, 30, 35		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage		-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-20	+20	-20	+20	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, CS ≤ V _{IL}		450		330	mA
I _{SB1}	Automatic CS Power-Down Current ^[1]	Max. V _{CC} , CS ≥ V _{IH} , Min. Duty Cycle = 100%		120		60	mA
I _{SB2}	Automatic CS Power-Down Current ^[1]	Max. V _{CC} , CS ≤ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V		90		60	mA

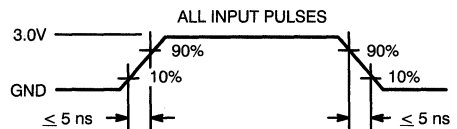
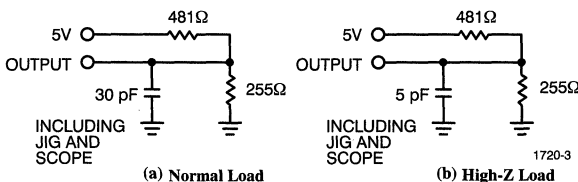
Shaded area contains preliminary information.

Capacitance^[2]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	35	pF
C _{OUT}	Output Capacitance		25	pF

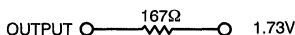
Notes:

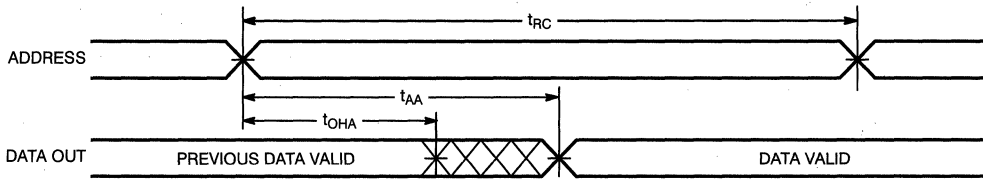
1. A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. * Tested on a sample basis.

AC Test Loads and Waveforms


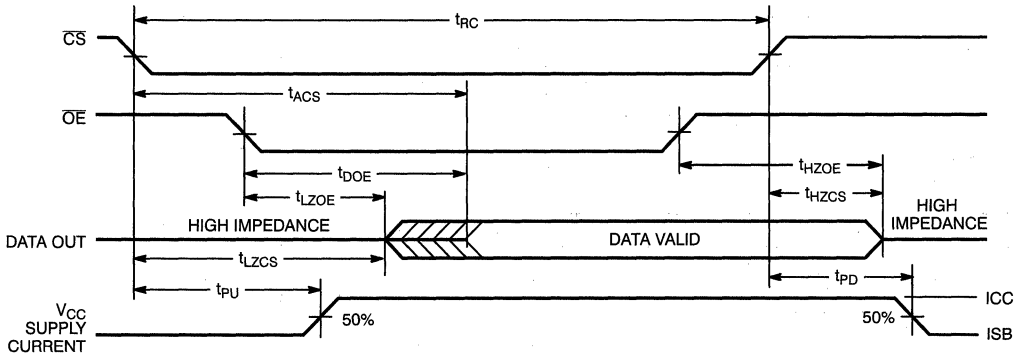
1720-4

Equivalent to: THÉVENIN EQUIVALENT

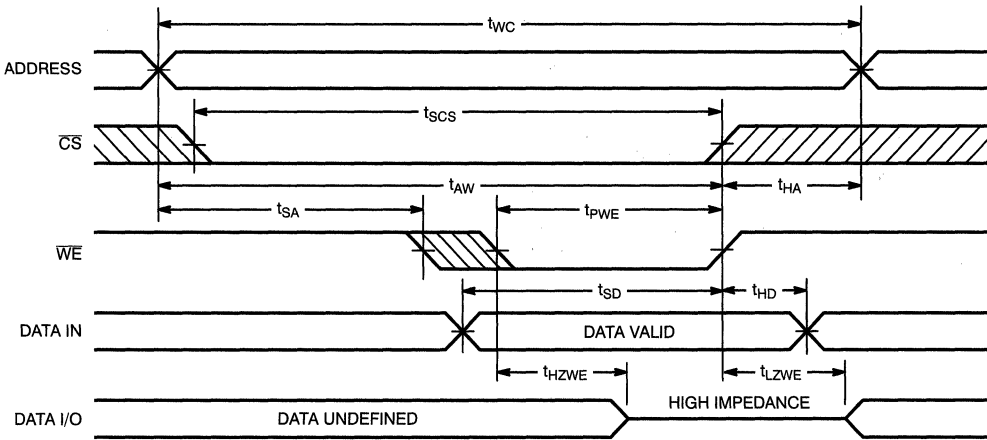


Switching Waveforms
Read Cycle No. 1^[7, 8]


1720-5

Read Cycle No. 2^[7, 9]


1720-6

Write Cycle No. 1 (WE Controlled)^[6, 10]


1720-7

Notes:

7. \overline{WE} is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
9. Address valid prior to or coincident with \overline{CS} transition LOW.
10. Data I/O will be high impedance if $\overline{OE} = V_{IH}$.



64K x 24 Static RAM Module

Features

- High-density 1.5M SRAM module
- High-speed CMOS SRAMs
— Access time of 25 ns
- 56-pin, 0.5-inch-high ZIP package
- Low active power
— 2.8W (max. for $t_{AA} = 25$ ns)
- SMD technology
- TTL-compatible inputs and outputs
- Commercial temperature range
- Small PCB footprint
— 1.05 sq. in.

Functional Description

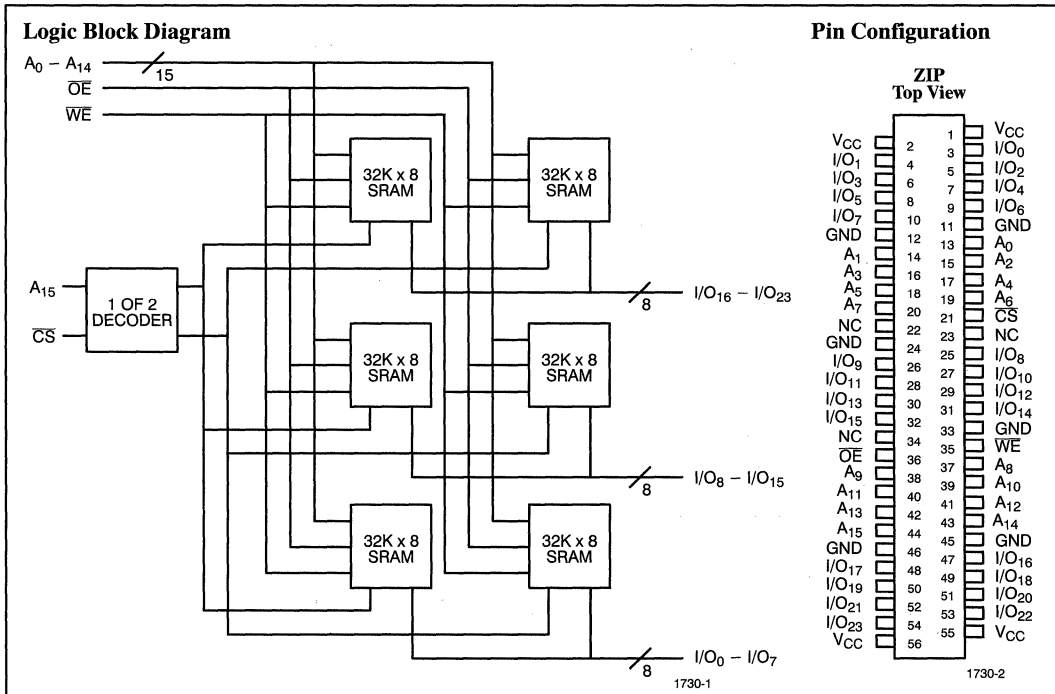
The CYM1730 is a high-performance 1.5M static RAM module organized as 64K words by 24 bits. This module is constructed using six 32K x 8 static RAMs in SOJ packages mounted onto an epoxy laminate board with pins.

Writing to the device is accomplished when the chip select (\overline{CS}) and write enable (\overline{WE}) inputs are both LOW. Data on the input/output pins (I/O_0 through I/O_{23}) of the device is written into the memory location

specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip select (\overline{CS}) and output enable (\overline{OE}) LOW while write enable (\overline{WE}) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable is HIGH.



Selection Guide

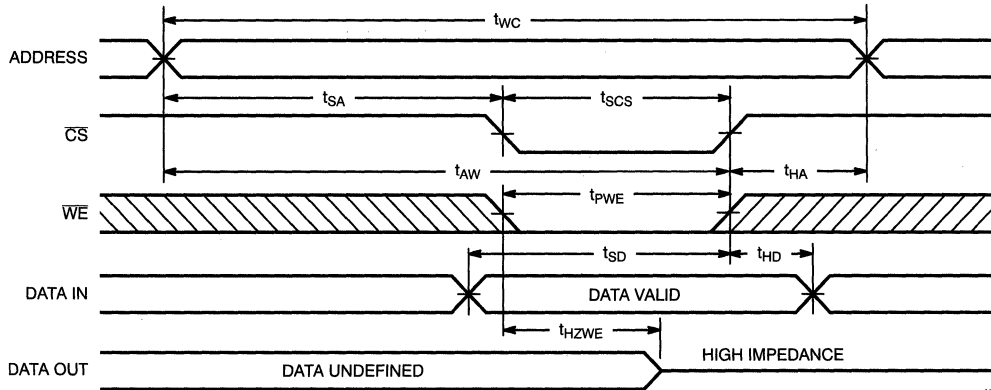
	1730-25	1730-30	1730-35
Maximum Access Time (ns)	25	30	35
Maximum Operating Current (mA)	510	510	510
Maximum Standby Current (mA)	180	180	180

Switching Characteristics Over the Operating Range^[3]

Parameter	Description	1730-25		1730-30		1730-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	25		30		35		ns
t _{AA}	Address to Data Valid		25		30		35	ns
t _{OHA}	Output Hold from Address Change	5		5		5		ns
t _{ACS}	$\overline{\text{CS}}$ LOW to Data Valid		25		30		35	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		12		15		20	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z	3		3		3		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z		10		15		20	ns
t _{LZCS}	$\overline{\text{CS}}$ LOW to Low Z ^[4]	5		5		5		ns
t _{HZCS}	$\overline{\text{CS}}$ HIGH to High Z ^[4, 5]		10		15		15	ns
WRITE CYCLE^[6]								
t _{WC}	Write Cycle Time	25		30		35		ns
t _{SCS}	$\overline{\text{CS}}$ LOW to Write End	20		25		30		ns
t _{AW}	Address Set-Up to Write End	22		25		30		ns
t _{HA}	Address Hold from Write End	2		2		2		ns
t _{SA}	Address Set-Up to Write Start	2		2		2		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	20		23		25		ns
t _{SD}	Data Set-Up to Write End	13		15		20		ns
t _{HD}	Data Hold from Write End	2		2		2		ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z	3		3		5		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[5]	0	10	0	10	0	15	ns

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
- t_{HZOE}, t_{HZCS}, and t_{LZCE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{\text{CS}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{CS} Controlled)[6, 10, 11]


1730-9

Note:

11. If \overline{CS} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Truth Table

\overline{CS}	\overline{WE}	\overline{OE}	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CYM1730PZ-25C	PZ07	56-Pin ZIP Module	Commercial
30	CYM1730PZ-30C	PZ07	56-Pin ZIP Module	Commercial
35	CYM1730PZ-35C	PZ07	56-Pin ZIP Module	Commercial

Document #: 38-M-00049-A

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-10°C to +85°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
Output Current into Outputs (LOW)	20 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1821-12 1821-15		1821-20 1821-25 1821-35 1821-45		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage		-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-20	+20	-20	+20	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-20	+20	-20	+20	μA
I _{OS}	Output Short Circuit Current ^[1]	V _{CC} = Max., V _{OUT} = GND		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, CS ≤ V _{IL}		960		720	mA
I _{SB1}	Automatic CS Power-Down Current ^[2]	Max. V _{CC} , CS ≥ V _{IH} , Min. Duty Cycle = 100%		450		160	mA
I _{SB2}	Automatic CS Power-Down Current ^[2]	Max. V _{CC} , CS _N ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		160		160	mA

Capacitance^[3]

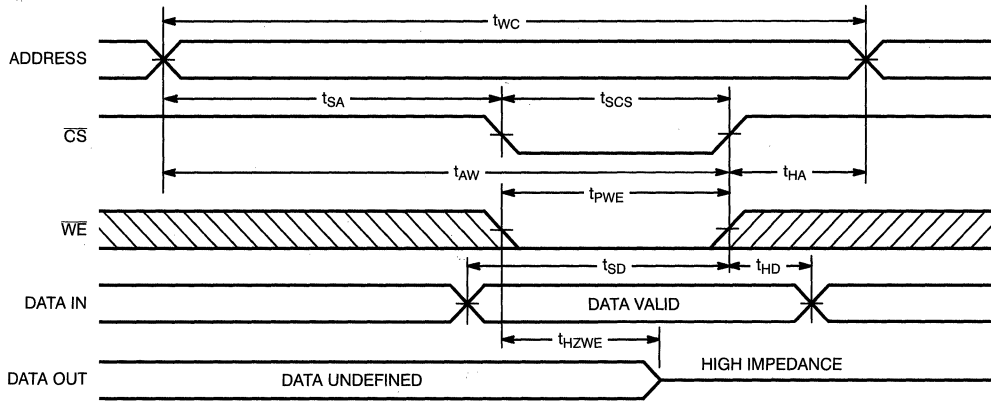
Parameter	Description	Test Conditions	Max.	Unit
C _{INA}	Input Capacitance (ADDR, OE, WE)	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	70	pF
C _{INB}	Input Capacitance (CS)		35	pF
C _{OUT}	Output Capacitance		20	pF

Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
- Tested on a sample basis.

Switching Characteristics Over the Operating Range (continued)^[4]

Parameter	Description	1821-25		1821-35		1821-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	25		35		45		ns
t _{AA}	Address to Data Valid		25		35		45	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACS}	\overline{CS} LOW to Data Valid		25		35		45	ns
t _{DOE}	\overline{OE} LOW to Data Valid		15		25		30	ns
t _{LZOE}	\overline{OE} LOW to Low Z	3		3		3		ns
t _{HZOE}	\overline{OE} HIGH to High Z		15		20		20	ns
t _{LZCS}	\overline{CS} LOW to Low Z ^[5]	5		10		10		ns
t _{HZCS}	\overline{CS} HIGH to High Z ^[5, 6]		10		15		20	ns
t _{PU}	\overline{CS} LOW to Power-Up	0		0		0		ns
t _{PD}	\overline{CS} HIGH to Power-Down		25		35		45	ns
WRITE CYCLE^[7]								
t _{WC}	Write Cycle Time	25		35		45		ns
t _{SCS}	\overline{CS} LOW to Write End	20		25		35		ns
t _{AW}	Address Set-Up to Write End	20		25		35		ns
t _{HA}	Address Hold from Write End	2		2		2		ns
t _{SA}	Address Set-Up to Write Start	2		2		2		ns
t _{PWE}	\overline{WE} Pulse Width	20		25		30		ns
t _{SD}	Data Set-Up to Write End	13		15		20		ns
t _{HD}	Data Hold from Write End	2		2		2		ns
t _{LZWE}	\overline{WE} HIGH to Low Z	3		5		5		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[6]	0	7	0	10	0	15	ns

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{CS} Controlled)^[7, 11]


1821-8

Note:

 11. If \overline{CS} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Truth Table

\overline{CS}_N	\overline{WE}	\overline{OE}	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
12	CYM1821PM-12C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821PZ-12C	PZ01	64-Pin Plastic ZIP Module	
15	CYM1821PM-15C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821PZ-15C	PZ01	64-Pin Plastic ZIP Module	
20	CYM1821PM-20C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821PZ-20C	PZ01	64-Pin Plastic ZIP Module	
25	CYM1821PM-25C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821PZ-25C	PZ01	64-Pin Plastic ZIP Module	
35	CYM1821PM-35C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821PZ-35C	PZ01	64-Pin Plastic ZIP Module	
45	CYM1821PM-45C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821PZ-45C	PZ01	64-Pin Plastic ZIP Module	

Document #: 38-M-00015-E

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1828		Unit
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} +0.3	V
V _{IL}	Input LOW Voltage		-0.3	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC} , V _{CC} = Max.	-20	+20	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-20	+20	μA
I _{CCx32}	V _{CC} Operating Supply Current by 32 Mode	V _{CC} = Max., I _O UT = 0 mA, CS ≤ V _{IL}		600	mA
			L Version	400	
I _{CCx16}	V _{CC} Operating Supply Current by 16 Mode	V _{CC} = Max., I _O UT = 0 mA, CS ≤ V _{IL}		360	mA
			L Version	230	
I _{CCx8}	V _{CC} Operating Supply Current by 8 Mode	V _{CC} = Max., I _O UT = 0 mA, CS ≤ V _{IL}		240	mA
			L Version	145	
I _{SB1}	Automatic CS Power-Down Current ^[1]	Max. V _{CC} ; CS ≥ V _{IH} , Min. Duty Cycle = 100%		200	mA
I _{SB2}	Automatic CS Power-Down Current ^[1]	Max. V _{CC} ; CS ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V		100	mA

Capacitance^[2]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	50	pF
C _{OUT}	Output Capacitance		20	pF

Notes:

1. A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

Switching Characteristics Over the Operating Range (continued)^[3]

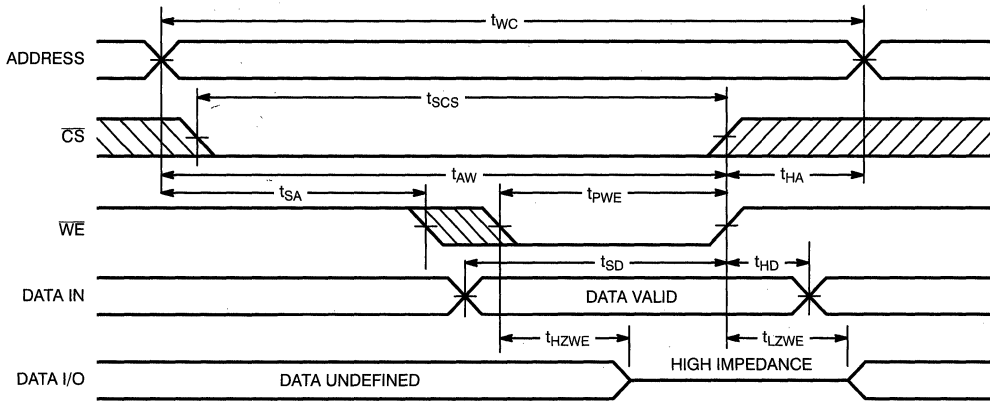
Parameter	Description	1828-45		1828-55		1828-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	45		55		70		ns
t _{AA}	Address to Data Valid		45		55		70	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACS}	$\overline{\text{CS}}$ LOW to Data Valid		45		55		70	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		25		30		35	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z	0		0		0		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z		25		30		30	ns
t _{LZCS}	$\overline{\text{CS}}$ LOW to Low Z ^[4]	3		3		3		ns
t _{HZCS}	$\overline{\text{CS}}$ HIGH to High Z ^[4,5]		25		30		30	ns
WRITE CYCLE^[6]								
t _{WC}	Write Cycle Time	45		55		70		ns
t _{SCS}	$\overline{\text{CS}}$ LOW to Write End	40		45		55		ns
t _{AW}	Address Set-Up to Write End	40		45		55		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	30		35		45		ns
t _{SD}	Data Set-Up to Write End	25		30		40		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z	0		0		0		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[5]	0	30	0	30	0	30	ns

Data Retention Characteristics (L Version Only)

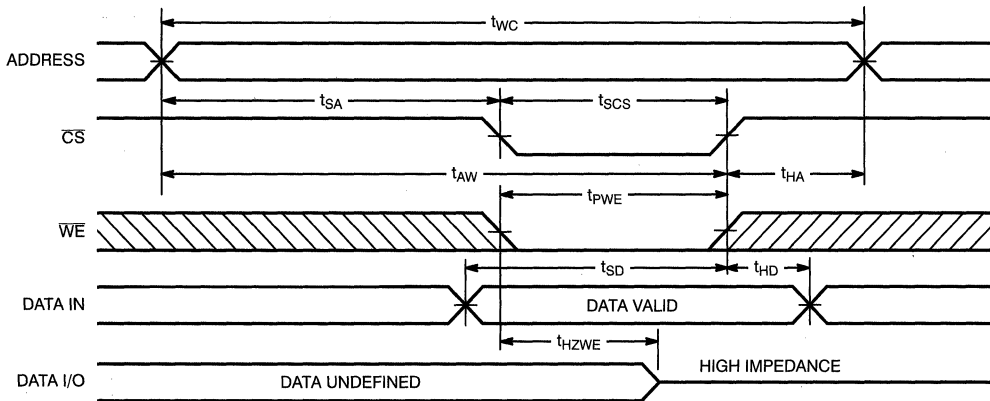
Parameter	Description	Test Conditions	1828		Unit
			Min.	Max.	
V _{DR}	V _{CC} for Retention Data	$\overline{\text{CS}} \geq V_{\text{CC}} - 0.2\text{V}$	2		V
I _{CCDR3}	Data Retention Current	$\overline{\text{CS}} \geq V_{\text{CC}} - 0.2\text{V}$, $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{IN}} \leq 0.2\text{V}$, V _{DR} = 3.0V		320	μA
t _{CDR^[7]}	Chip Deselect to Data Retention Time		0		ns
t _{R^[7]}	Operation Recovery Time		t _{RC}		

Note:

7. Guaranteed, not tested.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{WE} Controlled)^[6, 11]


1828-8

Write Cycle No. 2 (\overline{CS} Controlled)^[6, 11, 12]


1828-9

Notes:

 11. Data I/O will be high impedance if $\overline{OE} = V_{IH}$.

 12. If \overline{CS}_N goes HIGH simultaneously with \overline{WE}_N HIGH, the output remains in a high-impedance state.

64K x 32 Static RAM Module

Features

- High-density 2-Mbit SRAM module
- 32-bit standard footprint supports densities from 16K x 32 through 1M x 32
- High-speed CMOS SRAMs
— Access time of 15 ns
- Low active power
— 5.3W (max.)
- SMD technology
- TTL-compatible inputs and outputs
- Low profile
— Max. height of .50 in.
- Small PCB footprint
— 1.2 sq. in.

Functional Description

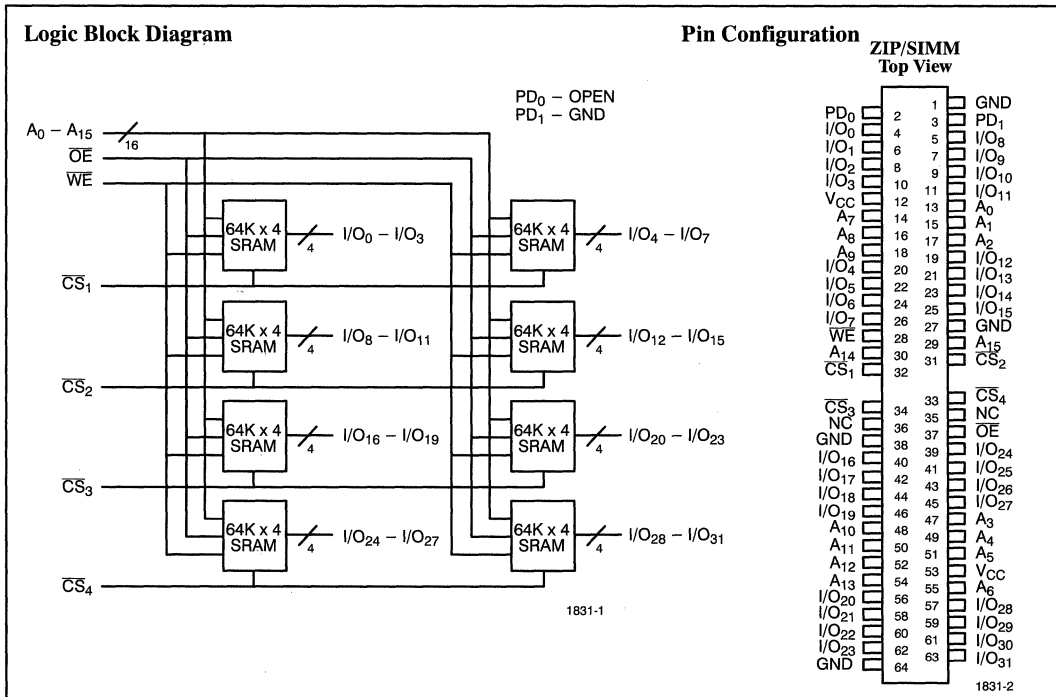
The CYM1831 is a high-performance 2-Mbit static RAM module organized as 64K words by 32 bits. This module is constructed from eight 64K x 4 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects (\overline{CS}_1 , \overline{CS}_2 , \overline{CS}_3 , and \overline{CS}_4) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

Writing to each byte is accomplished when the appropriate chip selects (\overline{CS}_N) and write enable (\overline{WE}) inputs are both LOW. Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip selects (\overline{CS}_N) LOW and output enable (\overline{OE}) LOW while write enable (\overline{WE}) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_X).

The data input/output pins stay in the high-impedance state when write enable (\overline{WE}) is LOW or the appropriate chip selects are HIGH.

Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.


Selection Guide

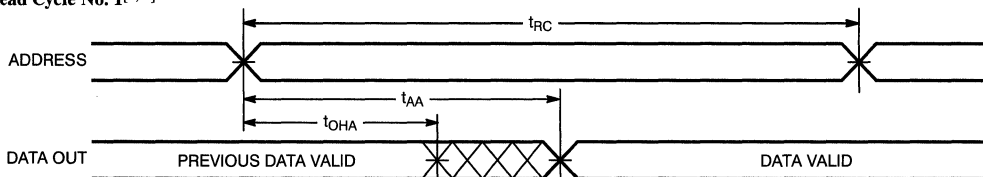
	1831-15	1831-20	1831-25	1831-30	1831-35	1831-45
Maximum Access Time (ns)	15	20	25	30	35	45
Maximum Operating Current (mA)	1120	960	720	720	720	720
Maximum Standby Current (mA)	160	160	160	160	160	160

Switching Characteristics Over the Operating Range^[3]

Parameter	Description	1831-15		1831-20		1831-25		1831-30		1831-35		1831-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t _{RC}	Read Cycle Time	15		20		25		30		35		45		ns
t _{AA}	Address to Data Valid		15		20		25		30		35		45	ns
t _{OHA}	Data Hold from Address Change	3		3		3		3		3		3		ns
t _{ACS}	CS LOW to Data Valid		15		20		25		30		35		45	ns
t _{DOE}	OE LOW to Data Valid		8		10		15		20		20		30	ns
t _{LZOE}	OE LOW to Low Z	0		0		0		0		0		0		ns
t _{HZOE}	OE LOW to High Z		8		10		15		15		20		20	ns
t _{LZCS}	CS LOW to Low Z ^[4]	0		0		3		3		3		3		ns
t _{HZCS}	CS HIGH to High Z ^[4, 5]		6		8		13		15		20		20	ns
WRITE CYCLE^[6]														
t _{WC}	Write Cycle Time	15		20		25		30		35		45		ns
t _{SCS}	CS LOW to Write End	10		15		20		25		30		40		ns
t _{AW}	Address Set-Up to Write End	10		15		20		25		30		40		ns
t _{HA}	Address Hold from Write End	2		2		2		2		2		2		ns
t _{SA}	Address Set-Up to Write Start	2		2		2		2		2		2		ns
t _{PWE}	WE Pulse Width	10		15		20		25		25		30		ns
t _{SD}	Data Set-Up to Write End	8		12		15		15		20		20		ns
t _{HD}	Data Hold from Write End	2		2		2		2		2		2		ns
t _{LZWE}	WE HIGH to Low Z	3		3		3		3		3		3		ns
t _{HZWE}	WE LOW to High Z ^[5]	0	7	0	10	0	13	0	15	0	20	0	20	ns

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed by design and not 100% tested.
- t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of CS LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- WE is HIGH for read cycle.
- Device is continuously selected, CS = V_{IL} and OE = V_{IL}.

Switching Waveforms
Read Cycle No. 1^[7, 8]


1831-5

Truth Table

CS _N	WE	OE	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
15	CYM1831PM-15C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN-15C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ-15C	PZ01	64-Pin Plastic ZIP Module	
20	CYM1831PM-20C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN-20C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ-20C	PZ01	64-Pin Plastic ZIP Module	
25	CYM1831PM-25C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN-25C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ-25C	PZ01	64-Pin Plastic ZIP Module	
30	CYM1831PM-30C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN-30C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ-30C	PZ01	64-Pin Plastic ZIP Module	
35	CYM1831PM-35C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN-35C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ-35C	PZ01	64-Pin Plastic ZIP Module	
45	CYM1831PM-45C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN-45C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ-45C	PZ01	64-Pin Plastic ZIP Module	

Document #: 38-M-00018-E

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature -45°C to +125°C
 Ambient Temperature with
 Power Applied -10°C to +85°C
 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Voltage Applied to Outputs
 in High Z State -0.5V to +7.0V
 DC Input Voltage -0.5V to +7.0V
 Output Current into Outputs (LOW) 20 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

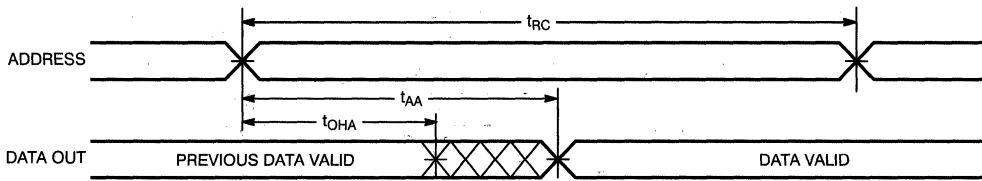
Parameter	Description	Test Conditions	CYM1832		Unit
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[1]		-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-20	+20	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-100	+100	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, $\overline{CS}_N \leq V_{IL}$		980	mA
I _{SB1}	Automatic \overline{CS} Power-Down Current ^[2]	Max. V _{CC} , $\overline{CS}_N \geq V_{IH}$, Min. Duty Cycle = 100%		240	mA
I _{SB2}	Automatic \overline{CS} Power-Down Current ^[2]	Max. V _{CC} , $\overline{CS}_N \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V		120	mA

Capacitance^[3]

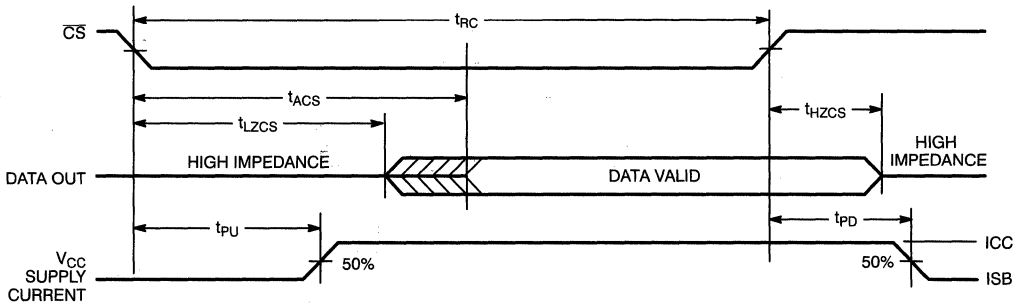
Parameter	Description	Test Conditions	Max.	Unit
C _{INA}	Input Capacitance (A _X , \overline{WE})	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	60	pF
C _{INB}	Input Capacitance (\overline{CS})		25	pF
C _{OUT}	Output Capacitance		15	pF

Notes:

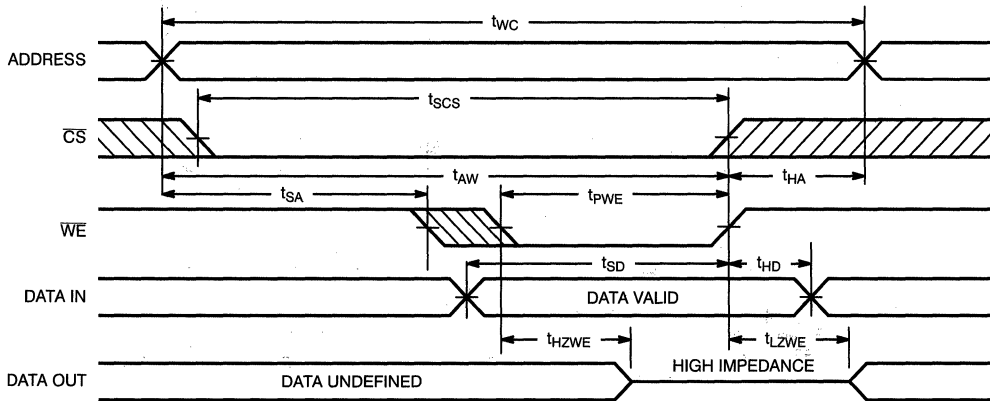
- V_{IL}(min.) = -3.0V for pulse widths less than 20 ns.
- A pull-up resistor to V_{CC} on the \overline{CS} input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
- Tested on a sample basis.

Switching Waveforms
Read Cycle No. 1^[8, 9]


M1832-5

Read Cycle No. 2^[9, 10]


M1832-6

Write Cycle No. 1 (\overline{WE} Controlled)^[7]


M1832-7

Notes:

8. Device is continuously selected, $\overline{CS} = V_{IL}$.
9. \overline{WE} is HIGH for read cycle.

10. Address valid prior to or coincident with \overline{CS} transition LOW.



128K x 32 Static RAM Module

Features

- High-density 4-megabit SRAM module
- 32-bit standard footprint supports densities from 16K x 32 through 1M x 32
- High-speed CMOS SRAMs
— Access time of 15 ns
- Low active power
— 2.6W (max.) at 20 ns
- SMD technology
- TTL-compatible inputs and outputs
- Low profile
— Max. height of 0.57 in.
- Small PCB footprint
— 0.78 sq. in.

- Available in SIMM, ZIP format.
SIMM suitable for vertical or angled sockets.

Functional Description

The CYM1836 is a high-performance 4-megabit static RAM module organized as 128K words by 32 bits. This module is constructed from four 128K x 8 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects (CS_1, CS_2, CS_3, CS_4) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

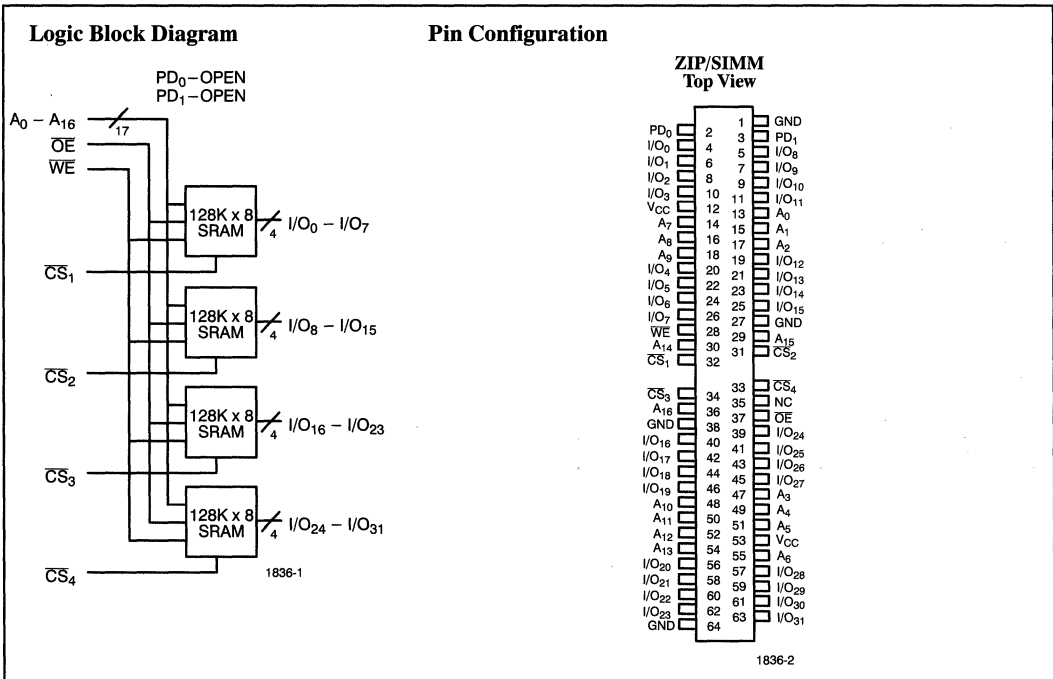
Writing to each byte is accomplished when the appropriate chip select (CS) and write enable (WE) inputs are both LOW. Data

on the input/output pins (I/O) is written into the memory location specified on the address pins (A_0 through A_{16}).

Reading the device is accomplished by taking the chip select (CS) LOW while write enable (WE) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O).

The data input/output pins stay at the high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.



Selection Guide

	1836-15	1836-20	1836-25	1836-30	1836-35	1836-45
Maximum Access Time (ns)	15	20	25	30	35	45
Maximum Operating Current (mA)	760	480	480	480	480	480
Maximum Standby Current (mA)	180	100	100	100	100	100

Shaded area contains preliminary information.

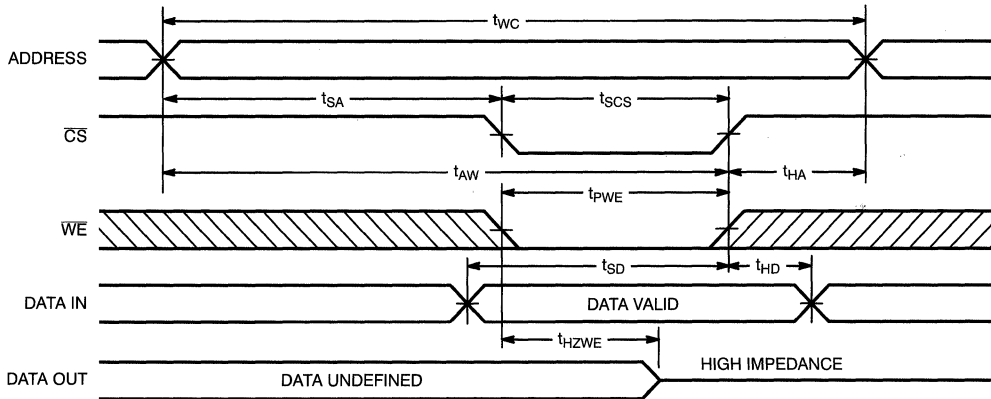
Switching Characteristics Over the Operating Range^[4]

Parameter	Description	1836-15		1836-20		1836-25		1836-30		1836-35		1836-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t _{RC}	Read Cycle Time	15		20		25		30		35		45		ns
t _{AA}	Address to Data Valid		15		20		25		30		35		45	ns
t _{OHA}	Output Hold from Address Change	3		3		3		3		3		3		ns
t _{ACS}	CS LOW to Data Valid		15		20		25		30		35		45	ns
t _{DOE}	OE LOW to Data Valid		7		8		8		10		12		15	ns
t _{LZOE}	OE LOW to Low Z	0		0		0		0		0		0		ns
t _{HZOE}	OE HIGH to High Z		7		8		10		11		12		15	ns
t _{LZCS}	CS LOW to Low Z ^[5]	3		3		3		3		3		3		ns
t _{HZCS}	CS HIGH to High Z ^[5,6]		7		10		10		13		15		18	ns
WRITE CYCLE^[7]														
t _{WC}	Write Cycle Time	15		20		25		30		35		45		ns
t _{SCS}	CS LOW to Write End	12		15		15		18		20		25		ns
t _{AW}	Address Set-Up to Write End	12		15		15		18		20		25		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t _{PWE}	WE Pulse Width	12		15		15		18		20		25		ns
t _{SD}	Data Set-Up to Write End	7		10		10		13		15		20		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		0		ns
t _{LZWE}	WE HIGH to Low Z	0		0		0		0		0		0		ns
t _{HZWE}	WE LOW to High Z ^[6]	0	6	0	8	0	10	0	15	0	15	0	18	ns

Shaded area contains preliminary information.

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed by design and not 100% tested.
- t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of CS LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{CS} Controlled)^[7, 11]


1836-8

Truth Table

\overline{CS}_N	\overline{WE}	\overline{OE}	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information^[12]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CYM1836PM-15C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-15C	PZ08	64-Pin ZIP Module	
20	CYM1836PM-20C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-20C	PZ08	64-Pin ZIP Module	
25	CYM1836PM-25C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-25C	PZ08	64-Pin ZIP Module	
30	CYM1836PM-30C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-30C	PZ08	64-Pin ZIP Module	
35	CYM1836PM-35C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-35C	PZ08	64-Pin ZIP Module	
45	CYM1836PM-45C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-45C	PZ08	64-Pin ZIP Module	

Shaded area contains preliminary information.

Notes:

11. If \overline{CS} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state. 12. 64-pin SIMM suitable for use in angled SIMM applications.

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

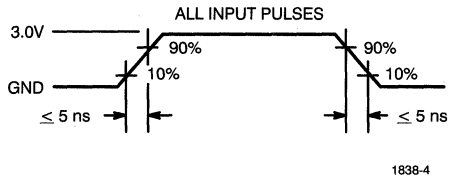
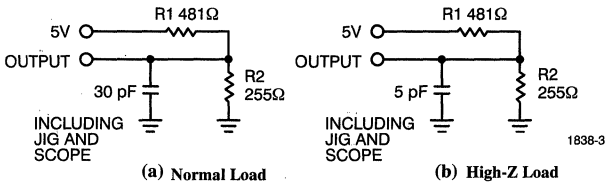
Parameter	Description	Test Conditions	1838		Unit
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.2	6.0	V
V _{IL}	Input LOW Voltage		-0.3	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC} , V _{CC} = Max.	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	μA
I _{CCx32}	V _{CC} Operating Supply Current by 32 Mode	V _{CC} = Max., I _{OUT} = 0 mA, $\overline{CS} \leq V_{IL}$		720	mA
I _{CCx16}	V _{CC} Operating Supply Current by 16 Mode	V _{CC} = Max., I _{OUT} = 0 mA, $\overline{CS} \leq V_{IL}$		480	mA
I _{CCx8}	V _{CC} Operating Supply Current by 8 Mode	V _{CC} = Max., I _{OUT} = 0 mA, $\overline{CS} \leq V_{IL}$		360	mA
I _{SB1}	Automatic \overline{CS} Power-Down Current ^[1]	Max. V _{CC} ; $\overline{CS} \geq V_{IH}$, Min. Duty Cycle = 100%		240	mA
I _{SB2}	Automatic \overline{CS} Power-Down Current ^[1]	Max. V _{CC} ; $\overline{CS} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V		40	mA

Capacitance^[2]

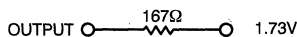
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	50	pF
C _{OUT}	Output Capacitance		50	pF

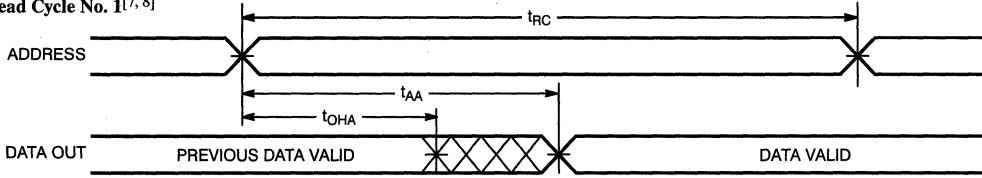
Notes:

1. A pull-up resistor to V_{CC} on the \overline{CS} input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

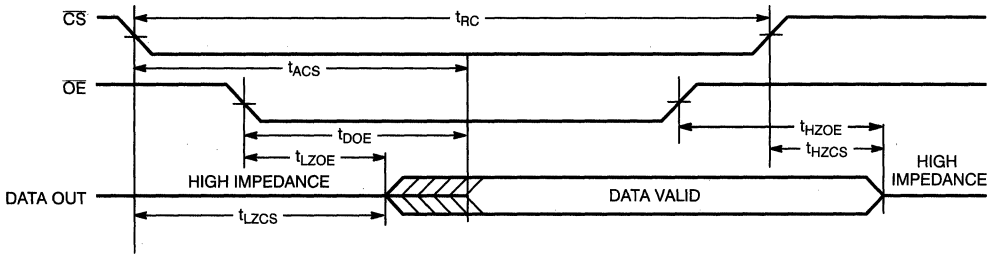
AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT

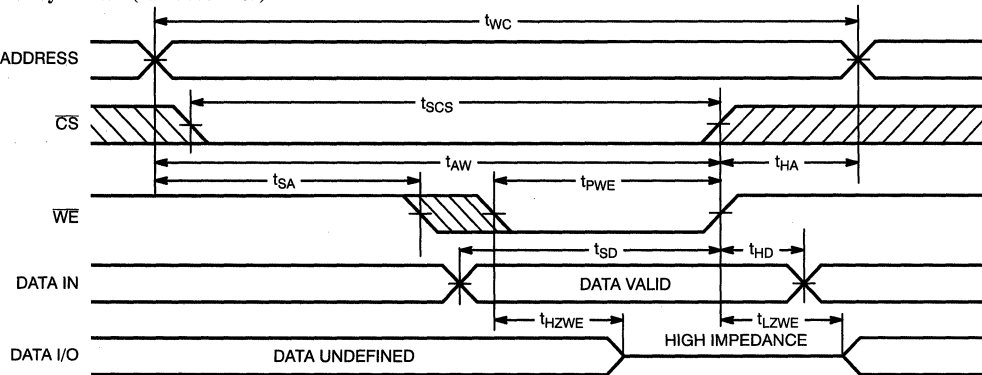


Switching Waveforms
Read Cycle No. 1^[7, 8]


1838-5

Read Cycle No. 2^[7, 9]


1838-6

Write Cycle No. 1 (\overline{WE} Controlled)^[6, 10]


1838-7

Notes:

7. \overline{WE}_N is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
9. Address valid prior to or coincident with \overline{CS} transition LOW.
10. Data I/O will be high impedance if $\overline{OE} = V_{IH}$.

256K x 32 Static RAM Module

Features

- High-density 8-megabit SRAM module
- High-speed CMOS SRAMs
— Access time of 20 ns
- Independent byte and word controls
- Low active power
— 6.2W (max.)
- SMD technology
- TTL-compatible inputs and outputs
- Low profile
— Max. height of .350 in.
- Small PCB footprint
— 1.8 sq. in.

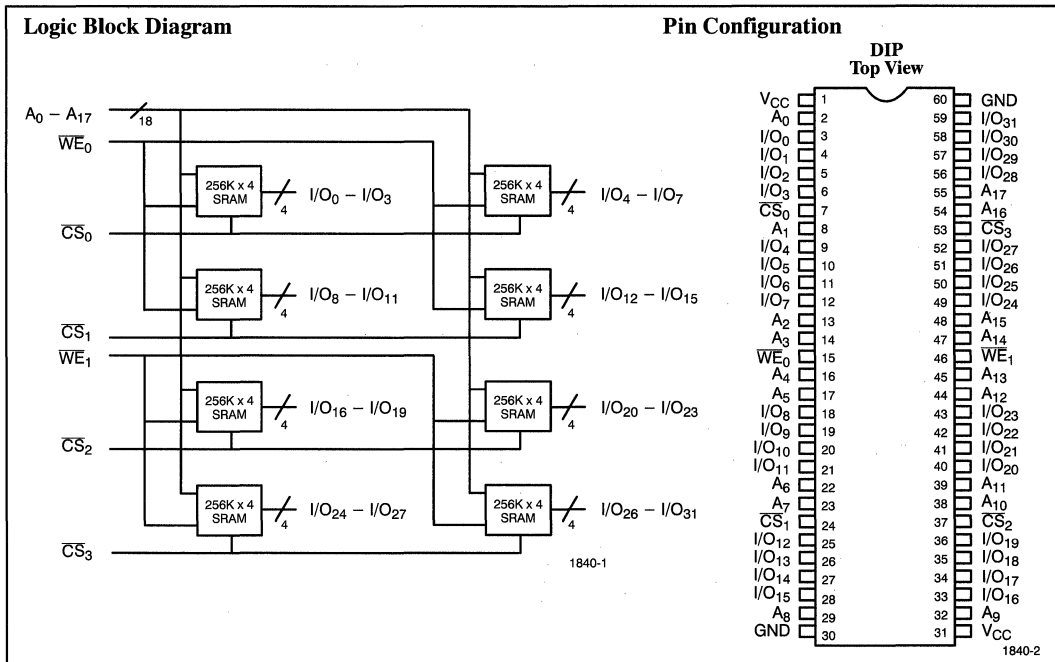
Functional Description

The CYM1840 is a high-performance 8-megabit static RAM module organized as 256K words by 32 bits. This module is constructed from eight 256K x 4 SRAMs in SOJ packages mounted on an epoxy laminate substrate with pins. Four chip selects (\overline{CS}_0 , \overline{CS}_1 , \overline{CS}_2 , and \overline{CS}_3) are used to independently enable the four bytes. Two write enables (\overline{WE}_0 and \overline{WE}_1) are used to independently write to either the upper or lower 16-bit word of RAM. Reading or writing can be executed on individual bytes or on any combination of multiple bytes through the proper use of selects and write enables.

Writing to each byte is accomplished when the appropriate chip select (\overline{CS}) and write enable (\overline{WE}) inputs are both LOW. Data on the input/output pins ($\overline{I/O}_X$) is written into the memory location specified on the address pins (A_0 through A_{17}).

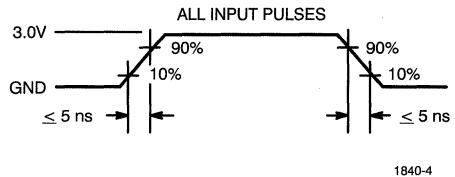
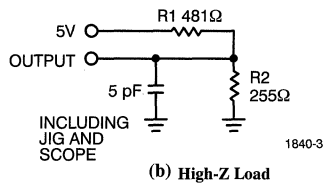
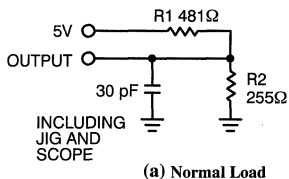
Reading the device is accomplished by taking the chip selects (\overline{CS}) LOW, while write enables (\overline{WE}) remain HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins ($\overline{I/O}$).

The data input/output pins stay in the high-impedance state when write enables (\overline{WE}) are LOW or the appropriate chip selects are HIGH.

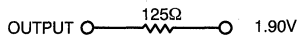


Selection Guide

	1840-20	1840-25	1840-30	1840-35	1840-45	1840-55
Maximum Access Time (ns)	20	25	30	35	45	55
Maximum Operating Current (mA)	1120	1120	1120	1120	1120	1120
Maximum Standby Current (mA)	320	320	320	320	320	320

AC Test Loads and Waveforms


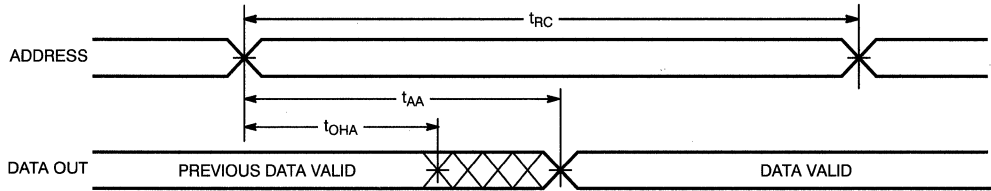
Equivalent to: THÉVENIN EQUIVALENT


Switching Characteristics Over the Operating Range^[3]

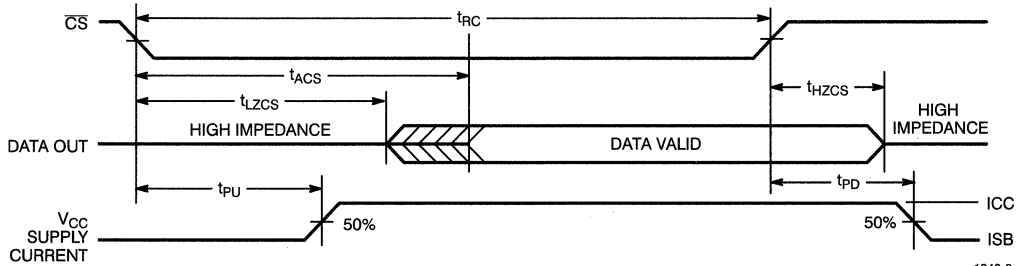
Parameter	Description	1840-20		1840-25		1840-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	20		25		30		ns
t _{AA}	Address to Data Valid		20		25		30	ns
t _{OHA}	Output Hold from Address Change	5		5		5		ns
t _{ACS}	$\overline{\text{CS}}$ LOW to Data Valid		20		25		30	ns
t _{LZCS}	$\overline{\text{CS}}$ LOW to Low Z ^[4]	5		5		5		ns
t _{HZCS}	$\overline{\text{CS}}$ HIGH to High Z ^[4, 5]		20		20		20	ns
t _{PU}	$\overline{\text{CS}}$ LOW to Power-Up	0		0		0		ns
t _{PD}	$\overline{\text{CS}}$ HIGH to Power-Down		20		25		30	ns
WRITE CYCLE^[6]								
t _{WC}	Write Cycle Time	20		25		30		ns
t _{SCS}	$\overline{\text{CS}}$ LOW to Write End	18		20		25		ns
t _{AW}	Address Set-Up to Write End	18		20		25		ns
t _{HA}	Address Hold from Write End	2		2		2		ns
t _{SA}	Address Set-Up to Write Start	2		2		2		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	15		20		25		ns
t _{SD}	Data Set-Up to Write End	13		15		15		ns
t _{HD}	Data Hold from Write End	2		2		2		ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z	0		0		0		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[5]	0	15	0	15	0	15	ns

Notes:

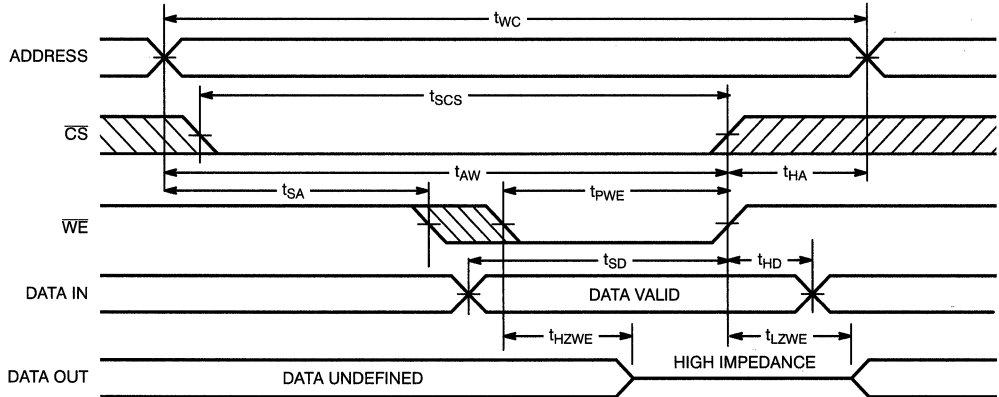
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
- t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{\text{CS}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms
Read Cycle No. 1^[7, 8]


1840-5

Read Cycle No. 2^[7, 8]


1840-6

Write Cycle No. 1 (\overline{WE} Controlled)^[6]


1840-7

Notes:

 7. Device is continuously selected, $\overline{CS} = V_{IL}$.

 8. \overline{WE} is HIGH for read cycle.

256K x 32 Static RAM Module

Features

- High-density 8-megabit SRAM module
- 32-bit standard footprint supports densities from 16K x 32 through 1M x 32
- High-speed CMOS SRAMs
 - Access time of 12 ns
- Low active power
 - 5.3W (max.) at 25 ns
- SMD technology
- TTL-compatible inputs and outputs
- Low profile
 - Max. height of 0.58 in.
- Available in ZIP, SIMM, and angled SIMM footprint
- 72-pin SIMM version compatible with 1M x 32 (CYM1851)

Functional Description

The CYM1841/1841A is a high-performance 8-megabit static RAM module organized as 256K words by 32 bits. This module is constructed from eight 256K x 4 SRAMs mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS}_1, \overline{CS}_2, \overline{CS}_3, \overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

Writing to each byte is accomplished when the appropriate chip select (\overline{CS}) and write enable (\overline{WE}) inputs are both LOW. Data on the input/output pins (I/O) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking the chip select (\overline{CS}) LOW while write enable (\overline{WE}) remains HIGH. Under these

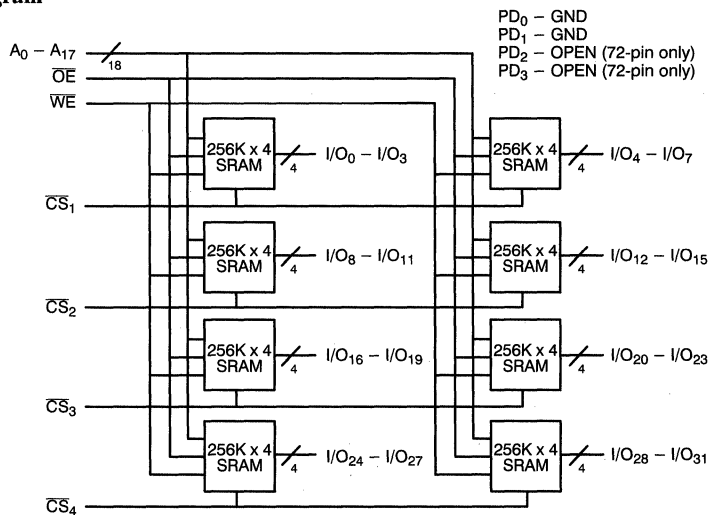
conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O).

The data input/output pins stay at the high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.

A 72-pin SIMM is offered for compatibility with the 1M x 32 CYM1851. This version is socket upgradable to the CYM1851.

Logic Block Diagram



Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1841A-12 1841A-15		1841-20 1841A-20		1841-25, 30, 35, 45, 55 1841A-25, 30, 35, 45, 55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-16	+16	-16	+16	-16	+16	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	-10	+10	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, CS ≤ V _{IL}		1600		1120		960	mA
I _{SB1}	Automatic CS Power-Down Current ^[1]	Max. V _{CC} , CS ≥ V _{IH} , Min. Duty Cycle = 100%		480		480		480	mA
I _{SB2} 1841	Automatic CS Power-Down Current ^[1]	Max. V _{CC} , CS ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V, or V _{IN} ≤ 0.2V				16		16	mA
I _{SB2} 1841A	Automatic CS Power-Down Current ^[1]	Max. V _{CC} , CS ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V, or V _{IN} ≤ 0.2V		240		120		120	mA

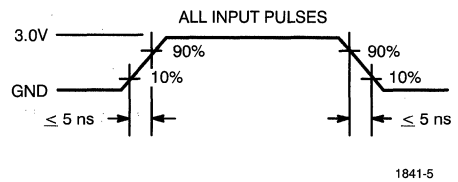
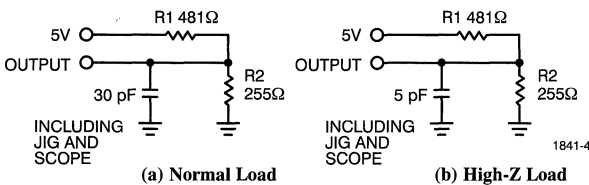
Shaded area contains preliminary information.

Capacitance^[2]

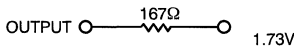
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance ^[3]	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	70/20	pF
C _{OUT}	Output Capacitance			

Note:

1. A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.
3. 20 pF on CS, 70 pF all others.

AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT

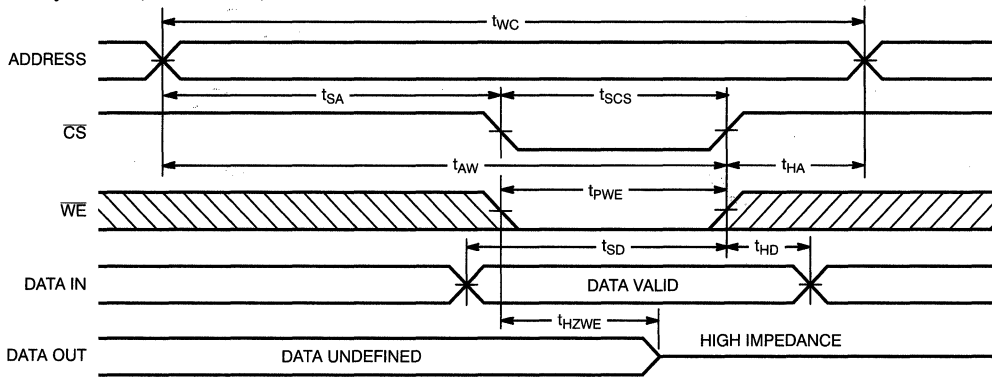


Switching Characteristics Over the Operating Range (continued)^[4]

Parameter	Description	1841-35 1841A-35		1841-45 1841A-45		1841-55 1841A-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	35		45		55		ns
t _{AA}	Address to Data Valid		35		45		55	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACS}	\overline{CS} LOW to Data Valid		35		45		55	ns
t _{DOE}	\overline{OE} LOW to Data Valid		25		30		35	ns
t _{LZOE}	\overline{OE} LOW to Low Z	0		0		0		ns
t _{HZOE}	\overline{OE} LOW to High Z		15		15		15	ns
t _{LZCS}	\overline{CS} LOW to Low Z ^[5]	10		10		10		ns
t _{HZCS}	\overline{CS} HIGH to High Z ^[5, 6]		20		20		20	ns
t _{PD}	\overline{CS} HIGH to Power-Down		35		45		55	ns
WRITE CYCLE^[7]								
t _{WC}	Write Cycle Time	35		45		55		ns
t _{SCS}	\overline{CS} LOW to Write End	30		40		50		ns
t _{AW}	Address Set-Up to Write End	30		40		50		ns
t _{HA}	Address Hold from Write End	2		2		2		ns
t _{SA}	Address Set-Up to Write Start	2		2		2		ns
t _{PWE}	\overline{WE} Pulse Width	30		35		45		ns
t _{SD}	Data Set-Up to Write End	20		25		35		ns
t _{HD}	Data Hold from Write End	2		2		2		ns
t _{LZWE}	\overline{WE} HIGH to Low Z	0		0		0		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[6]	0	15	0	15	0	15	ns

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed by design and not 100% tested.
- t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CS} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms (continued)
Write Cycle No. 2 (CS Controlled)^[7, 11]


1841-9

Note:

11. If CS goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.

Truth Table

CS	WE	OE	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect



Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CYM1841PM-45C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7-45C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN-45C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APM-45C	PM02	64-Pin Plastic SIMM Module	
	CYM1841AP7-45C	PM04	72-Pin Plastic SIMM Module	
	CYM1841APN-45C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APZ-45C	PZ03	64-Pin Plastic ZIP Module	
55	CYM1841PM-55C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7-55C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN-55C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APM-55C	PM02	64-Pin Plastic SIMM Module	
	CYM1841AP7-55C	PM04	72-Pin Plastic SIMM Module	
	CYM1841APN-55C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APZ-55C	PZ03	64-Pin Plastic ZIP Module	

Document #: 38-M-00031-D

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-10°C to +85°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +V _{CC}

DC Input Voltage -0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

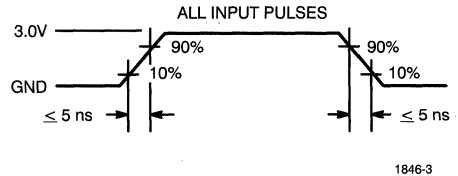
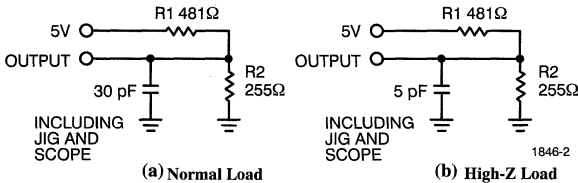
Parameter	Description	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage		-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, CS _N ≤ V _{IL}		800	mA
I _{SB1}	Automatic CS Power-Down Current ^[1]	Max. V _{CC} , CS ≥ V _{IH} , Min. Duty Cycle = 100%		240	mA
I _{SB2}	Automatic CS Power-Down Current ^[1]	Max. V _{CC} , CS ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V, or V _{IN} ≤ 0.2V		40	mA

Capacitance^[2]

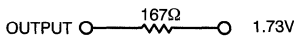
Parameter	Description	Test Conditions	Max.	Unit
C _{INA}	Input Capacitance (\overline{WE} , \overline{OE} , A ₀₋₁₈)	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	40	pF
C _{INB}	Input Capacitance (\overline{CS})		20	pF
C _{OUT}	Output Capacitance		20	pF

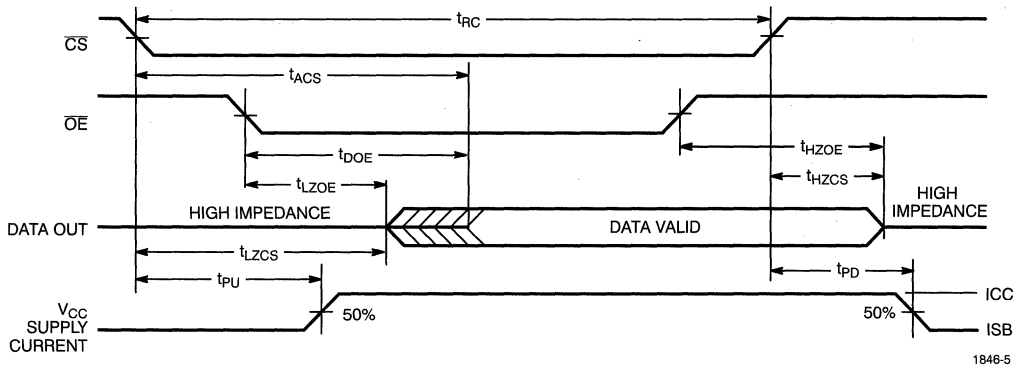
Notes:

1. A pull-up resistor to V_{CC} on the \overline{CS} input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

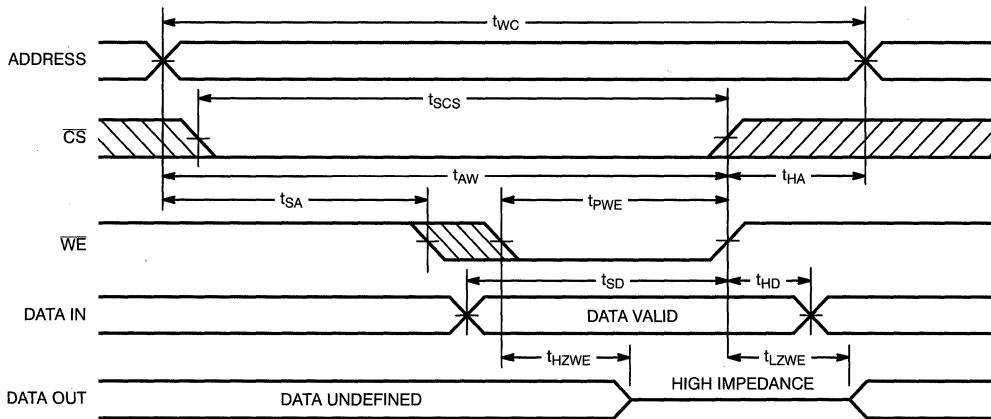
AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT



Switching Waveforms (continued)
Read Cycle No. 2^[7, 9]


1846-5

Write Cycle No. 1 (\overline{WE} Controlled)^[6]


1846-6

Notes:

7. \overline{WE} is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS} = V_{IL}$, and $\overline{OE} = V_{IL}$.

9. Address valid prior to or coincident with \overline{CS} transition LOW.



1,024K x 32 Static RAM Module

Features

- High-density 32-megabit SRAM module
- 32-bit Standard Footprint supports densities from 16K x 32 through 1M x 32
- High-speed CMOS SRAMs — Access time of 25 ns
- Low active power — 6.6W (max.) at 25 ns
- 72 pins
- Available in ZIP, SIMM, or angled SIMM format

Functional Description

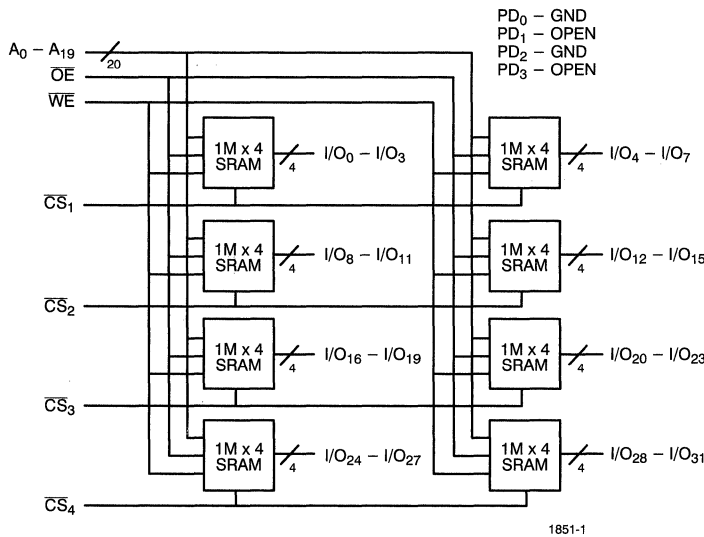
The CYM1851 is a high-performance 32-megabit static RAM module organized as 1,024K words by 32 bits. This module is constructed from eight 1,024K x 4 SRAMs in SOJ packages mounted on an epoxy laminate substrate. Four chip selects are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The CYM1851 is designed for use with standard 72-pin SIMM sockets. The pin-

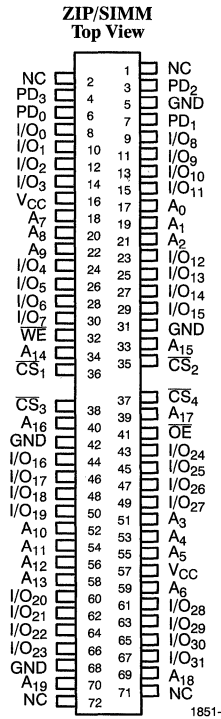
out is downward compatible with the 64-pin JEDEC ZIP/SIMM module family (CYM1821, CYM1831, CYM1836, and CYM1841). Thus, a single motherboard design can be used to accommodate memory depth ranging from 16K words (CYM1821) to 1,024K words (CYM1851).

Presence detect pins (PD₀ – PD₃) are used to identify module memory density in applications where modules with alternate word depths can be interchanged.

Logic Block Diagram



Pin Configuration



Selection Guide

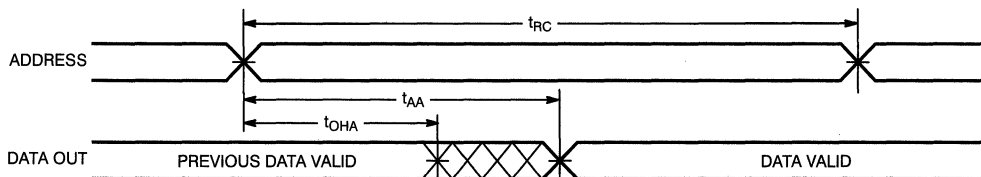
	1851-25	1851-30	1851-35
Maximum Access Time (ns)	25	30	35
Maximum Operating Current (mA)	1200	1200	960
Maximum Standby Current (mA)	480	480	480

Switching Characteristics Over the Operating Range^[3]

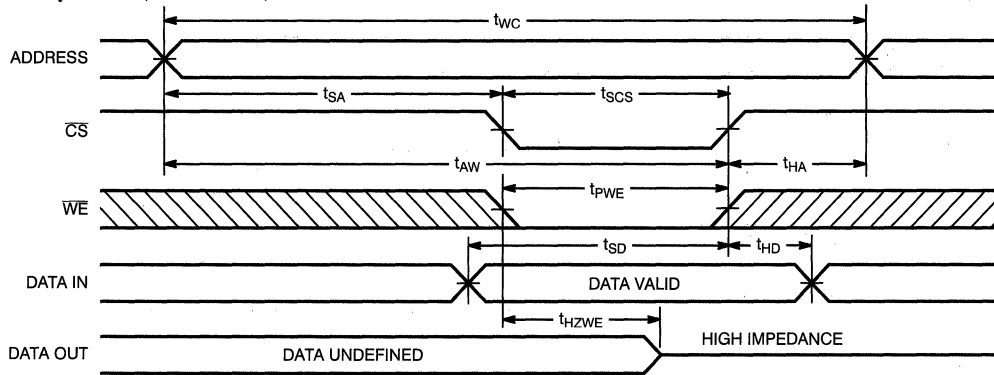
Parameter	Description	1851-25		1851-30		1851-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		30		35		ns
t_{AA}	Address to Data Valid		25		30		35	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	\overline{CS} LOW to Data Valid		25		30		35	ns
t_{DOE}	\overline{OE} LOW to Data Valid		15		20		25	ns
t_{LZOE}	\overline{OE} LOW to Low Z	0		0		0		ns
t_{HZOE}	\overline{OE} HIGH to High Z		12		12		12	ns
t_{LZCS}	\overline{CS} LOW to Low Z ^[4]	10		10		10		ns
t_{HZCS}	\overline{CS} HIGH to High Z ^[4,5]		12		12		12	ns
t_{PD}	\overline{CS} HIGH to Power-Down		25		30		35	ns
WRITE CYCLE^[6]								
t_{WC}	Write Cycle Time	25		30		35		ns
t_{SCS}	\overline{CS} LOW to Write End	20		25		30		ns
t_{AW}	Address Set-Up to Write End	20		25		30		ns
t_{HA}	Address Hold from Write End	3		3		3		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	\overline{WE} Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	15		15		20		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	\overline{WE} HIGH to Low Z	0		0		0		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[5]	0	12	0	12	0	12	ns

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
- t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CS} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms
Read Cycle No. 1^[7,8]


1851-5

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{CS} Controlled)^[6, 10]


1851-8

Note:

 10. If \overline{CS} goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.

Truth Table

\overline{CS}	\overline{WE}	\overline{OE}	Inputs/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
25	CYM1851PM-25C	PM04	72-Pin Plastic SIMM Module	Commercial
	CYM1851PN-25C	PN04	72-Pin Plastic Angled SIMM Module	
	CYM1851PZ-25C	PZ09	72-Pin Plastic ZIP Module	
30	CYM1851PM-30C	PM04	72-Pin Plastic SIMM Module	Commercial
	CYM1851PN-30C	PN04	72-Pin Plastic Angled SIMM Module	
	CYM1851PZ-30C	PZ09	72-Pin Plastic ZIP Module	
35	CYM1851PM-35C	PM04	72-Pin Plastic SIMM Module	Commercial
	CYM1851PN-35C	PN04	72-Pin Plastic Angled SIMM Module	
	CYM1851PZ-35C	PZ09	72-Pin Plastic ZIP Module	

Document #: 38-M-00052-A



This is an abbreviated datasheet. Contact a Cypress representative for complete specifications.

CYM7420
CYM7421

82420 PCIs et-Compatible Level II Cache Modules

Features

- 128 Kbytes (CYM7420), 256 Kbytes (CYM7421) cache module organized as 32K by 32 or 64K by 32
- Tag width of 7/8 bits plus valid bit
- Independent dirty bit
- Operates with systems based on the Intel™ 82420 core logic
- Zero-wait state operation at 33 Mhz
- Constructed using standard asynchronous SRAMs
- 112-pin Burndy Connector, Part Number CELP2X56SC3Z48
- Single 5V (±5%) power supply

- TTL-compatible inputs/outputs

Functional Description

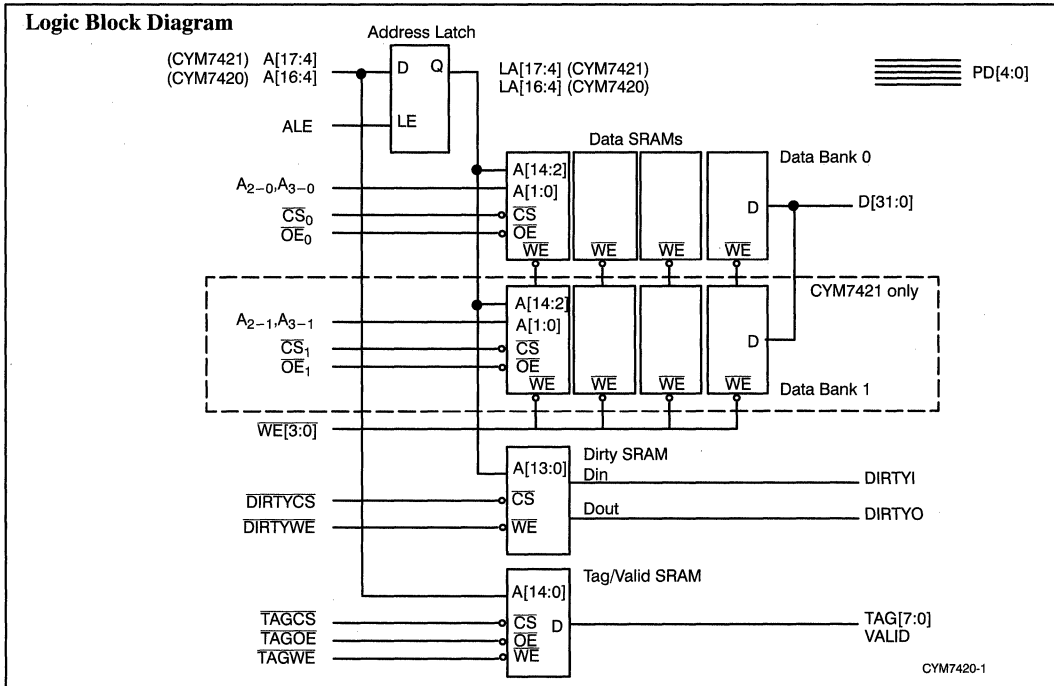
The CYM7420 module series is a family of cache memory subsystems for Intel 486-based systems. Each module contains either one or two banks of 32-bit wide Data SRAM, 8K/32K entries of 7/8-bit tag, and one Valid bit, and a single bit wide, separate I/O Dirty SRAM. CYM7420 has 8-bit tags, while CYM7421 support 7-bit tags. The address signals for the Data and Dirty SRAMs are latched.

The modules are configured as a 112-pin card-edge memory module. It is

constructed using standard asynchronous SRAMs in SOJ packages mounted on a multilayer epoxy laminate (FR4) substrate. The module dimensions are 3.145 inches long by 1.105 inches high by 0.365 inches thick.

These modules are designed for zero wait state operation in 486-based systems operating at a bus speed of 33 Mhz. They are designed for compatibility with the Intel 82420 PCIs et and other chip sets. The baseline speed grade is built using 12 nanosecond Tag SRAMs and 20 nanosecond Data SRAMs.

Logic Block Diagram



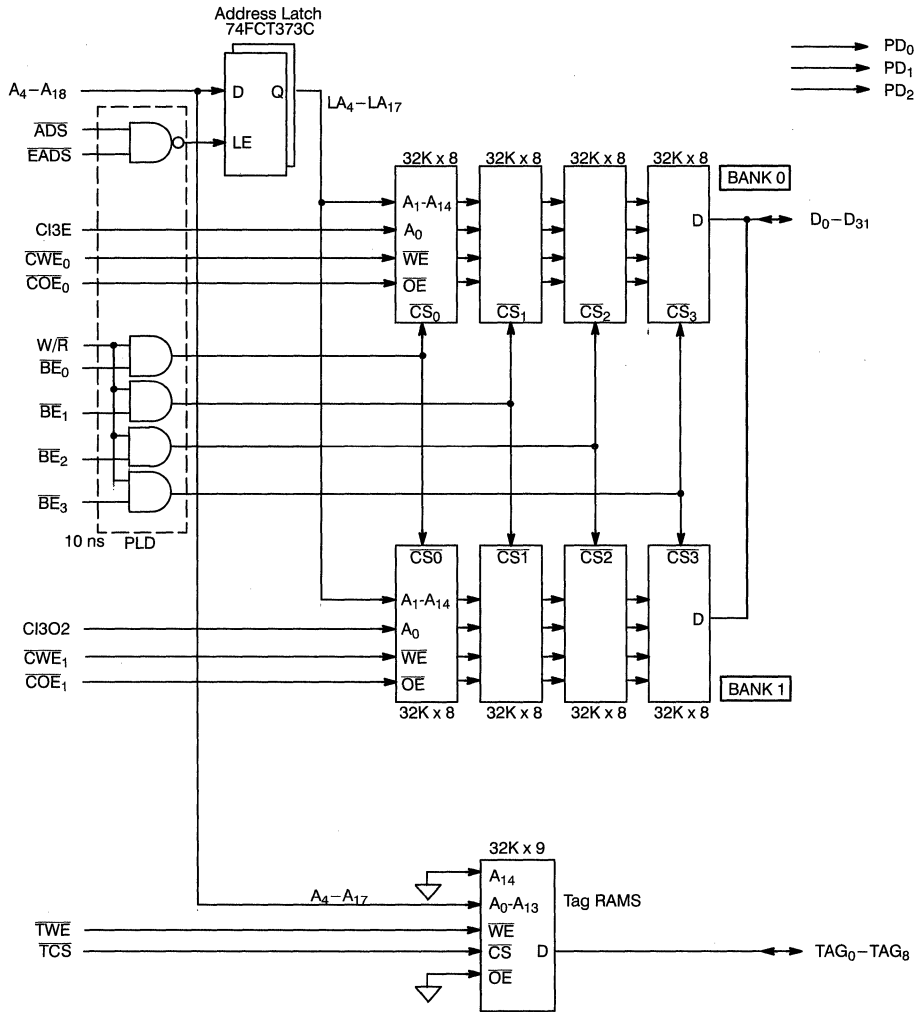
Selection Guide

	CYM7420PB-20	CYM7421PB-20
Cache Size (KB)	128	256
Data SRAM (ns)	20	20
Dirty SRAM (ns)	15	15
Tag/Valid SRAM (ns)	12	12

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Document #: 38-M-00065-A

Logic Block Diagram CYM7425



CYM7424-2

Pin Descriptions

Name	Description
A ₄ –A ₁₈	Cache Address Inputs
CI3O2, CI3E	Cache Index Address Inputs
D ₀ –D ₃₁	Cache Data Input/Outputs
\overline{BE}_0 – \overline{BE}_3	Byte Enable Inputs
\overline{CWE}_0	Bank 0 Write Enable Input
\overline{CWE}_1	Bank 1 Write Enable Input
\overline{COE}_0	Bank 0 Output Enable
\overline{COE}_1	Bank 1 Output Enable
W/ \overline{R}	Write/Read Input
\overline{ADS}	CPU Address Strobe Input
\overline{EADS}	External Address Strobe Input
TAG ₀ –TAG ₈	Tag Data Input/Output
\overline{TWE}	Tag Write Input
\overline{TCE}	Tag Chip Enable Input
PD ₀ –PD ₂	Presence Detect Pins
NC	No Connection

Presence Detect Table

	PD ₂	PD ₁	PD ₀
CYM7424	NC	V _{CC}	NC
CYM7425	NC	NC	V _{CC}

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature –55°C to +125°C
 Ambient Temperature with
 Power Applied –0°C to +70°C
 Supply Voltage to Ground Potential –0.5V to +7.0V
 DC Voltage Applied to Outputs
 in High Z State –0.5V to +7.0V

DC Input Voltage –0.5V to +7.0V
 Output Current into Outputs (LOW) 20 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 5%



82420 PCIsset-Compatible Level II Cache Module Family

Features

- Cache size 128 Kbytes or 256 Kbytes
- Tag width of 7 bits plus valid bit
- Independent dirty bit
- Operates with systems based on the Intel 82420 core logic
- Zero-wait state operation at 33 MHz
- Constructed using standard asynchronous SRAMs
- 112-pin Burndy Connector, Part Number CELP2X56SC3Z48
- Single 5V ($\pm 5\%$) power supply
- TTL-compatible inputs/outputs

Functional Description

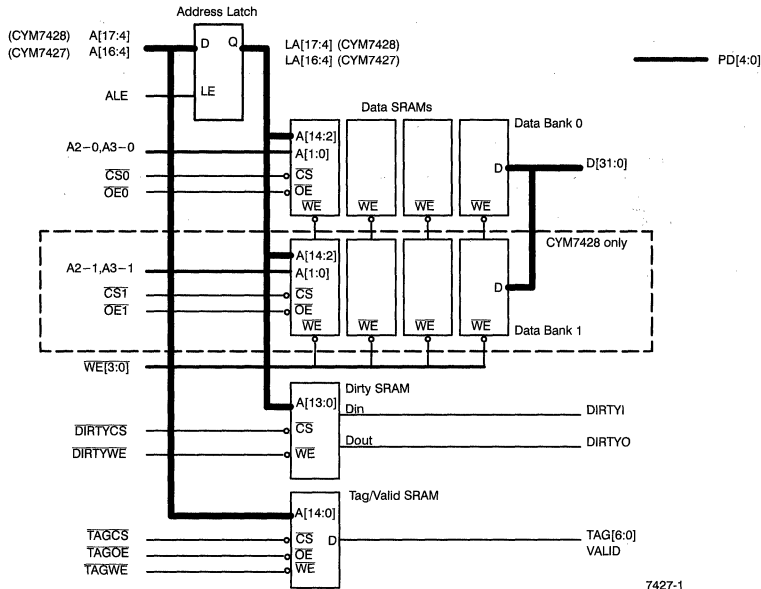
The CYM7427/28 module series is a family of cache memory subsystems for Intel 486-based systems. The CYM7427 (128 Kbytes) contains one memory bank organized as 32K by 32. The CYM7428 (256 Kbytes) contains two banks for interleaved operation. In addition, each module contains one 8-bit wide SRAM, supporting a 7-bit tag and one Valid bit, and a single-bit, separate I/O SRAM supporting a Dirty bit. The address signals for the Data and Dirty SRAMs are latched.

The 7427/28 is configured as a 112-pin card-edge memory module. It is con-

structed using standard asynchronous SRAMs in SOJ packages mounted on an epoxy laminate substrate. The module dimensions are 3.145 inches long by 1.105 inches high by 0.365 inches thick.

These modules are designed for zero-wait-state operation in 486-based systems operating at a bus speed of 33 MHz. They are designed for compatibility with the Intel 82420 PCIsset and other chipsets. The baseline speed grade is built using 12-nanosecond Tag SRAMs and 20-nanosecond Data SRAMs.

Logic Block Diagram

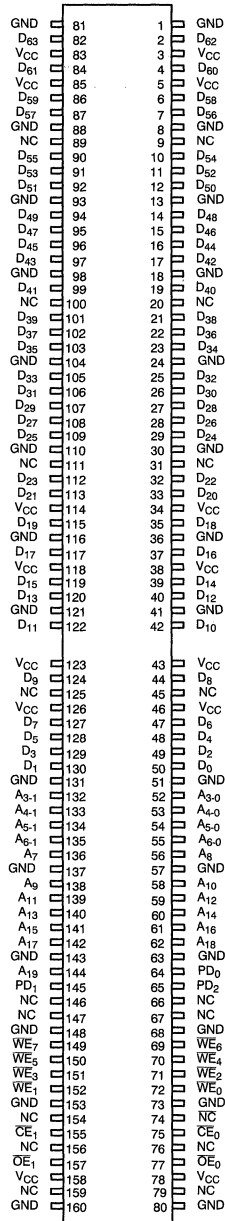


7427-1

Selection Guide

	CYM7427PB-20	CYM7428PB-20
Cache Size (KB)	128	256
Data SRAM (ns)	20	20
Dirty SRAM (ns)	15	15
Tag/Valid SRAM (ns)	12	12

Document #: 38-M-00077

Pin Configuration
Dual Read-out SIMM
Top View


7432b-2



This is an abbreviated datasheet. Contact a Cypress representative for complete specifications.

CYM7450
CYM7451

128K/256K Cache Module for VLSI VL82C483 Chipset

Features

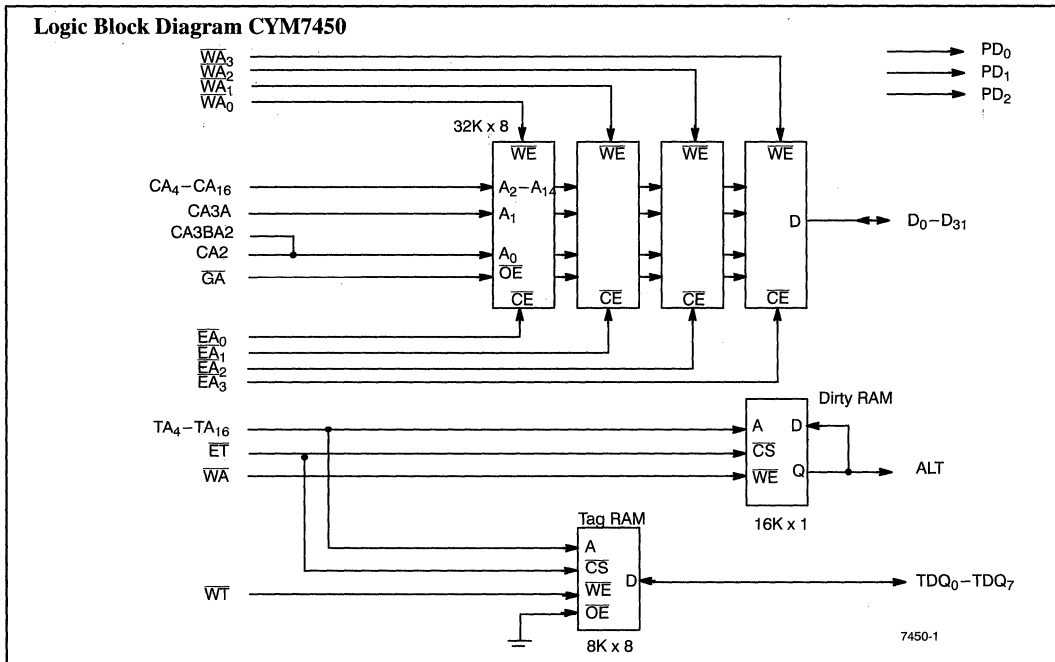
- 128 Kbyte (CYM7450) or 256 Kbyte (CYM7451) secondary cache module organized as 32K by 32 or 64K by 32
- Ideal for Intel™ 486-based systems with the VLSI VL82C483 chipset
- Zero-wait-state operations at 33 MHz
- Constructed using cost-effective CMOS asynchronous SRAMs
- On-board decoupling capacitors offer improved noise immunity
- 128-position Dual Readout SIMM
- 5V ($\pm 5\%$) power supply
- TTL-compatible inputs/outputs

Functional Description

These modules are designed specially to function as the secondary cache in Intel 486-based systems with the VLSI VL82C483 chipset. Each module contains either one or two banks of 32-bit wide data SRAMs, an 8-bit wide tag RAM, and a single-bit dirty RAM with separate I/O. Each byte in the data cache can be written individually. Separate address lines for the data RAMs and the tag/dirty RAMs are supported. Asynchronous CMOS SRAMs are used to provide a low-cost, low-power, and zero-wait-state solution for CPU speeds up to 33 MHz.

Multiple ground pins and on-board decoupling capacitors ensure maximum protection from noise.

Each module interfaces with the rest of the system via a 128-pin connector. All components on the cache module are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The package dimensions are 3.85" x 0.33" x 1.07". All inputs and outputs of the CYM7450 and CYM7451 cache modules are TTL compatible and operate from a single 5V power supply. The contact pins are plated with 100 micro-inches of nickel covered by 5 micro-inches of gold flash.



Selection Guide

	CYM7450PB-20C	CYM7451PB-20C
Cache Size (KB)	128	256
Data SRAM (ns)	20	20
Dirty SRAM (ns)	15	15
Tag/Valid SRAM (ns)	15	15

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Document #: 38-M-00066-A



PRELIMINARY

CYM74AP54
CYM74SP54
CYM74SP55

Intel™ 82430NX Chipset Level II Cache Module Family

Features

- Pin-compatible secondary cache module family
- Asynchronous (CYM74AP54) or synchronous (CYM74SP54, CYM74SP55) configurations with presence and configuration detect pins
- Ideal for Intel P54C-based systems with the 82430NX (Neptune) chipset
- Operates at 60 and 66 MHz
- Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs
- 160-position Burndy DIMM CELP2X80SC3Z48 connector
- 3.3V inputs/outputs

Functional Description

This family of secondary cache modules is designed for Intel P54C systems with the 82430NX (Neptune) chipset.

CYM74AP54 is an asynchronous 256-Kbyte cache module that provides a low-cost, high-performance solution for CPU bus speeds up to 66 MHz. The CYM74AP54 is organized as 32K by 64.

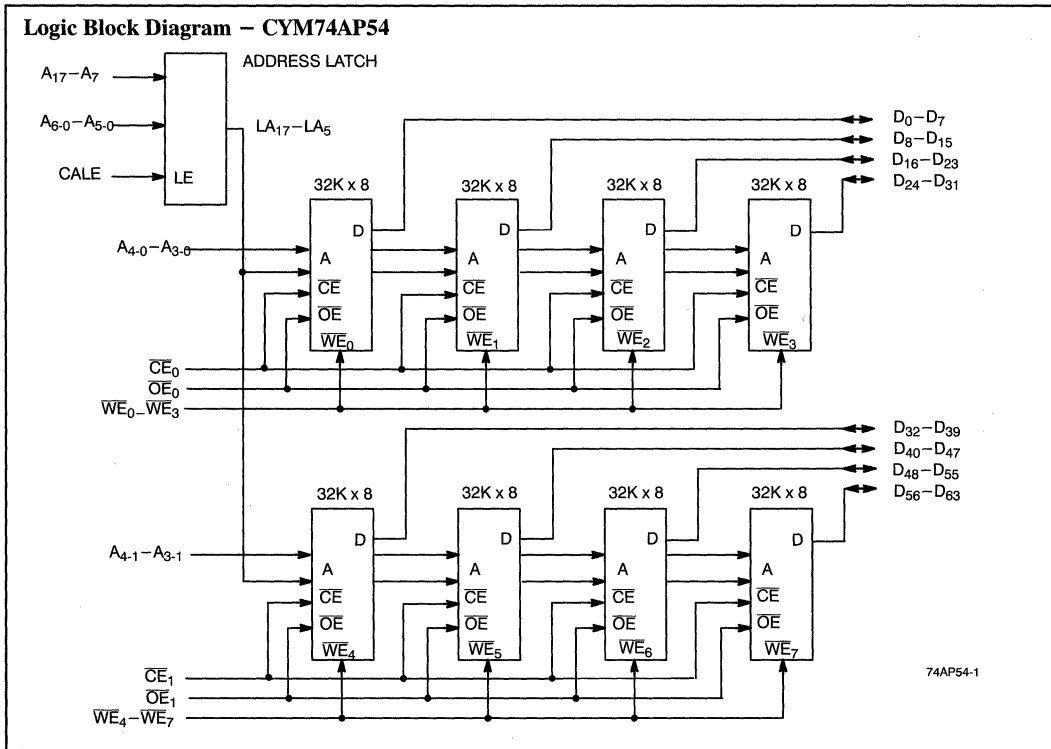
The CYM74SP54 and CYM74SP55 are synchronous cache modules that provide zero wait-state performance at a bus speed of 66 MHz. The CYM74SP54 is a 256-Kbyte cache module with byte parity.

The CYM74SP55 is a 512-Kbyte cache module with byte parity.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. All inputs and outputs of this family of modules are (3.3V) TTL compatible. Provisions are made on-board to support both mixed-mode (5V/3.3V) and 3.3V only SRAMs. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.

Logic Block Diagram – CYM74AP54



74AP54-1

Intel is a trademark of Intel Corporation.



Pin Configuration

Dual Read-Out SIMM (DIMM)

Top View

GND	81	1	GND
D ₆₃	82	2	D ₆₂
V _{CC}	83	3	V _{CCQ}
D ₆₁	84	4	D ₆₀
V _{CC}	85	5	V _{CCQ}
D ₅₉	86	6	D ₅₈
D ₅₇	87	7	D ₅₆
GND	88	8	GND
DP ₇ (74SP5X) / NC (74AP54)	89	9	NC (74AP54) / DP ₆ (74SP5X)
D ₅₅	90	10	D ₅₄
D ₅₃	91	11	D ₅₂
D ₅₁	92	12	D ₅₀
GND	93	13	GND
D ₄₉	94	14	D ₄₈
D ₄₇	95	15	D ₄₆
D ₄₅	96	16	D ₄₄
D ₄₃	97	17	D ₄₂
GND	98	18	GND
D ₄₁	99	19	D ₄₀
DP ₅ (74SP5X) / NC (74AP54)	100	20	NC (74AP54) / DP ₄ (74SP5X)
D ₃₉	101	21	D ₃₈
D ₃₇	102	22	D ₃₆
D ₃₅	103	23	D ₃₄
GND	104	24	GND
D ₃₃	105	25	D ₃₂
D ₃₁	106	26	D ₃₀
D ₂₉	107	27	D ₂₈
D ₂₇	108	28	D ₂₆
D ₂₅	109	29	D ₂₄
GND	110	30	GND
DP ₃ (74SP5X) / NC (74AP54)	111	31	NC (74AP54) / DP ₂ (74SP5X)
D ₂₃	112	32	D ₂₂
D ₂₁	113	33	D ₂₀
V _{CC}	114	34	V _{CCQ}
D ₁₉	115	35	D ₁₈
GND	116	36	GND
D ₁₇	117	37	D ₁₆
V _{CC}	118	38	V _{CCQ}
D ₁₅	119	39	D ₁₄
D ₁₃	120	40	D ₁₂
GND	121	41	GND
D ₁₁	122	42	D ₁₀
V _{CC}	123	43	V _{CCQ}
D ₉	124	44	D ₈
DP ₁ (74SP5X) / NC (74AP54)	125	45	NC (74AP54) / DP ₀ (74SP5X)
V _{CC}	126	46	V _{CCQ}
D ₇	127	47	D ₆
D ₅	128	48	D ₄
D ₃	129	49	D ₂
D ₁	130	50	D ₀
GND	131	51	GND
A ₃₋₁	132	52	A ₃₋₀
A ₄₋₁	133	53	A ₄₋₀
A ₅₋₁	134	54	A ₅₋₀
A ₆₋₁	135	55	A ₆₋₀
A ₇	136	56	A ₈
GND	137	57	GND
A ₉	138	58	A ₁₀
A ₁₁	139	59	A ₁₂
A ₁₃	140	60	A ₁₄
A ₁₅	141	61	A ₁₆
A ₁₇	142	62	A ₁₈
GND	143	63	GND
(Reserved A ₁₉) NC	144	64	PD ₀
PD ₁	145	65	PD ₂
CLK ₀ (74SP5X) / NC (74AP54)	146	66	NC (74AP54) / CLK ₁ (74SP5X)
(Reserved CLK ₂) NC	147	67	NC (Reserved CLK ₃)
GND	148	68	GND
WE ₇	149	69	WE ₆
WE ₅	150	70	WE ₄
WE ₃	151	71	WE ₂
WE ₁	152	72	WE ₀
GND	153	73	GND
ADSC _T (74SP5X) / NC (74AP54)	154	74	CALE (74AP54) / ADSC ₀ (74SP5X)
CE ₁	155	75	CE ₀
ADV _T (74SP5X) / NC (74AP54)	156	76	NC (74AP54) / ADV ₀ (74SP5X)
OE ₁	157	77	OE ₀
V _{CC}	158	78	V _{CCQ}
ADSP _T (74SP5X) / NC (74AP54)	159	79	NC (74AP54) / ADSP ₀ (74SP5X)
GND	160	80	GND

74AP54-3



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -55°C to +125°C
 Ambient Temperature with Power Applied -0°C to +70°C
 3.3V Supply Voltage to Ground Potential -0.5V to +4.6V
 5V Supply Voltage to Ground Potential -0.5V to +5.25V
 DC Voltage Applied to Outputs in High Z State -0.5V to +4.6V

DC Input Voltage -0.5V to +4.6V
 Output Current into Outputs (LOW) 20 mA

Operating Range

Range	Ambient Temperature	VCC
Commercial	0°C to +70°C	5V ± 5% 3.3V ± 5%

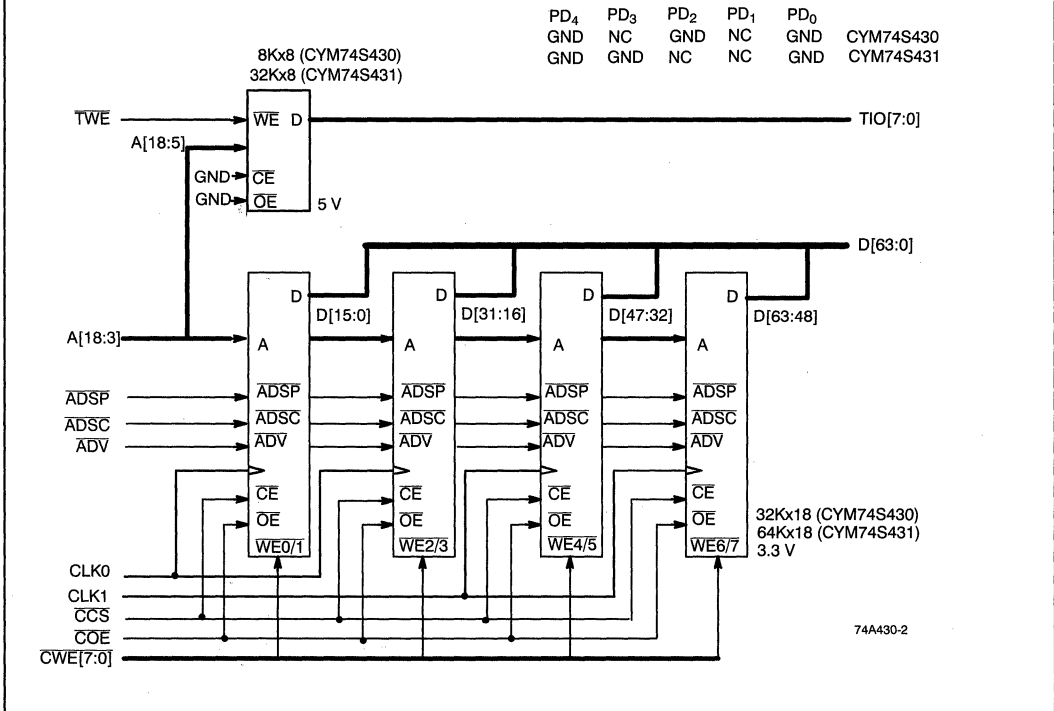
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V _{IH}	Input HIGH Voltage		2.2	V _{CCQ} + 0.3	V
V _{IL}	Input LOW Voltage		-0.3	0.8	V
V _{OH}	Output HIGH Voltage	V _{CC} =Min. I _{OH} = -4 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} =Min. I _{OL} = 8 mA		0.4	V
I _{CC} (74AP54)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1500	mA
I _{CC} (74SP54)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1500	mA
I _{CC} (74SP55)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1500	mA

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
60	CYM74AP54PM-60C	PM25	160-Pin Dual-Readout SIMM	Asynchronous, 15-ns Access RAMs	Commercial
	CYM74SP54PM-60C	PM26	160-Pin Dual-Readout SIMM	Synchronous	
	CYM74SP55PM-60C	PM26	160-Pin Dual-Readout SIMM	Synchronous	
66	CYM74AP54PM-66C	PM25	160-Pin Dual-Readout SIMM	Asynchronous, 12-ns Access RAMs	Commercial
	CYM74SP54PM-66C	PM26	160-Pin Dual-Readout SIMM	Synchronous	
	CYM74SP55PM-66C	PM26	160-Pin Dual-Readout SIMM	Synchronous	

Document #: 38-M-00070-A

Logic Block Diagram – CYM74S430/CYM74S431^[1]

Selection Guide

	74A430-50	74A430-60	74A430-66	74S430-50	74S430-60	74S430-66	74S431-50	74S431-60	74S431-66
Cache Size	256 KB			256 KB			512 KB		
System Clock (MHz)	50	60	66	50	60	66	50	60	66
RAM Type	Async			Sync Burst			Sync Burst		
Data t _{AA}	20 ns	17 ns	15 ns						
Data t _{CDV}				13.5 ns	10 ns	8.5 ns	13.5 ns	10 ns	8.5 ns
Tag t _{AA}	30 ns	20 ns	15 ns	30 ns	20 ns	15 ns	30 ns	20 ns	15 ns

Notes:

- A18 is not used by CYM74S430. DP pins are pulled high through 10 KΩ

Pin Definitions

Signal Name	Description
V _{CC}	5V Supply
V _{CCQ}	3.3V Supply
GND	Ground
A[18:3]	Addresses from processor
CAA[4:3]	Lower two address bits for bank 0 of CYM74A430
CAB[4:3]	Lower two address bits for bank 1 of CYM74A430
\overline{CS}	Chip Select (CYM74A430 only)
\overline{CCS}	Chip Select for CYM74S430 and CYM74S431
COE	Output Enable
\overline{CWE} [7:0]	Byte Write Enables
CALE	Latch Enable – CYM74A430 only
PD ₀ –PD ₄	Presence Detect output pins
D[63:0]	Data lines from processor
TIO[7:0]	Tag data bits
TWE	Tag Written Enable signal
\overline{ASDP}	Processor Address Strobe for CYM74S430 and CYM74S431
\overline{ADSC}	Cache Controller Address Strobe for CYM74S430 and CYM74S431
\overline{ADV}	Burst Address Advance for CYM74S430 and CYM74S431
CLK[1:0]	Clock signals for CYM74S430 and CYM74S431
NC	Signal not connected on module.
RSVD	Reserved.

Presence Detect Pins

	PD ₄	PD ₃	PD ₂	PD ₁	PD ₀
Asynchronous – CYM74A430	GND	NC	GND	GND	NC
Synchronous – CYM74S430	GND	NC	GND	NC	GND
Synchronous – CYM74S431	GND	GND	NC	NC	GND



CYM74A550, CYM74A551 PRELIMINARY CYM74S550, CYM74S551

OPTi Viper™ Chipset Level II Cache Module Family

Features

- Pin-compatible secondary cache module family
- Asynchronous (CYM74A550, CYM74A551) or synchronous (CYM74S550, CYM74S551) modules with presence and configuration detect pins
- Ideal for Intel™ P54C-based systems with the OPTi Viper™ chipset
- Operates at 50, 60, and 66 MHz
- Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs
- 160-position Burndy DIMM CELP2X80SC3Z48 connector
- 3.3V inputs/outputs

Functional Description

This family of secondary cache modules is designed for Intel P54C systems with the OPTi Viper chipset.

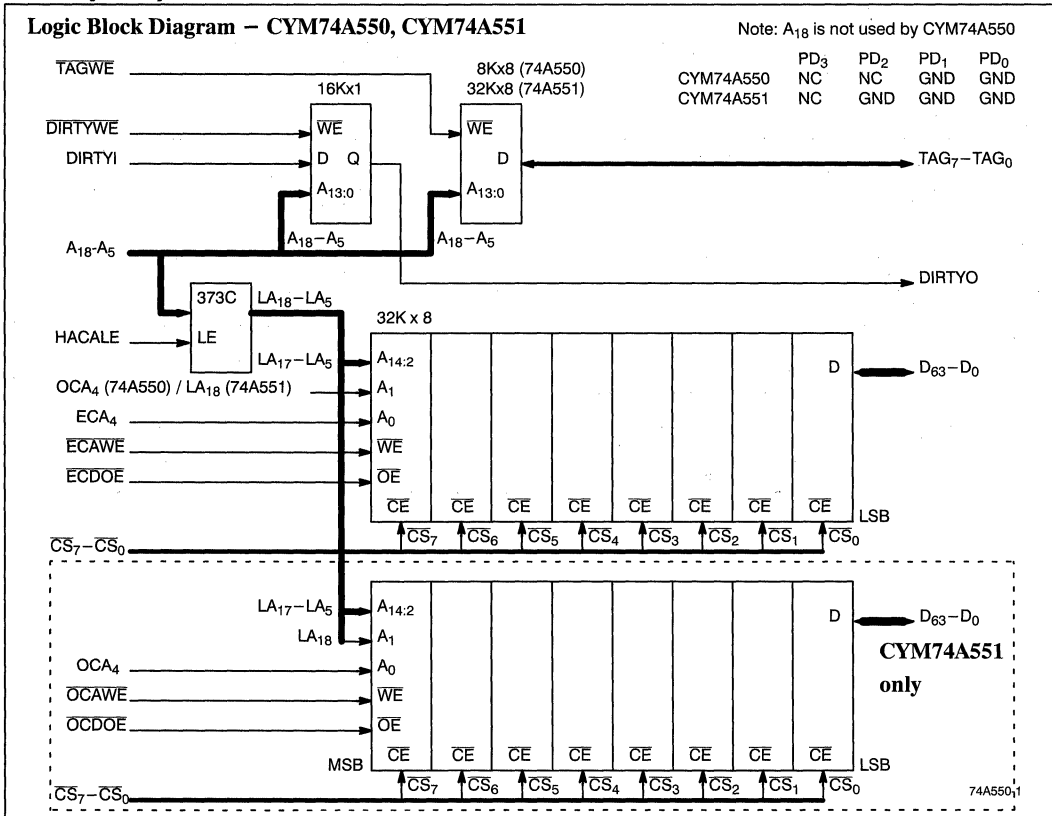
CYM74A550 and CYM74A551 are low-cost asynchronous cache modules that provide 256-Kbytes and 512-Kbytes of cache respectively. These modules offer 3-2-2-2 performance at CPU bus speeds up to 66 MHz.

The CYM74S550 and CYM74S551 are high performance synchronous cache modules that provide 256-Kbytes and 512-Kbytes of cache respectively. These modules support 3-1-1-1 performance at 66 MHz.

All of these modules include storage for 8 bits of tag and one dirty bit.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. All inputs and outputs of this family of modules are (3.3V) TTL compatible. Provisions are made on-board to support both mixed-mode (5V/3.3V) and 3.3V-only SRAMs. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.



Viper is a trademark of OPTi.
Intel is a trademark of Intel Corporation.



Pin Configuration

Dual Read-Out SIMM (DIMM)
 Top View

GND	81	1	GND
D ₆₃	82	2	D ₆₂
D ₆₁	83	3	D ₆₀
V _{CC}	84	4	V _{CCQ}
D ₅₉	85	5	D ₅₈
D ₅₇	86	6	D ₅₆
D ₅₅	87	7	D ₅₄
GND	88	8	GND
D ₅₃	89	9	D ₅₂
D ₅₁	90	10	D ₅₀
D ₄₉	91	11	D ₄₈
V _{CC}	92	12	V _{CCQ}
D ₄₇	93	13	D ₄₆
D ₄₅	94	14	D ₄₄
GND	95	15	GND
D ₄₃	96	16	D ₄₂
D ₄₁	97	17	D ₄₀
D ₃₉	98	18	D ₃₈
D ₃₇	99	19	D ₃₆
GND	100	20	GND
D ₃₅	101	21	D ₃₄
D ₃₃	102	22	D ₃₂
D ₃₁	103	23	D ₃₀
D ₂₉	104	24	D ₂₈
GND	105	25	GND
D ₂₇	106	26	D ₂₆
D ₂₅	107	27	D ₂₄
V _{CC}	108	28	V _{CCQ}
D ₂₃	109	29	D ₂₂
D ₂₁	110	30	D ₂₀
D ₁₉	111	31	D ₁₈
GND	112	32	GND
D ₁₇	113	33	D ₁₆
D ₁₅	114	34	D ₁₄
D ₁₃	115	35	D ₁₂
GND	116	36	GND
D ₁₁	117	37	D ₁₀
V _{CC}	118	38	V _{CCQ}
D ₉	119	39	D ₈
D ₇	120	40	D ₆
GND	121	41	GND
D ₅	122	42	D ₄
V _{CC}	123	43	V _{CCQ}
D ₃	124	44	D ₂
D ₁	125	45	D ₀
V _{CC}	126	46	V _{CCQ}
(74S55X) ADSC / (74A55X) ECA ₄	127	47	OCA ₄ (74A55X) / ADV (74S55X)
(74S55X) SYNC ₀ / (74A55X) ECAWE	128	48	OCAWE (74A55X) / SYNC ₁ (74S55X)
ECDOE	129	49	OCDOE
(74S55X) WE ₀ / (74A55X) CS ₀	130	50	CS ₁ (74A55X) / WE ₁ (74S55X)
GND	131	51	GND
(74S55X) WE ₂ / (74A55X) CS ₂	132	52	CS ₃ (74A55X) / WE ₃ (74S55X)
(74S55X) WE ₄ / (74A55X) CS ₄	133	53	CS ₅ (74A55X) / WE ₅ (74S55X)
V _{CC}	134	54	V _{CCQ}
(74S55X) WE ₆ / (74A55X) CS ₆	135	55	CS ₇ (74A55X) / WE ₇ (74S55X)
(74S55X) CLK / (74A55X) NC	136	56	HACALE (74A55X) / NC (74S55X)
GND	137	57	GND
DIRTYWE	138	58	TAGWE
(74S55X) A ₃ / (74A55X) NC	139	59	NC (74A55X) / A ₄ (74S55X)
A ₅	140	60	A ₆
A ₇	141	61	A ₈
GND	142	62	GND
A ₉	143	63	A ₁₀
A ₁₁	144	64	A ₁₂
A ₁₃	145	65	A ₁₄
V _{CC}	146	66	V _{CCQ}
A ₁₅	147	67	A ₁₆
A ₁₇	148	68	NC (74A55X) / A ₁₈ (74S55X)
(Reserved A ₁₉) NC	149	69	NC (Reserved A ₂₀)
GND	150	70	GND
DIRTY1	151	71	DIRTY0
TAG ₀	152	72	TAG ₁
V _{CC}	153	73	V _{CCQ}
TAG ₂	154	74	TAG ₃
TAG ₄	155	75	TAG ₅
GND	156	76	GND
TAG ₆	157	77	TAG ₇
PD ₀	158	78	PD ₁
PD ₂	159	79	PD ₃
V _{CC}	160	80	V _{CCQ}

74A550-3



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -55°C to +125°C
 Ambient Temperature with Power Applied -0°C to +70°C
 3.3V Supply Voltage to Ground Potential -0.5V to +4.6V
 5V Supply Voltage to Ground Potential -0.5V to +5.25V
 DC Voltage Applied to Outputs in High Z State -0.5V to +4.6V

DC Input Voltage -0.5V to +4.6V
 Output Current into Outputs (LOW) 20 mA

Operating Range

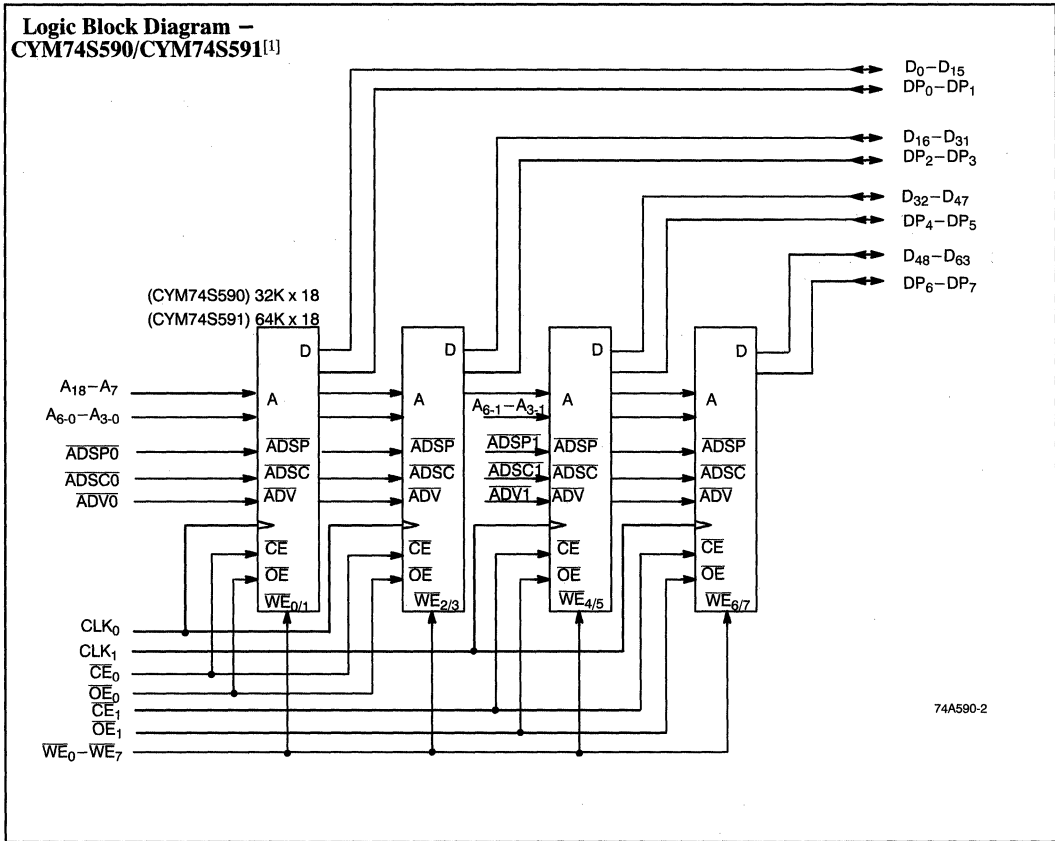
Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 5% 3.3V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V _{IH}	Input HIGH Voltage		2.2	V _{CCQ} + 0.3	V
V _{IL}	Input LOW Voltage		-0.3	0.8	V
V _{OH}	Output HIGH Voltage	V _{CC} =Min. I _{OH} = -4 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} =Min. I _{OL} = 8 mA		0.4	V
I _{CC} (74A550)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1500	mA
I _{CC} (74A551)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		2700	mA
I _{CC} (74S550)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1500	mA
I _{CC} (74S551)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1500	mA

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
50	CYM74A550PM-50C	PM31	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74A551PM-50C	PM32		Async 512 KB	
	CYM74S550PM-50C	PM33		Sync 256 KB	
	CYM74S551PM-50C	PM33		Sync 512 KB	
60	CYM74A550PM-60C	PM31	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74A551PM-60C	PM32		Async 512 KB	
	CYM74S550PM-60C	PM33		Sync 256 KB	
	CYM74S551PM-60C	PM33		Sync 512 KB	
66	CYM74A550PM-66C	PM31	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74A551PM-66C	PM32		Async 512 KB	
	CYM74S550PM-66C	PM33		Sync 256 KB	
	CYM74S551PM-66C	PM33		Sync 512 KB	

**Logic Block Diagram –
CYM74S590/CYM74S591⁽¹⁾**

Selection Guide

	74A590-60	74A590-66	74S590-60	74S590-66	74S591-60	74S591-66
Cache Size (KB)	256	256	256	256	512	512
System Clock (MHz)	60	66	60	66	60	66
RAM Clock	Asynchronous	Asynchronous	Synchronous	Synchronous	Synchronous	Synchronous
RAM Speed	$t_{AA}=15$ ns	$t_{AA}=15$ ns	$t_{CDV}=10.5$ ns	$t_{CDV}=8.5$ ns	$t_{CDV}=10.5$ ns	$t_{CDV}=8.5$ ns

Notes:

1. A18 is not used by CYM74S590..



Pin Definitions

Signal Name	Description
V _{CC}	5V Supply
V _{CCQ}	3.3V Supply
GND	Ground
A ₇ -A ₁₉	Addresses from processor
A ₃₋₀ , A ₄₋₀ , A ₅₋₀ , A ₆₋₀	Lower address from chip set for bank0, identical to the bank1 addresses
A ₃₋₁ , A ₄₋₁ , A ₅₋₁ , A ₆₋₁	Lower address from chip set for bank1, identical to the bank0 addresses
\overline{CE}_0 , \overline{CE}_1	Chip Enable (same signal)
\overline{OE}_0 , \overline{OE}_1	Output Enable (same signal)
\overline{WE}_0 , \overline{WE}_1 , \overline{WE}_2 , \overline{WE}_3 \overline{WE}_4 , \overline{WE}_5 , \overline{WE}_6 , \overline{WE}_7	Byte Write Enables
CALE	Latch Enable – CYM74A590 only
PD ₀ -PD ₂	Presence Detect pins
D ₀ -D ₆₃	Data lines from processor
DP ₀ -DP ₇	Data Parity lines (Optional), CYM74S590 or CYM74S591 only
ADSP ₀ , ADSP ₁	Processor Address Strobe, CYM74S590 or CYM74S591 only
ADSC ₀ , ADSC ₁	Cache Controller Address Strobe, CYM74S590 or CYM74S591 only
ADV ₀ , ADV ₁	Burst Address Advance – CYM74S590 or CYM74S591 only
CLK ₀ , CLK ₁ , CLK ₂ , CLK ₃	Clock signals
NC	Signal not connected on module.

Presence Detect Pins

	PD ₂	PD ₁	PD ₀
Asynchronous – CYM74A590	NC	GND	NC
Synchronous – CYM74S590	GND	GND	NC
Synchronous – CYM74S591	GND	GND	GND



This is an abbreviated datasheet. Contact a Cypress representative for complete specifications.

CYM9230
CYM9231

82420 PCIset-Compatible Level II Cache Modules

Features

- 128K-byte (CYM9230) or 256K-byte (CYM9231) cache module organized as 32K by 32 or 64K by 32
- Tag width of 9 bits plus valid bit
- Independent dirty bit
- Operates with systems based on the Intel™ 82420 core logic
- Zero-wait state operation at 33 Mhz
- Constructed using standard asynchronous SRAMs
- 112-pin Burndy Connector, Part Number CELP2X56SC3Z48
- Single 5V (±5%) power supply

• TTL-compatible inputs/outputs

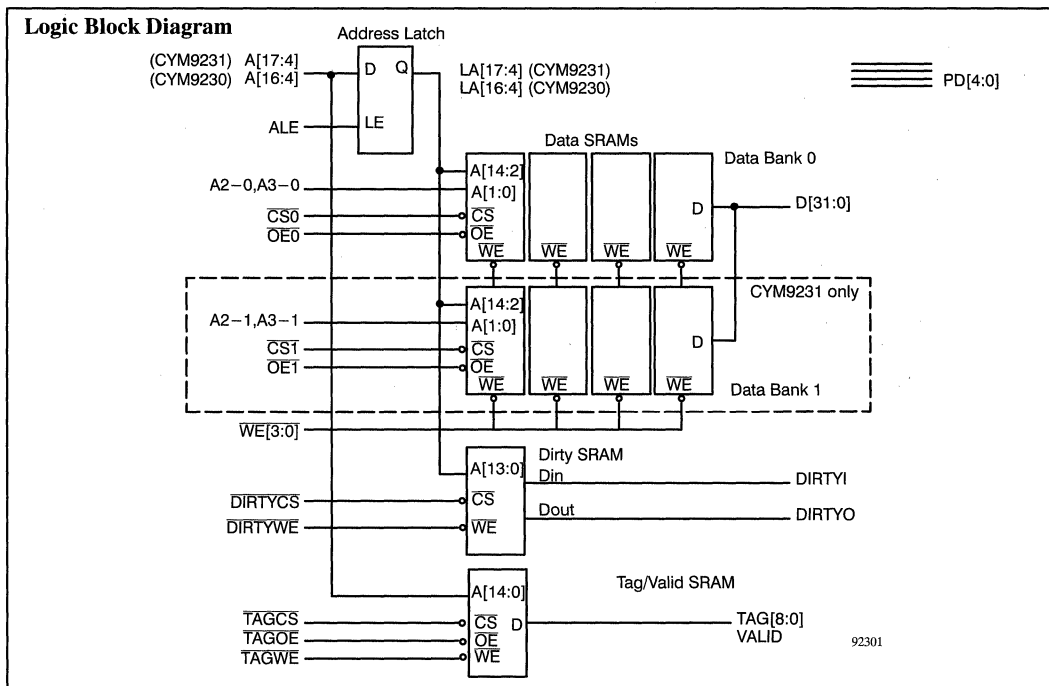
Functional Description

The CYM9230 module series is a family of cache memory subsystems for Intel 486-based systems. The CYM9230 (128Kbytes) contains one memory bank organized as 32K by 32. The CYM9231 (256Kbytes) contains two banks for interleaved operation. In addition, each module contains two SRAMs, supporting a 9-bit tag and valid bit, separate I/O SRAM supporting a dirty bit. The address signals for the Data and Dirty SRAMs are latched.

These modules are designed for zero wait state operation in 486-based systems operating at a bus speed of 33 Mhz. They are designed for compatibility with the Intel 82420 PCIset and other chip sets. The baseline speed grade is built using 12 nanosecond Tag SRAMs and 20 nanosecond Data SRAMs.

The modules are configured as a 112-pin card-edge memory module. It is constructed using standard asynchronous SRAMs in SOJ packages mounted on an epoxy laminate substrate. The module dimensions are 3.145 inches long by 1.105 inches high by 0.365 inches thick.

Logic Block Diagram



Selection Guide

	CYM9230PB-20	CYM9231PB-20
Cache Size (KB)	128	256
Data SRAM (ns)	20	20
Dirty SRAM (ns)	15	15
Tag/Valid SRAM (ns)	12	12

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Document #: 38-M-00064-A



CYPRESS

PRELIMINARY

CYM9244, CYM9245
CYM9246, CYM9247

128K/256K Cache Module Family for the OPTi 802GP Chipset

Features

- 128 Kbyte (CYM9244 & CYM9246), 256 Kbyte (CYM9245 & CYM9247), secondary cache modules
- Ideal for Intel™ 486 systems with the OPTi 802GP chipset
- Zero-wait-state operations at 33 MHz
- Constructed using cost-effective CMOS asynchronous SRAMs
- On-board decoupling capacitors offer improved noise immunity
- 112-position Burndy Connector, Part Number CELP2X56SC3Z48
- 5V (±5%) power supply

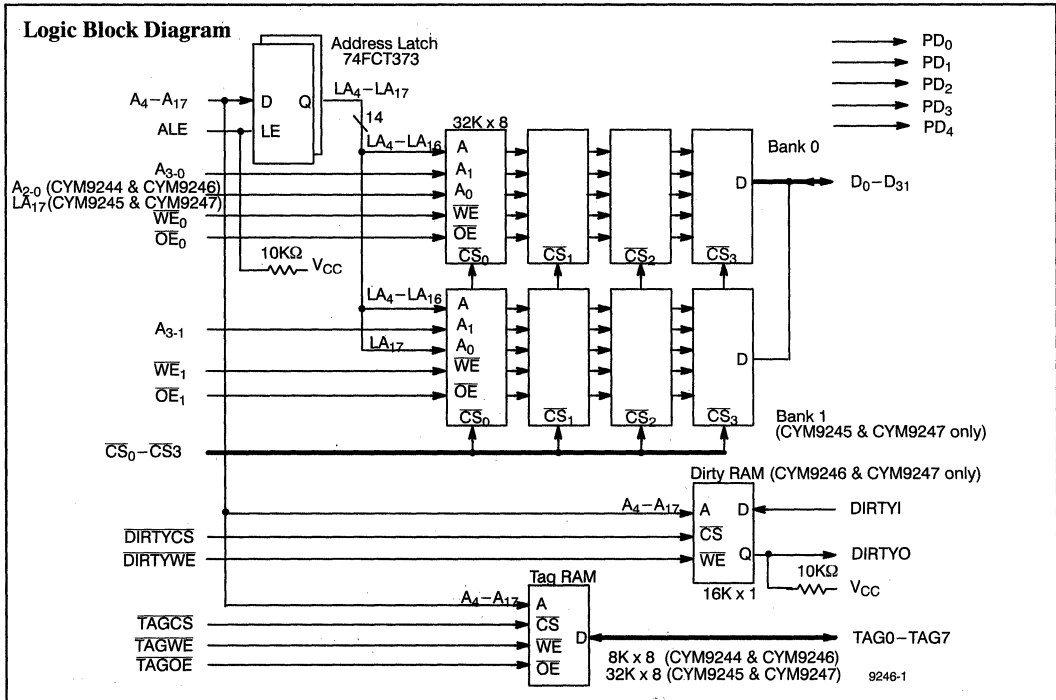
TTL-compatible inputs/outputs

Functional Description

These modules are designed to function as the secondary cache in Intel 486-based systems with the OPTi 802GP chipset. Each module contains either one or two banks of 32-bit wide data SRAMs, an 8-bit wide tag RAM, and a single-bit dirty RAM with separate I/O (CYM9246 and CYM9247 only). The addresses for the data SRAMs are buffered by an on-board latch. Asynchronous CMOS SRAMs are used to provide a low-cost, low-power, and zero-wait-state solution for CPU speeds up to 33 MHz. Multiple ground

pins and on-board decoupling capacitors ensure maximum protection from noise.

Each module interfaces with the rest of the system via a 112-pin Burndy connector. All components on the cache module are surface mounted on a multi-layer epoxy laminate (FR-4) board. The package dimensions are 3.15" x 0.365" x 1.1". All inputs and outputs of the CYM9244, CYM9245, CYM9246, and CYM9247 cache modules are TTL compatible and operate from a single 5V power supply. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.



Selection Guide

	CYM9244PB-20C	CYM9245PB-20C	CYM9246PB-20C	CYM9247PB-20C
Cache Size (KB)	128	256	128	256
Data SRAM (ns)	20	20	20	20
Dirty SRAM (ns)			20	20
Tag/Valid SRAM (ns)	15	15	15	15

Intel is a trademark of Intel Corporation.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-0°C to +70°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V

DC Input Voltage	-0.5V to +7.0V
Output Current into Outputs (LOW)	20 mA

Operating Range

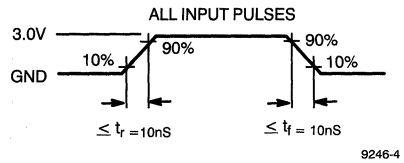
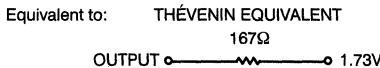
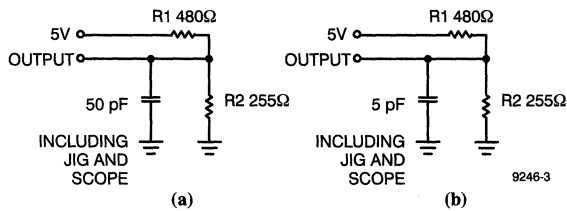
Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM9244, CYM9245, CYM9246, CYM9247		Unit
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =8.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} +0.3	V
V _{IL}	Input LOW Voltage		-0.5	0.8	V
I _{CC}	V _{CC} Operating Supply Current (CYM9244)	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		950	mA
I _{CC}	V _{CC} Operating Supply Current (CYM9245)	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1700	mA
I _{CC}	V _{CC} Operating Supply Current (CYM9246)	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1050	mA
I _{CC}	V _{CC} Operating Supply Current (CYM9247)	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1800	mA

Presence Detect Table

	PD ₄	PD ₃	PD ₂	PD ₁	PD ₀
CYM9244	NC	NC	NC	NC	GND
CYM9245	NC	NC	NC	GND	NC
CYM9246	GND	NC	NC	NC	GND
CYM9247	GND	NC	NC	GND	NC

AC Test Loads and Waveforms


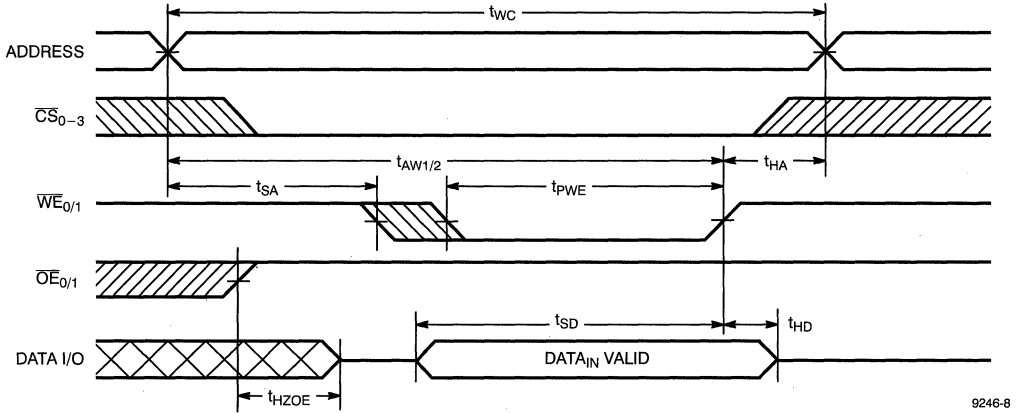


Switching Characteristics (continued)

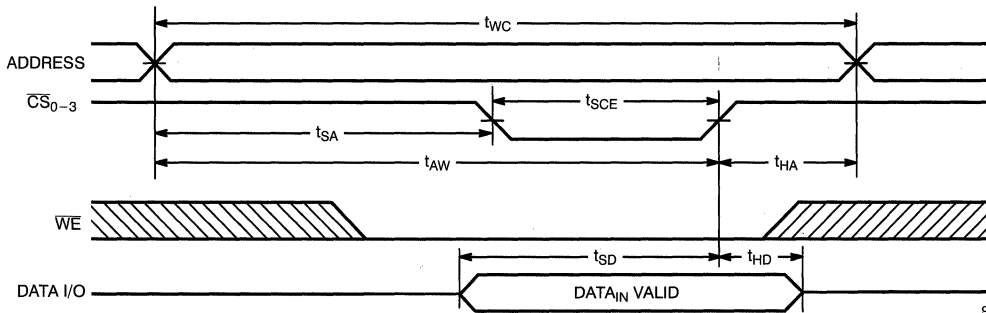
Parameters	Description	Min.	Max.	Units
Data SRAM Write Timing				
t _{WC}	Write Cycle Time ^[1]	27		ns
t _{SCE}	CS[7:0] LOW to End of Write ^[1]		22	ns
t _{AW1}	Address Set-Up to End of Write (A ₄ -A ₁₇) ^[1]	20		ns
t _{AW2}	Address Set-Up to End of Write (A ₂₋₀ , A ₃₋₀ , A ₃₋₁ , No Latch Path) ^[1]	15		ns
t _{HA}	Address Hold from End of Write ^[2]	0		ns
t _{SA}	Address Set-Up to Start of Write ^[2]	0		ns
t _{PWE}	WE[1:0] Pulse Width ^[1]	15		ns
t _{SD}	Data Set-Up to End of Write ^[2]	12		ns
t _{HD}	Data Hold from End of Write ^[2]	0		ns
t _{LZWE}	WE[1:0] LOW to High Z ^[2]		12	ns
t _{HZWE}	WE[1:0] HIGH to Low Z ^[2]	3		ns
Tag SRAM Write Timing				
t _{TWC}	Tag Write Cycle Time ^[1]	17		ns
t _{TSCE}	TAGCS LOW to End of Tag Write ^[1]	10		ns
t _{TAW}	Address Set-Up to End of Tag Write ^[1]	10		ns
t _{THA}	Address Hold from End of Tag Write ^[2]	0		ns
t _{TSA}	Address Set-Up to Start of Tag Write ^[2]	0		ns
t _{TWPE}	TAGWE Pulse Width ^[1]	10		ns
t _{TSD}	Tag Set-Up to End of Tag Write ^[2]	11		ns
t _{THD}	Tag Hold from End of Tag Write ^[2]	0		ns
t _{TLZWE}	TAGWE LOW to Tag High Z ^[2]		9	ns
t _{THZWE}	TAGWE HIGH to Tag Low Z ^[2]	3		ns
Dirty SRAM Write Timing (CYM9246 & CYM9247)				
t _{DWC}	Dirty Write Cycle Time ^[1]	27		ns
t _{DDW}	DIRTYI Set-Up to End of Dirty Write ^[1]	12		ns
t _{DDHW}	DIRTYI Hold from End of Dirty Write ^[1]	0		ns
t _{DSCE}	DIRTYCS LOW to End of Dirty Write ^[2]	12		ns
t _{DAW}	Address Set-Up to End of Dirty Write ^[2]	16		ns
t _{DHA}	Address Hold from End of Dirty Write ^[2]	0		ns
t _{DSA}	Address Set-Up to Start of Dirty Write ^[2]	0		ns
t _{DWPE}	DIRTYWE Pulse Width ^[1]	12		ns
t _{DLZWE}	DIRTYWE LOW to DIRTYO pulled HIGH ^[2]		9	ns
t _{DHZWE}	DIRTYWE HIGH to DIRTYO Low Z ^[2]	5		ns

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Parameters guaranteed by design, not tested.

Switching Waveforms (continued)
Data Write Cycle No. 1 (\overline{WE} Controlled)[6, 7, 8]


9246-8

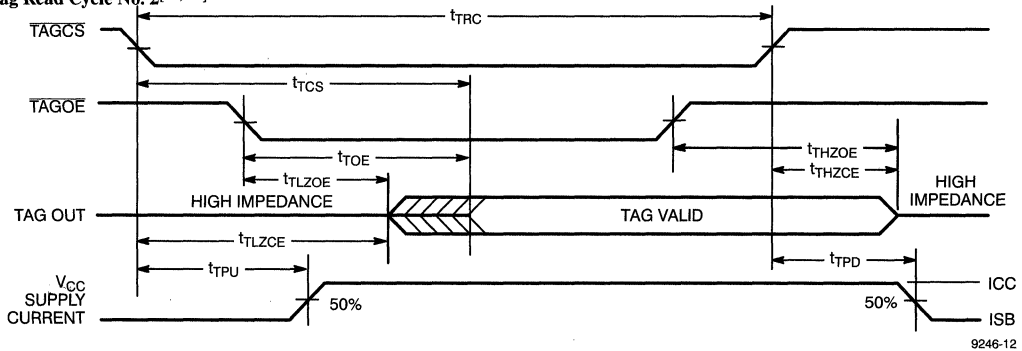
Data Write Cycle No. 2 ($\overline{CS}[0-3]$ Controlled)[16, 17, 8]


9246-9

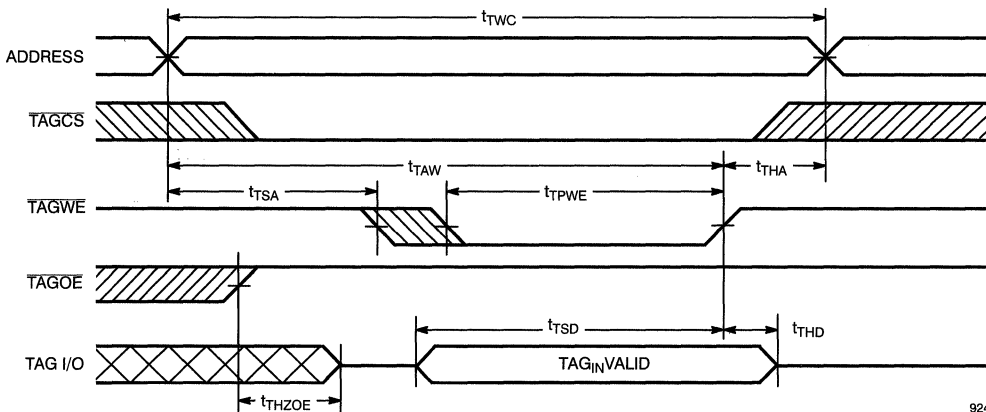
Notes:

 7. Data I/O is high impedance if $\overline{OE}_{0/1} = V_{IH}$.

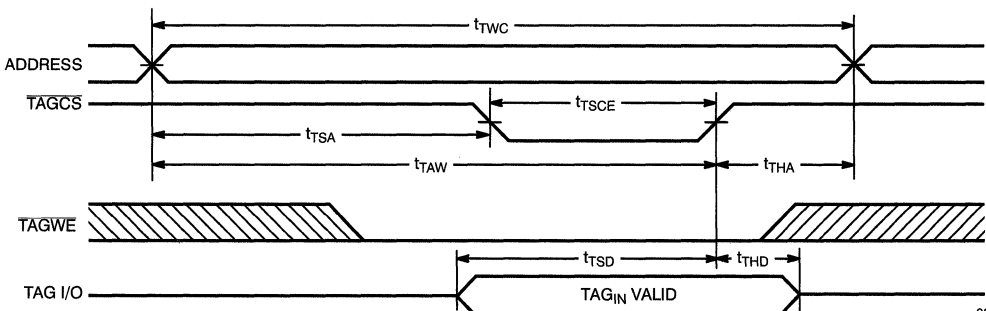
 8. If $\overline{CS}_0 - \overline{CS}_3$ goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)
Tag Read Cycle No. 2^[11, 12]


9246-12

Tag Write Cycle No. 1 (TAGWE Controlled)^[13, 14, 15]


9246-13

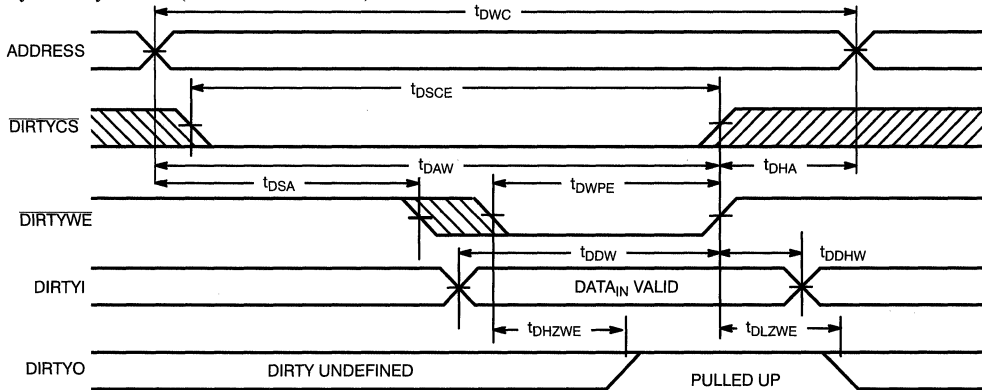
Tag Write Cycle No. 2 (TAGCS Controlled)^[13, 14, 15]


9246-14

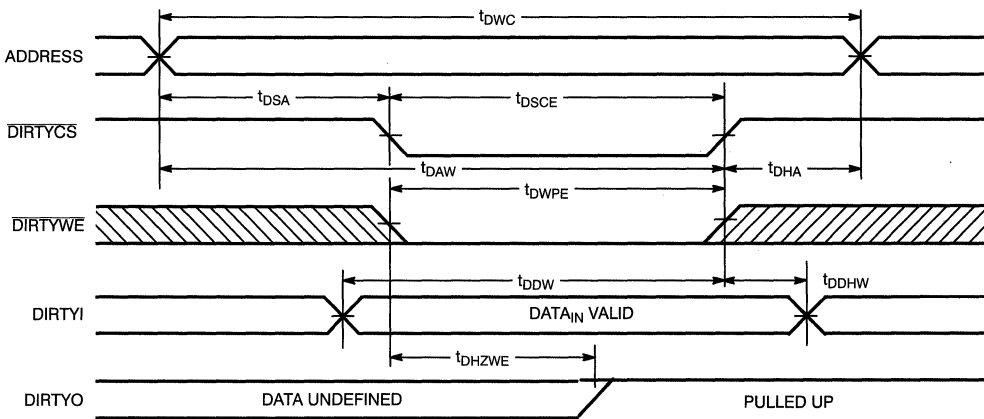
Notes:

12. Address valid prior to, or coincident with TAGCS transition LOW.
13. The internal write time of the memory is defined by the overlap of TAGCS LOW and TAGWE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The

- data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
14. TAG I/O is high impedance if TAGOE = LOW.

Switching Waveforms (continued)
Dirty Write Cycle No. 1 (DIRTYWE Controlled)^[19]


9246-18

Dirty Write Cycle No. 2 (DIRTYCS Controlled)^[19, 20]


9246-19

Notes:

19. The internal write time of the memory is defined by the overlap of DIRTYCS LOW and DIRTYWE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
20. If DIRTYCS goes HIGH simultaneously with DIRTYWE HIGH, the output remains in a high-impedance state.

Non-Volatile Memories
Page Number

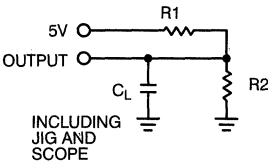
Introduction to CMOS Non-Volatile Memories	4-1
Device	Description
CY27C64	8K x 8 EPROM 4-3
CY27C010	128K x 8 CMOS EPROM 4-9
CY27C020	256K x 8 CMOS EPROM 4-16
CY27C040	512K x 8 CMOS EPROM 4-23
CY27C128	128K (16K x 8-Bit) CMOS EPROM 4-30
CY27C256	32K x 8-Bit CMOS EPROM 4-37
CY27C512	64K x 8 CMOS EPROM 4-45
CY27H010	128K x 8 High-Speed CMOS EPROM 4-52
CY27H256	32K x 8 High-Speed CMOS EPROM 4-60
CY27H512	64K x 8 High-Speed CMOS EPROM 4-68
CY7C225A	512 x 8 Registered PROM 4-76
CY7C235A	1K x 8 Registered PROM 4-83
CY7C243	4K x 8 Reprogrammable PROM 4-90
CY7C244	4K x 8 Reprogrammable PROM 4-90
CY7C245A	2K x 8 Reprogrammable Registered PROM 4-97
CY7C251	16K x 8 Power-Switched and Reprogrammable PROM 4-105
CY7C254	16K x 8 Power-Switched and Reprogrammable PROM 4-105
CY7C261	8K x 8 Power-Switched and Reprogrammable PROM 4-112
CY7C263	8K x 8 Power-Switched and Reprogrammable PROM 4-112
CY7C264	8K x 8 Power-Switched and Reprogrammable PROM 4-112
CY7C265	8K x 8 Registered PROM 4-121
CY7C266	8K x 8 Power-Switched and Reprogrammable PROM 4-129
CY7C269	8K x 8 Registered Diagnostic PROM 4-136
CY7C271	32K x 8 Power-Switched and Reprogrammable PROM 4-147
CY7C274	32K x 8 Power-Switched and Reprogrammable PROM 4-147
CY7C271A	32K x 8 Power-Switched and Reprogrammable PROM 4-148
CY7C276	16K x 16 Reprogrammable PROM 4-155
CY7C277	32K x 8 Reprogrammable Registered PROM 4-161
CY7C281A	1K x 8 PROM 4-168
CY7C282A	1K x 8 PROM 4-168
CY7C287	64K x 8 Reprogrammable Registered PROM 4-174
CY7C291A	2K x 8 Reprogrammable PROM 4-180
CY7C292A	2K x 8 Reprogrammable PROM 4-180
CY7C293A	2K x 8 Reprogrammable PROM 4-180
Non-Volatile Memory Programming Information	4-189

large variations of power supply voltage, creating erroneous function or transient performance failures.

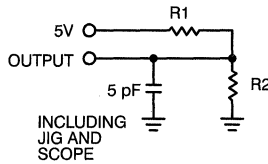
- All device test loads should be located within 2' of device outputs.
- Do not leave any inputs disconnected (floating) during any tests.
- Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
- V_{OH} and V_{OL} are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
- Capacitance is tested initially and after any design or process changes that may affect these parameters.
- The CMOS process does not provide a clamp diode. However, the Cypress PROM Products are insensitive to $-3V$ dc input levels and $-5V$ undershoot pulses of less than 10 ns (measured at 50%).

Switching Tests

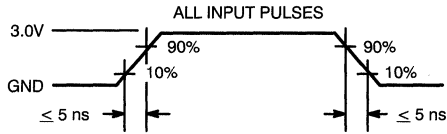
AC Test Loads and Waveforms



(a) Normal Load



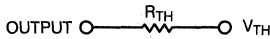
(b) High Z Load



INTRO-1

INTRO-2

Equivalent to: THÉVENIN EQUIVALENT



Load circuit (a) is used to test all switching characteristics except High Z parameters. Load circuit (b) is used to test High Z parameters. R_1 is a resistor connected from the output to V_{CC} and R_2 is connected between the device ground pin and the test system ground for testing purposes.

Values of R_1 and R_2 are given in the individual datasheet for each product. Speed is measured at 1.5V reference levels except for delay to output High Z.

Document #: 38-00234-A

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential (DIP Pin 28 to Pin 14)	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-3.0V to +7.0V
DC Program Voltage	13.0V

Static Discharge Voltage	> 2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	> 200 mA
UV Exposure	7258 Wsec/cm ²

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial ^[2]	-40°C to +85°C	5V ± 10%
Military ^[3]	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[4,5]

Parameter	Description	Test Conditions	Min.	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 16.0 mA		0.4	V	
V _{IH}	Input HIGH Voltage		2.0		V	
V _{IL}	Input LOW Voltage			0.8	V	
I _{IX}	Input Current	GND ≤ V _{IN} ≤ V _{CC}	-10	+10	μA	
V _{CD}	Input Diode Clamp Voltage		Note 5			
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled	-10	+10	μA	
I _{OS}	Output Short Circuit Current ^[6]	V _{CC} = Max., V _{OUT} = GND	-20	-90	mA	
I _{CC}	Power Supply Current	V _{CC} = Max., V _{IN} = 2.0V, I _{OUT} = 0 mA f = 10 MHz	Com'l		80	mA
			Mil		100	
I _{SB}	Standby Supply Current	Chip Enable Inactive, CE = V _{IH} , I _{OUT} = 0 mA	Com'l		15	mA
			Mil		15	

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

- Contact a Cypress representative regarding industrial temperature range specification.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- See the "Introduction to CMOS NVMs" section of the Cypress Data Book for general information on testing.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

Erasure Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the devices in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm². For an ultraviolet lamp with a 12 mW/cm² power rating, the exposure time would be approximately 35 minutes. The CY27C64 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the

EPROM is exposed to high-intensity UV light for an extended period of time.

7258 Wsec/cm² is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative. When programming, select the Cypress CY7C266 algorithm.

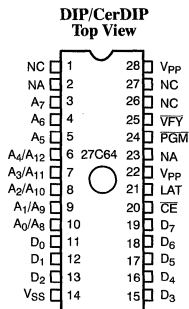
Table 1. Mode Selection

Mode	Pin Function ^[7, 8]								
	Normal Operation	A ₈	A ₉	A ₁₀	A ₁₁	A ₁₂	\overline{CE}	\overline{OE}	D ₇ - D ₀
Program	VFY	PGM	LAT	NA	NA	NA	\overline{CE}	V _{PP}	D ₇ - D ₀
Read		A ₈	A ₉	A ₁₀	A ₁₁	A ₁₂	V _{IL}	V _{IL}	O ₇ - O ₀
Standby		X	X	X	X	X	V _{IH}	X	Three-States
Output Disable		A ₈	A ₉	A ₁₀	A ₁₁	A ₁₂	V _{IL}	V _{IH}	Three-States
Program		V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{PP}	D ₇ - D ₀
Program Verify		V _{ILP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{PP}	O ₇ - O ₀
Program Inhibit		V _{IHP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{PP}	Three-States
Blank Check		V _{ILP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{PP}	O ₇ - O ₀

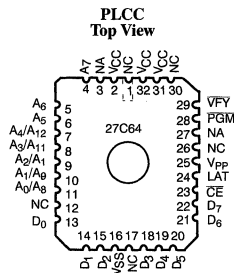
Notes:

7. X = "don't care" but must not exceed V_{CC} + 5%.

8. Address A₈ - A₁₂ must be latched through lines A₀ - A₄ in Programming modes.



27C64-56



27C64-67

Figure 1. Programming Pinout

Ordering Information^[9]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY27C64-70JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C64-70PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C64-70WC	W16	28-Lead (600-Mil) Windowed CerDIP	
90	CY27C64-90JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C64-90PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C64-90WC	W16	28-Lead (600-Mil) Windowed CerDIP	
120	CY27C64-120JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C64-120PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C64-120WC	W16	28-Lead (600-Mil) Windowed CerDIP	
150	CY27C64-150JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C64-150PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C64-150WC	W16	28-Lead (600-Mil) Windowed CerDIP	
200	CY27C64-200JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C64-200PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C64-200WC	W16	28-Lead (600-Mil) Windowed CerDIP	

Note:

9. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

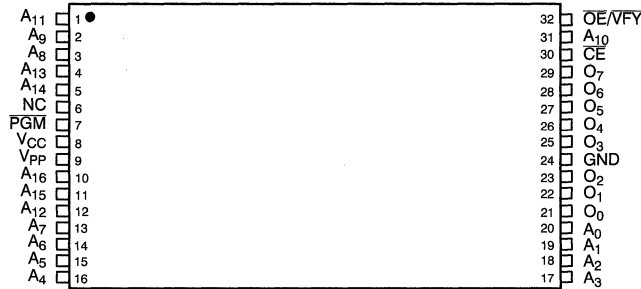
**MILITARY SPECIFICATIONS
Group A Subgroup Testing**
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{AA}	7, 8, 9, 10, 11
t _{OE}	7, 8, 9, 10, 11
t _{CE}	7, 8, 9, 10, 11

Document #: 38-00448

Pin Configurations (continued)
**TSOP
Top View**


C010-4

Selection Guide

		27C010-70	27C010-90	27C010-120	27C010-150	27C010-200
Maximum Access Time (ns)		70	90	120	150	200
CE Access Time (ns)		70	90	120	150	200
OE Access Time (ns)		25	30	40	50	60
I _{CC} ^[1] (mA) Power Supply Current	Com'l	40	40	40	40	40
	Mil	50	50	50	50	50
I _{SB} ^[2] (mA) Stand-by Current	Com'l	15	15	15	15	15
	Mil	25	25	25	25	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +5.5V
DC Input Voltage	-3.0V to +7.0V
Transient Input Voltage	-3.0V for <20 ns
DC Program Voltage	13.0V

UV Erasure	7258 Wsec/cm ²
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial ^[3]	-40°C to +85°C	5V ± 10%
Military ^[4]	-55°C to +125°C	5V ± 10%

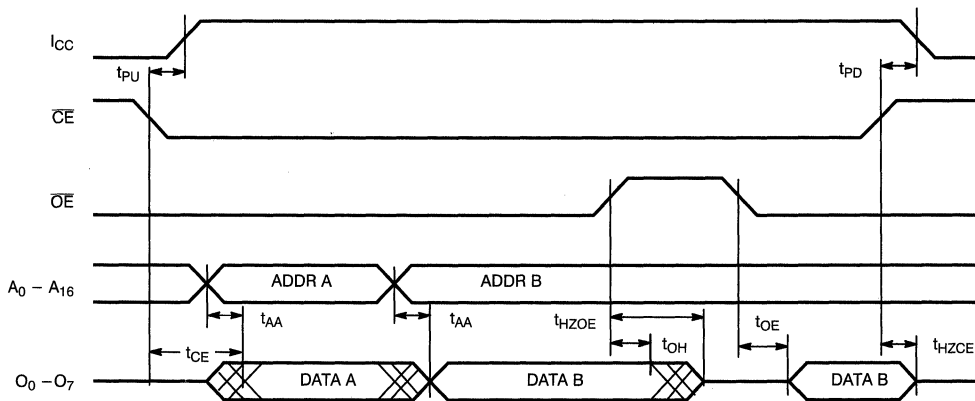
Notes:

- V_{CC} = Max., I_{OUT} = 0 mA, f = 5 MHz.
- V_{CC} = Max., CE = V_{IH}.

- Contact a Cypress representative for industrial temperature range specification.
- T_A is the "instant on" case temperature.

Switching Characteristics Over the Operating Range

Parameter	Description	27C010-70		27C010-90		27C010-120		27C010-150		27C010-200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		70		90		120		150		200	ns
t_{OE}	\overline{OE} Active to Output Valid		25		30		40		50		60	ns
t_{HZOE}	\overline{OE} Inactive to High Z		25		30		40		50		60	ns
t_{CE}	\overline{CE} Active to Output Valid		70		90		120		150		200	ns
t_{HZCE}	\overline{CE} Inactive to High Z		25		30		30		30		30	ns
t_{PU}	\overline{CE} Active to Power-Up	0		0		0		0		0		ns
t_{PD}	\overline{CE} Inactive to Power-Down		60		65		65		65		65	ns
t_{OH}	Output Data Hold	0		0		0		0		0		ns

Switching Waveform


C010-7

Ordering Information^[10]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY27C010-70JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C010-70PC	P15	32-Lead (600-Mil) Molded DIP	
	CY27C010-70WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C010-70ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C010-70DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C010-70LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C010-70QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
90	CY27C010-90JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C010-90PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C010-90WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C010-90ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C010-90DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C010-90LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C010-90QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
120	CY27C010-120JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C010-120PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C010-120WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C010-120ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C010-120DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C010-120LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C010-120QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
150	CY27C010-150JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C010-150PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C010-150WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C010-150ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C010-150DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C010-150LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C010-150QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
200	CY27C010-200JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C010-200PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C010-200WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C010-200ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C010-200DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C010-200LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C010-200QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C010-200WMB	W20	32-Lead (600-Mil) Windowed CerDIP	

Notes:

10. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.



256K x 8 CMOS EPROM

Features

- CMOS for optimum speed/power
- High speed
 - $t_{AA} = 70$ ns max.
- Low power
 - 140 mW max.
 - Less than 550 μ W when deselected
- Byte-wide memory organization
- 100% reprogrammable in the windowed package
- EPROM technology
- Capable of withstanding >2001V static discharge
- Available in
 - 32-pin PLCC
 - 32-pin TSOP-I
 - 32-pin, 600-mil plastic or hermetic DIP
 - 32-pin hermetic LCC

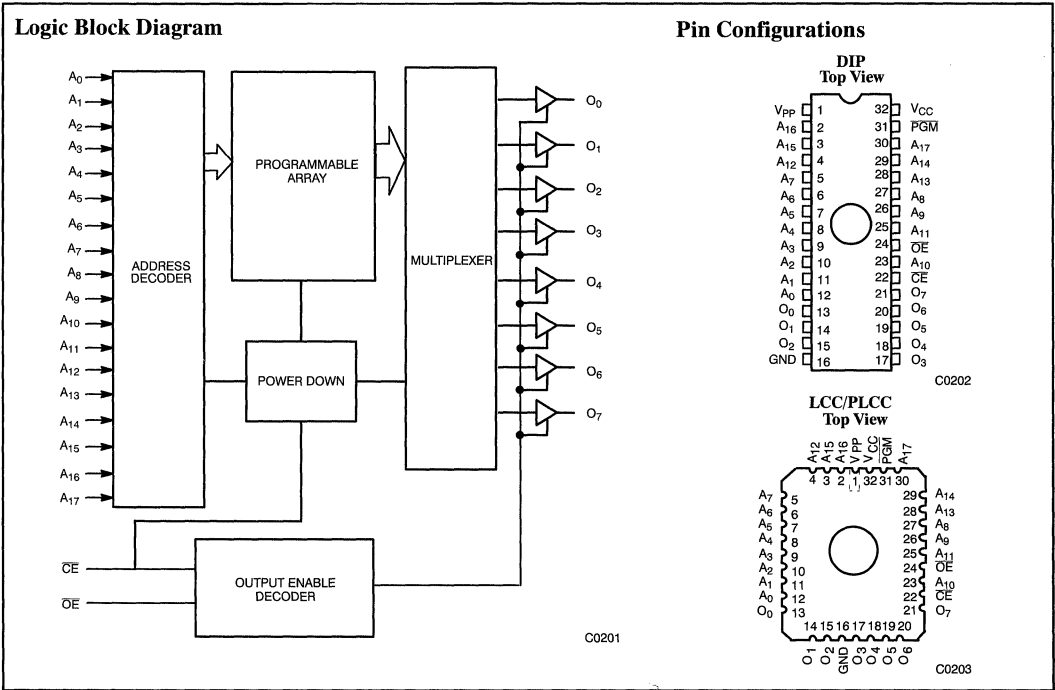
Functional Description

The CY27C020 is a high-performance, 2-megabit CMOS EPROM organized in 256 Kbytes. It is available in industry-standard 32-pin, 600-mil DIP, 32-pin LCC and PLCC, and 32-pin TSOP-I packages. The CY27C020 is available in windowed and opaque packages. Windowed packages allow the device to be erased with UV light for 100% reprogrammability.

The CY27C020 is equipped with a power-down chip enable (\overline{CE}) input and output enable (\overline{OE}). When \overline{CE} is deasserted, the device powers down to a low-power standby mode. The \overline{OE} pin three-states the outputs without putting the device into standby mode. While \overline{CE} offers lower power, \overline{OE} provides a more rapid transition to and from three-stated outputs.

The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms. The EPROM cell requires only 12.75 V for the supervoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

The CY27C020 is read by asserting both the \overline{CE} and the \overline{OE} inputs. The contents of the memory location selected by the address on inputs $A_{17}-A_0$ will appear at the outputs O_7-O_0 .



Electrical Characteristics Over the Operating Range^[6,7]

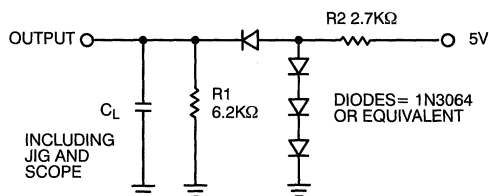
Parameter	Description	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -400 μA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.1 mA		0.45	V
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs	2.0	V _{CC} +0.5	V
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disable	-10	+10	μA
I _{CC}	Power Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=5 MHz	Com'l	25	mA
			Mil	30	mA
I _{SB}	Stand-By Current	V _{CC} =Max., CE = V _{IH}	Com'l	1	mA
			Mil	1	mA

Capacitance^[6]

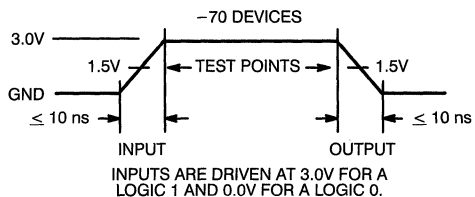
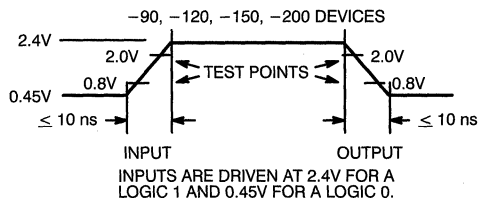
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

6. See the last page of this specification for Group A subgroup testing information.
7. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms


C_L = 100 pF FOR -90, -120, -150, -200 DEVICES
 C_L = 30 pF FOR -70 DEVICES



C0205

C0206

Erase Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the CY27C020 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm². For an ultraviolet lamp with a 12 mW/cm² power rating, the exposure time would be approximately 35 minutes. The CY27C020 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the

EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm² is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V _{PP}	Programming Power Supply	12.5	13	V
I _{PP}	Programming Supply Current		50	mA
V _{IHP}	Programming Input Voltage HIGH	3.0	V _{CC}	V
V _{ILP}	Programming Input Voltage LOW	-0.5	0.4	V
V _{CCP}	Programming V _{CC}	6.0	6.5	V

Table 2. Mode Selection

Mode	Pin Function ^[8]						
	CE	OE	PGM	V _{PP}	A ₀	A ₉	Data
Read	V _{IL}	V _{IL}	X	V _{IH}	A ₀	A ₉	O ₇ - O ₀
Output Disable	V _{IL}	V _{IH}	X	V _{IH}	A ₀	A ₉	High Z
Stand-by (CMOS)	V _{CC} - 0.3V	X	X	V _{IH}	X	X	High Z
Stand-by (TTL)	V _{IH}	X	X	V _{IH}	X	X	High Z
Program	V _{ILP}	V _{IHP}	V _{ILP}	V _{PP}	A ₀	A ₉	D ₇ - D ₀
Program Verify	V _{ILP}	V _{ILP}	V _{IHP}	V _{PP}	A ₀	A ₉	O ₇ - O ₀
Program Inhibit	V _{ILP}	V _{IHP}	V _{IHP}	V _{PP}	A ₀	A ₉	High Z
Signature Read (MFG)	V _{IL}	V _{IL}	X	V _{IH}	V _{IL}	V _{HV} ^[9]	34H
Signature Read (DEV)	V _{IL}	V _{IL}	X	V _{IH}	V _{IH}	V _{HV} ^[8]	Note 10

Note:

8. X can be V_{IL} or V_{IH}.

9. V_{HV}=12V±0.5V

10. To be determined.

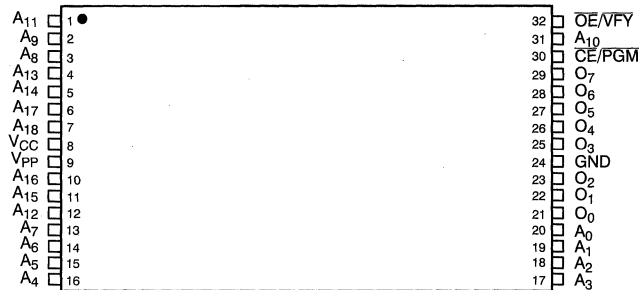
MILITARY SPECIFICATIONS**Group A Subgroup Testing****DC Characteristics**

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{CE}	7, 8, 9, 10, 11

Document #: 38-00449

Pin Configurations (continued)
**TSOP
Top View**


C040-4

Selection Guide

	27C040-70	27C040-90	27C040-120	27C040-150	27C040-200
Maximum Access Time (ns)	70	90	120	150	200
CE Access Time (ns)	70	90	120	150	200
OE Access Time (ns)	30	35	40	50	60
I _{CC} ^[1] (mA) Power Supply Current	Com'l	25	25	25	25
	Mil		30	30	30
I _{SB} ^[2] (μA) CMOS Stand-by Current	100	100	100	100	100
I _{SB} ^[3] (mA) TTL Stand-by Current	1	1	1	1	1

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature -65°C to +150°C
- Ambient Temperature with Power Applied -55°C to +125°C
- Supply Voltage to Ground Potential -0.5V to +7.0V
- DC Voltage Applied to Outputs in High Z State -0.5V to +5.5V
- DC Input Voltage -3.0V to +7.0V
- Transient Input Voltage -3.0V for <20 ns
- DC Program Voltage 13.0V

Notes:

1. V_{CC} = Max., I_{OUT} = 0 mA, f=5 MHz.
2. V_{CC} = Max., CE = V_{CC} - 0.3V to V_{CC} + 1.0V.
3. V_{CC} = Max., CE = V_{IH}.

- UV Erasure 7258 Wsec/cm²
- Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current >200 mA

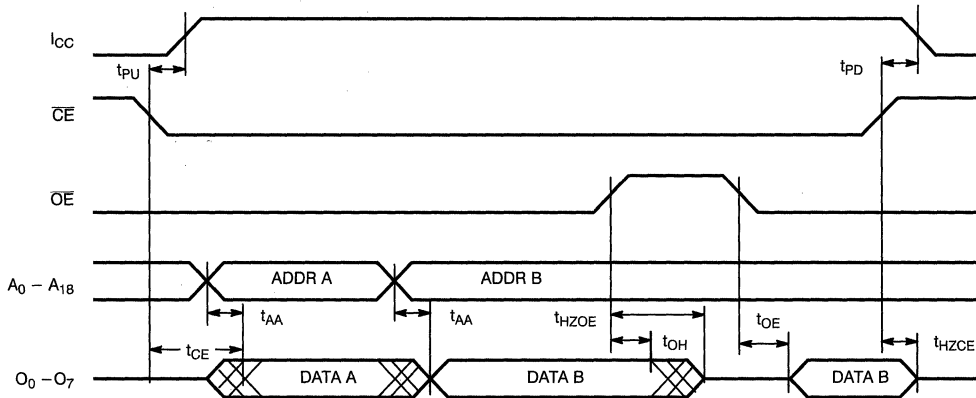
Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial ^[4]	-40°C to +85°C	5V ± 10%
Military ^[5]	-55°C to +125°C	5V ± 10%

4. Contact a Cypress representative for industrial temperature range specification.
5. T_A is the "instant on" case temperature.

Switching Characteristics Over the Operating Range

Parameter	Description	27C040-70		27C040-90		27C040-120		27C040-150		27C040-200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		70		90		120		150		200	ns
t_{OE}	\overline{OE} Active to Output Valid		30		35		40		50		60	ns
t_{HZOE}	\overline{OE} Inactive to High Z		25		25		30		30		40	ns
t_{CE}	\overline{CE} Active to Output Valid		70		90		120		150		200	ns
t_{HZCE}	\overline{CE} Inactive to High Z		25		25		30		30		40	ns
t_{PU}	\overline{CE} Active to Power-Up	0		0		0		0		0		ns
t_{PD}	\overline{CE} Inactive to Power-Down		60		65		65		65		70	ns
t_{OH}	Output Data Hold	0		0		0		0		0		ns

Switching Waveform


C040-7

Ordering Information^[11]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY27C040-70JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C040-70PC	P15	32-Lead (600-Mil) Molded DIP	
	CY27C040-70WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C040-70ZC	Z32	32-Lead Thin Small Outline Package	
90	CY27C040-90JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C040-90PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C040-90WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C040-90ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C040-90DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C040-90LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C040-90QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C040-90WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
120	CY27C040-120JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C040-120PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C040-120WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C040-120ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C040-120DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C040-120LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C040-120QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C040-120WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
150	CY27C040-150JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C040-150PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C040-150WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C040-150ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C040-150DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C040-150LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C040-150QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C040-150WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
200	CY27C040-200JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C040-200PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C040-200WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C040-200ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C040-200DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C040-200LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C040-200QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C040-200WMB	W20	32-Lead (600-Mil) Windowed CerDIP	

Notes:

11. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.



128K (16K x 8-Bit) CMOS EPROM

Features

- **Wide speed range**
 - 45 ns to 200 ns (commercial and military)
- **Low power**
 - 248 mW (commercial)
 - 303 mW (military)
- **Low standby power**
 - Less than 83 mW when deselected
- **±10% Power supply tolerance**

Functional Description

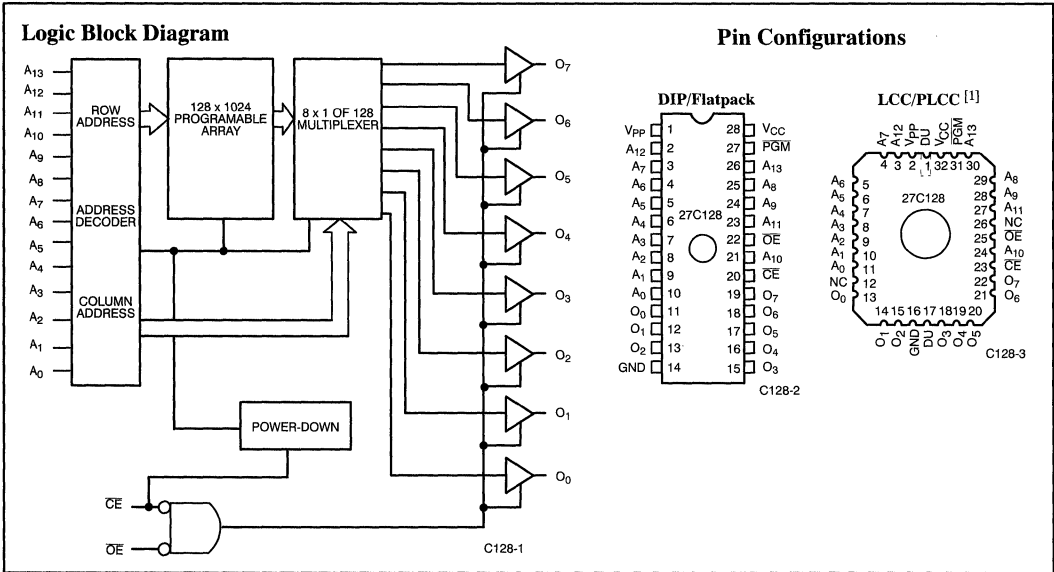
The CY27C128 is a high-performance 16,384-word by 8-bit CMOS EPROM. When disabled (CE HIGH), the

CY27C128 automatically powers down into a low-power stand-by mode. The CY27C128 is packaged in the industry standard 600-mil DIP and LCC packages. The CY27C128 is also available in a Cer-DIP package equipped with an erasure window to provide for reprogrammability. When exposed to UV light, the EPROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY27C128 offers the advantage of lower power and superior performance and programming yield. The EPROM cell requires only 12.5V for the super voltage,

and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each EPROM is also tested for AC performance to guarantee that after customer programming, the product will meet both DC and AC specification limits.

Reading the CY27C128 is accomplished by placing active LOW signals on OE and CE. The contents of the memory location addressed by the address lines (A₀ – A₁₃) will become available on the output lines (O₀ – O₇).

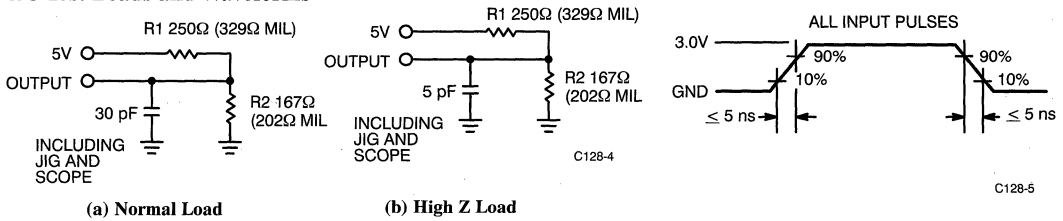


Selection Guide

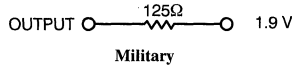
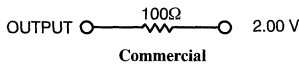
	27C128-45	27C128-55	27C128-70	27C128-90	27C128-120	27C128-150	27C128-200
Maximum Access Time (ns)	45	55	70	90	120	150	200
Maximum Operating Current (mA) ^[2]	Com ¹	45	45	45	45	45	45
	Mil	55	55	55	55	55	55
Standby Current (mA)	Com ¹	15	15	15	15	15	15
	Mil	20	20	20	20	20	20
Chip Select Time (ns)	45	55	70	90	120	150	200
Output Enable Time (ns)	15	20	25	30	30	40	40

Notes:

1. For PLCC only: Pins 1 and 17 are common and tied to the die attach pad. They must therefore be DU (don't use) for the PLCC package.
2. Add 2 mA/MHz for AC power component.

AC Test Loads and Waveforms


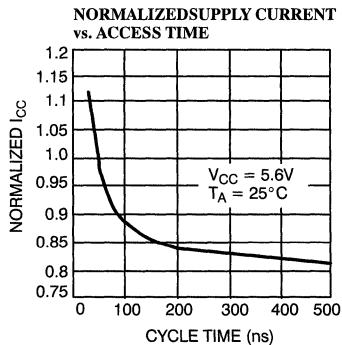
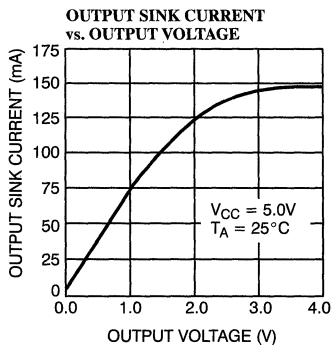
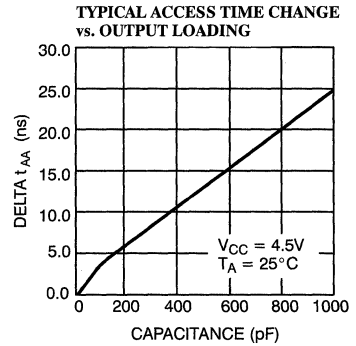
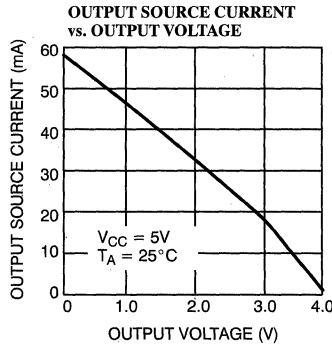
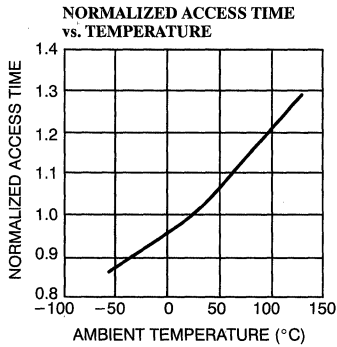
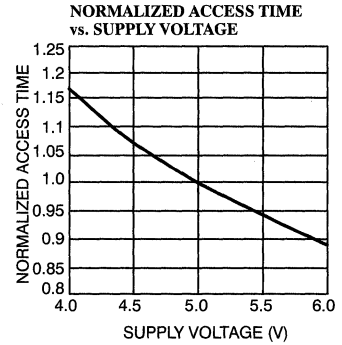
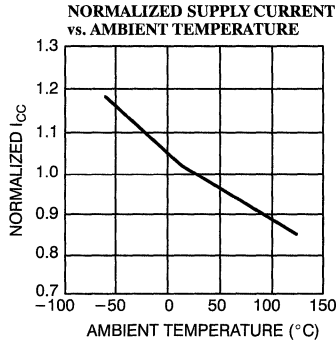
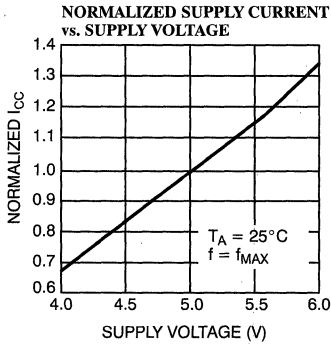
Equivalent to: THÉVENIN EQUIVALENT


Switching Characteristics Over the Operating Range^[4, 7]

Parameter	Description	27C128-45		27C128-55		27C128-70		27C128-90		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		45		55		70		90	ns
t_{HZOE}	Output Enable Inactive to High Z		15		20		25		25	ns
t_{OE}	Output Enable Active to Output Valid		15		20		25		30	ns
t_{HZCE}	Chip Enable Inactive to High Z		20		25		25		25	ns
t_{ACE}	Chip Enable Active to Output Valid		45		55		70		90	ns
t_{PU}	Chip Enable Active to Power Up	0		0		0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		45		55		70		90	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

Switching Characteristics Over the Operating Range^[4, 7] (continued)

Parameter	Description	27C128-120		27C128-150		27C128-200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		120		150		200	ns
t_{HZOE}	Output Enable Inactive to High Z		30		30		30	ns
t_{OE}	Output Enable Active to Output Valid		30		40		40	ns
t_{HZCE}	Chip Enable Inactive to High Z		30		30		30	ns
t_{ACE}	Chip Enable Active to Output Valid		120		150		200	ns
t_{PU}	Chip Enable Active to Power Up	0		0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		120		150		200	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns

Typical DC and AC Characteristics


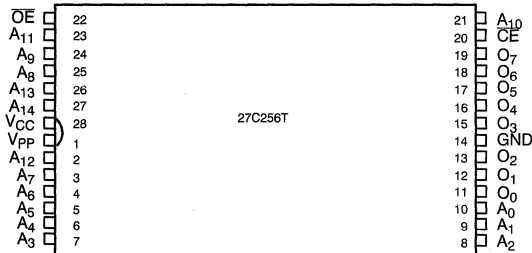
MILITARY SPECIFICATIONS
Group A Subgroup Testing**DC Characteristics**

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{Ix}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB}	1, 2, 3

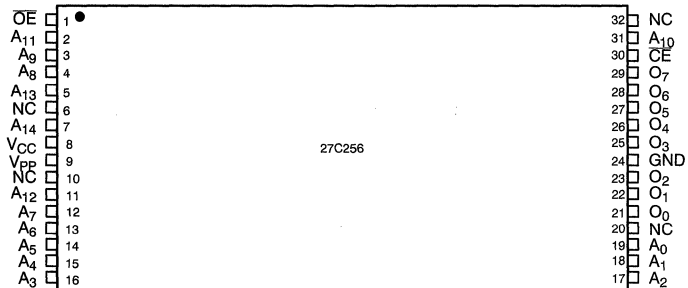
Switching Characteristics

Parameter	Subgroups
t _{AA}	7, 8, 9, 10, 11
t _{OE}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11

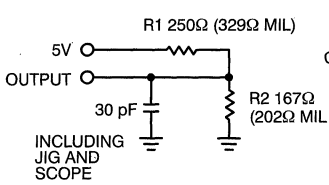
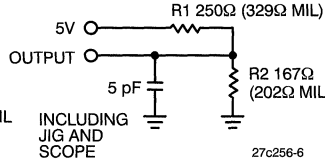
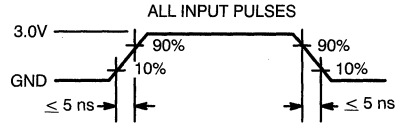
Document #: 38-00357

Pin Configurations
**28-Pin TSOP
Top View**


27c256-4

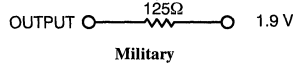
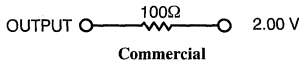
**32-Pin TSOP
Top View**


27c256-5

AC Test Loads and Waveforms

(a) Normal Load

(b) High Z Load


27c256-7

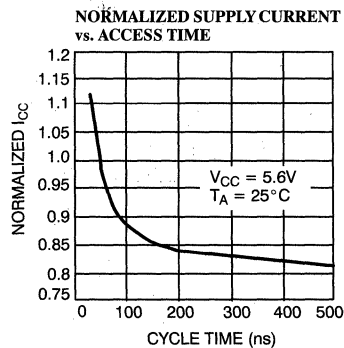
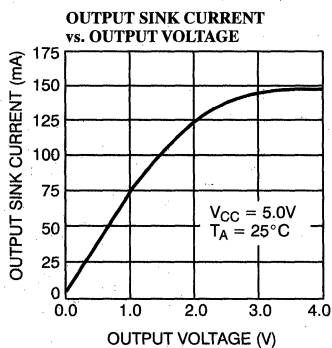
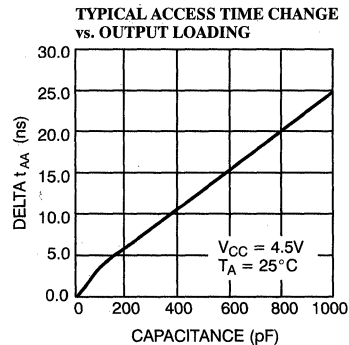
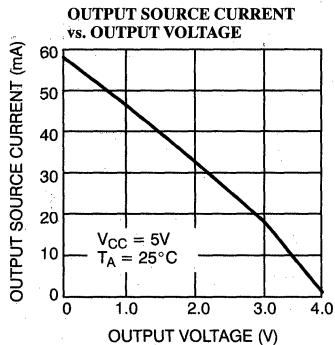
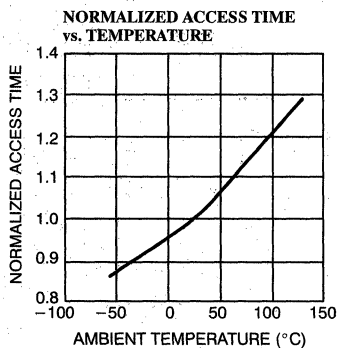
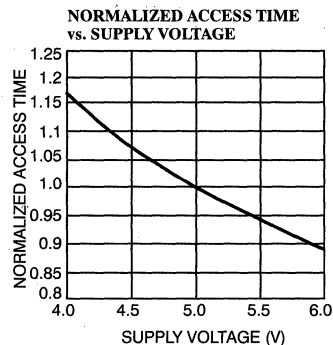
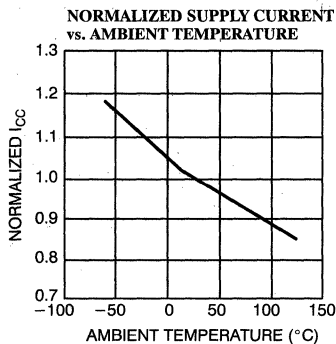
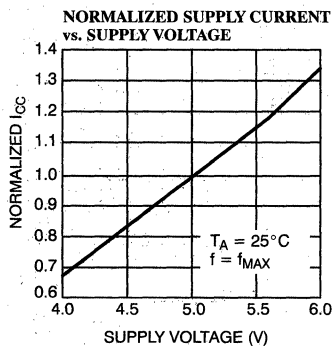
Equivalent to: THÉVENIN EQUIVALENT


Switching Characteristics Over the Operating Range^[4,7]

Parameter	Description	27C256-45		27C256-55		27C256-70		27C256-90		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		45		55		70		90	ns
t_{HZOE}	Output Enable Inactive to High Z		15		20		25		25	ns
t_{OE}	Output Enable Active to Output Valid		15		20		25		30	ns
t_{HZCE}	Chip Enable Inactive to High Z		20		25		25		25	ns
t_{ACE}	Chip Enable Active to Output Valid		45		55		70		90	ns
t_{PU}	Chip Enable Active to Power Up	0		0		0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		45		55		70		90	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

Switching Characteristics Over the Operating Range^[4,7]

Parameter	Description	27C256-120		27C256-150		27C256-200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		120		150		200	ns
t_{HZOE}	Output Enable Inactive to High Z		30		30		30	ns
t_{OE}	Output Enable Active to Output Valid		30		40		40	ns
t_{HZCE}	Chip Enable Inactive to High Z		30		30		30	ns
t_{ACE}	Chip Enable Active to Output Valid		120		150		200	ns
t_{PU}	Chip Enable Active to Power Up	0		0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		120		150		200	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns

Typical DC and AC Characteristics


Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY27C256T-45WC	W22	28-Lead (300-Mil) Windowed CerDIP	Commercial
	CY27C256T-45ZC	Z28	28-Thin Small Outline Package	
	CY27C256T-45WMB	W22	28-Lead (300-Mil) Windowed CerDIP	Military
55	CY27C256T-55WC	W22	28-Lead (300-Mil) Windowed CerDIP	Commercial
	CY27C256T-55ZC	Z28	28-Thin Small Outline Package	
	CY27C256T-55WMB	W22	28-Lead (300-Mil) Windowed CerDIP	Military
70	CY27C256T-70WC	W22	28-Lead (300-Mil) Windowed CerDIP	Commercial
	CY27C256T-70ZC	Z28	28-Thin Small Outline Package	
	CY27C256T-70WMB	W22	28-Lead (300-Mil) Windowed CerDIP	Military

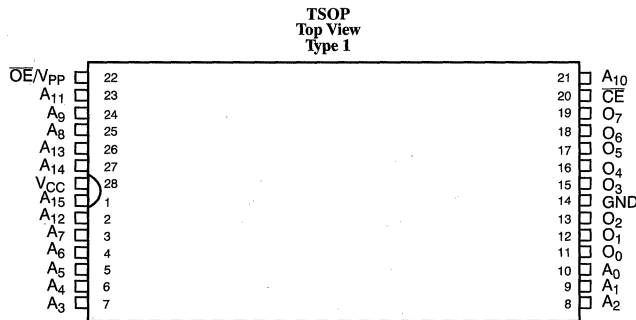
MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{AA}	7, 8, 9, 10, 11
t _{OE}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11

Document #: 38-00245-D

Pin Configurations (continued)


C512-4

Selection Guide

		27C512-70	27C512-90	27C512-120	27C512-150	27C512-200
Maximum Access Time (ns)		70	90	120	150	200
CE Access Time (ns)		70	90	120	150	200
OE Access Time (ns)		25	30	40	50	60
I _{CC} ^[2] (mA) Power Supply Current	Com'l	40	40	40	40	40
	Mil	50	50	50	50	50
I _{SB} ^[3] (mA) Stand-by Current	Com'l	15	15	15	15	15
	Mil	25	25	25	25	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +5.5V
DC Input Voltage	-3.0V to +7.0V
Transient Input Voltage	-3.0V for <20 ns
DC Program Voltage	13.0V

Notes:

- V_{CC} = Max., I_{OUT} = 0 mA, f = 5 MHz.
- V_{CC} = Max., CE = V_{IH}.

UV Erasure	7258 Wsec/cm ²
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V
Latch-Up Current	>200 mA

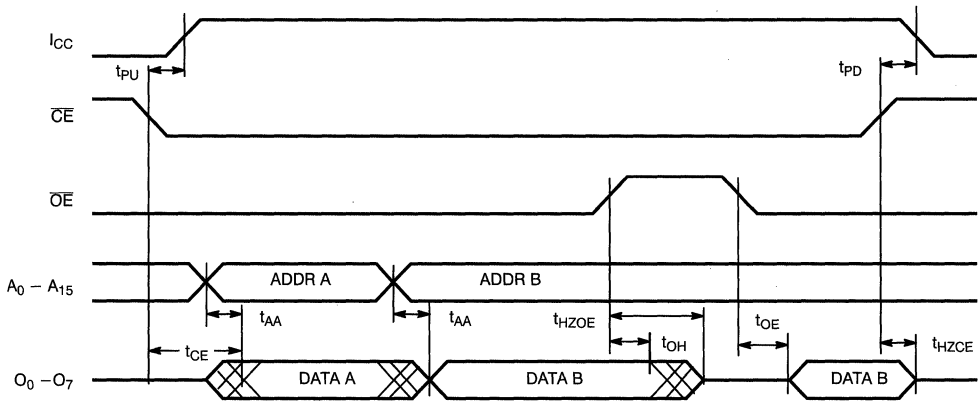
Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial ^[4]	-40°C to +85°C	5V ± 10%
Military ^[5]	-55°C to +125°C	5V ± 10%

- Contact a Cypress representative for industrial temperature range specification.
- T_A is the "instant on" case temperature.

Switching Characteristics Over the Operating Range

Parameter	Description	27C512-70		27C512-90		27C512-120		27C512-150		27C512-200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		70		90		120		150		200	ns
t_{OE}	\overline{OE} Active to Output Valid		25		30		40		50		60	ns
t_{HZOE}	\overline{OE} Inactive to High Z		25		30		40		50		60	ns
t_{CE}	\overline{CE} Active to Output Valid		70		90		120		150		200	ns
t_{HZCE}	\overline{CE} Inactive to High Z		25		30		30		30		30	ns
t_{PU}	\overline{CE} Active to Power-Up	0		0		0		0		0		ns
t_{PD}	\overline{CE} Inactive to Power-Down		60		65		65		65		65	ns
t_{OH}	Output Data Hold	0		0		0		0		0		ns

Switching Waveform


C512-7

Ordering Information^[1]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY27C512-70JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C512-70PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C512-70WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C512-70ZC	Z28	28-Lead Thin Small Outline Package	
	CY27C512-70DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27C512-70LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C512-70QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C512-70WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
90	CY27C512-90JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C512-90PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C512-90WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C512-90ZC	Z28	28-Lead Thin Small Outline Package	
	CY27C512-90DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27C512-90LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C512-90QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C512-90WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
120	CY27C512-120JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C512-120PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C512-120WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C512-120ZC	Z28	28-Lead Thin Small Outline Package	
	CY27C512-120DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27C512-120LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C512-120QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C512-120WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
150	CY27C512-150JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C512-150PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C512-150WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C512-150ZC	Z28	28-Lead Thin Small Outline Package	
	CY27C512-150DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27C512-150LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C512-150QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C512-150WMB	W16	28-Lead (600-Mil) Windowed CerDIP	



128K x 8 High-Speed CMOS EPROM

Features

- CMOS for optimum speed/power
- High speed
 - $t_{AA} = 25$ ns max. (commercial)
 - $t_{AA} = 35$ ns max. (military)
- Low power
 - 275 mW max.
 - Less than 85 mW when deselected
- Byte-wide memory organization
- 100% reprogrammable in the windowed package
- EPROM technology
- Capable of withstanding >2001V static discharge
- Available in
 - 32-pin PLCC
 - 32-pin TSOP-I
 - 32-pin, 600-mil plastic or hermetic DIP
 - 32-pin hermetic LCC

Functional Description

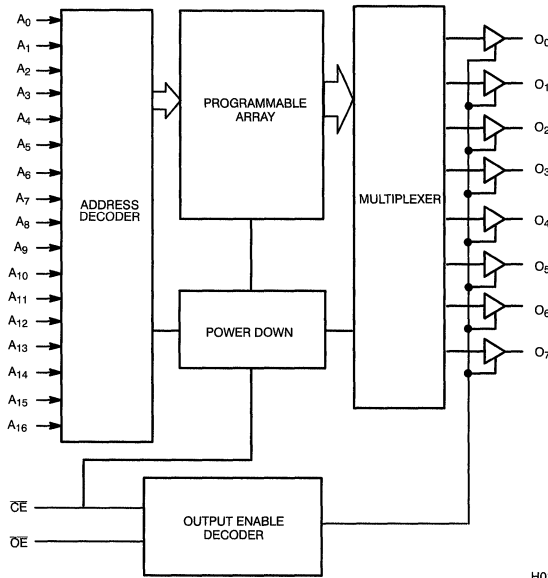
The CY27H010 is a high-performance, 1-megabit CMOS EPROM organized in 128 Kbytes. It is available in industry-standard 32-pin, 600-mil DIP, LCC, PLCC, and TSOP-I packages. These devices offer high-density storage combined with 40-MHz performance. The CY27H010 is available in windowed and opaque packages. Windowed packages allow the device to be erased with UV light for 100% reprogrammability.

The CY27H010 is equipped with a power-down chip enable (\overline{CE}) input and output enable (\overline{OE}). When \overline{CE} is deasserted, the device powers down to a low-power standby mode. The \overline{OE} pin three-states the outputs without putting the device into standby mode. While \overline{CE} offers lower power, \overline{OE} provides a more rapid transition to and from three-stated outputs.

The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms. The EPROM cell requires only 12.75 V for the supervoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

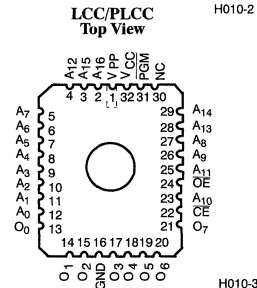
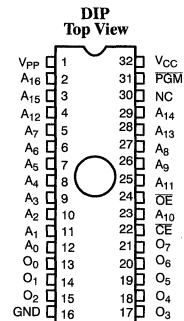
The CY27H010 is read by asserting both the \overline{CE} and the \overline{OE} inputs. The contents of the memory location selected by the address on inputs $A_{16}-A_0$ will appear at the outputs O_7-O_0 .

Logic Block Diagram



H010-1

Pin Configurations



H010-2

H010-3

Electrical Characteristics Over the Operating Range^[5, 6]

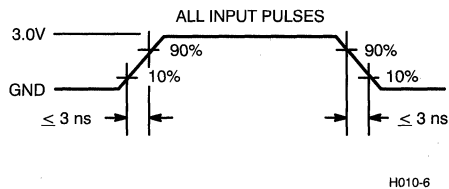
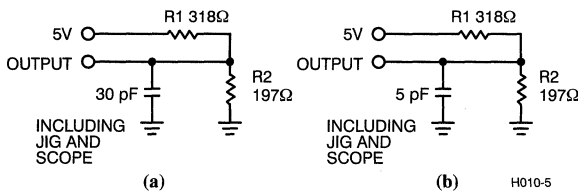
Parameter	Description	Test Conditions	27H010-25 27H010-30		27H010-35		27H010-45 27H010-55 27H010-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 12.0 mA		0.45		0.45		0.45	V
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs	2.0	V _{CC} +0.5	2.0	V _{CC} +0.5	2.0	V _{CC} +0.5	V
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		0.8		0.8		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}	-10	+10	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disable	-10	+10	-10	+10	-10	+10	μA
I _{CC}	Power Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=10 MHz	Com'l	75		50		50	mA
			Mil			85		60	mA
I _{SB}	Stand-By Current	V _{CC} =Max., CE = V _{IH}	Com'l	15		15		15	mA
			Mil			25		25	mA

Capacitance^[6]

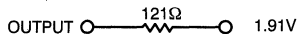
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		12	pF

Notes:

5. See the last page of this specification for Group A subgroup testing information. 6. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT



Erase Characteristics

Wavelengths of light less than 4000 Å begin to erase the CY27H010 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm². For an ultraviolet lamp with a 12 mW/cm² power rating, the exposure time would be approximately 35 minutes. The CY27H010 needs to be within 1 inch of the lamp

during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm² is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V _{PP}	Programming Power Supply	12.5	13	V
I _{PP}	Programming Supply Current		50	mA
V _{IHP}	Programming Input Voltage HIGH	3.0	V _{CC}	V
V _{ILP}	Programming Input Voltage LOW	-0.5	0.4	V
V _{CCP}	Programming V _{CC}	6.0	6.5	V

Table 2. Mode Selection

Mode	Pin Function ^[7]						
	\overline{CE}	\overline{OE}	\overline{PGM}	V _{PP}	A ₀	A ₉	Data
Read	V _{IL}	V _{IL}	X	V _{IH}	A ₀	A ₉	O ₇ - O ₀
Output Disable	V _{IL}	V _{IH}	X	V _{IH}	A ₀	A ₉	High Z
Stand-by	V _{IH}	X	X	V _{IH}	X	X	High Z
Program	V _{ILP}	V _{IHP}	V _{ILP}	V _{PP}	A ₀	A ₉	D ₇ - D ₀
Program Verify	V _{ILP}	V _{ILP}	V _{IHP}	V _{PP}	A ₀	A ₉	O ₇ - O ₀
Program Inhibit	V _{ILP}	V _{IHP}	V _{IHP}	V _{PP}	A ₀	A ₉	High Z
Signature Read (MFG)	V _{IL}	V _{IL}	X	V _{IH}	V _{IL}	V _{HV} ^[8]	34H
Signature Read (DEV)	V _{IL}	V _{IL}	X	V _{IH}	V _{IH}	V _{HV} ^[8]	1DH

Note:

7. X can be V_{IL} or V_{IH}.

8. V_{HV}=12V±0.5V

Ordering Information^[9]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY27H010-25HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H010-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H010-25ZC	Z32	32-Lead Thin Small Outline Package	
30	CY27H010-30HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H010-30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H010-30PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27H010-30WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27H010-30ZC	Z32	32-Lead Thin Small Outline Package	
35	CY27H010-35HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H010-35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H010-35PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27H010-35WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27H010-35ZC	Z32	32-Lead Thin Small Outline Package	Military
	CY27H010-35HMB	H65	32-Pin Windowed Leaded Chip Carrier	
	CY27H010-35LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H010-35QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
45	CY27H010-45HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H010-45JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H010-45PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27H010-45WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27H010-45ZC	Z32	32-Lead Thin Small Outline Package	Military
	CY27H010-45DMB	D20	32-Lead (600-Mil) CerDIP	
	CY27H010-45HMB	H65	32-Pin Windowed Leaded Chip Carrier	
	CY27H010-45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H010-45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H010-45WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
55	CY27H010-55HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H010-55JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H010-55PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27H010-55WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27H010-55ZC	Z32	32-Lead Thin Small Outline Package	
	CY27H010-55DMB	D20	32-Lead (600-Mil) CerDIP	
	CY27H010-55HMB	H65	32-Pin Windowed Leaded Chip Carrier	
	CY27H010-55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H010-55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H010-55WMB	W20	32-Lead (600-Mil) Windowed CerDIP	

Notes:

9. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

32K x 8 High-Speed CMOS EPROM

Features

- CMOS for optimum speed/power
- High speed
 - $t_{AA} = 25$ ns max. (commercial)
 - $t_{AA} = 35$ ns max. (military)
- Low power
 - 275 mW max.
 - Less than 85 mW when deselected
- Byte-wide memory organization
- 100% reprogrammable in the windowed package
- EPROM technology
- Capable of withstanding >2001 V static discharge
- Available in
 - 32-pin PLCC
 - 28-pin TSOP-I
 - 28-pin, 600-mil plastic or hermetic DIP
 - 32-pin hermetic LCC

Functional Description

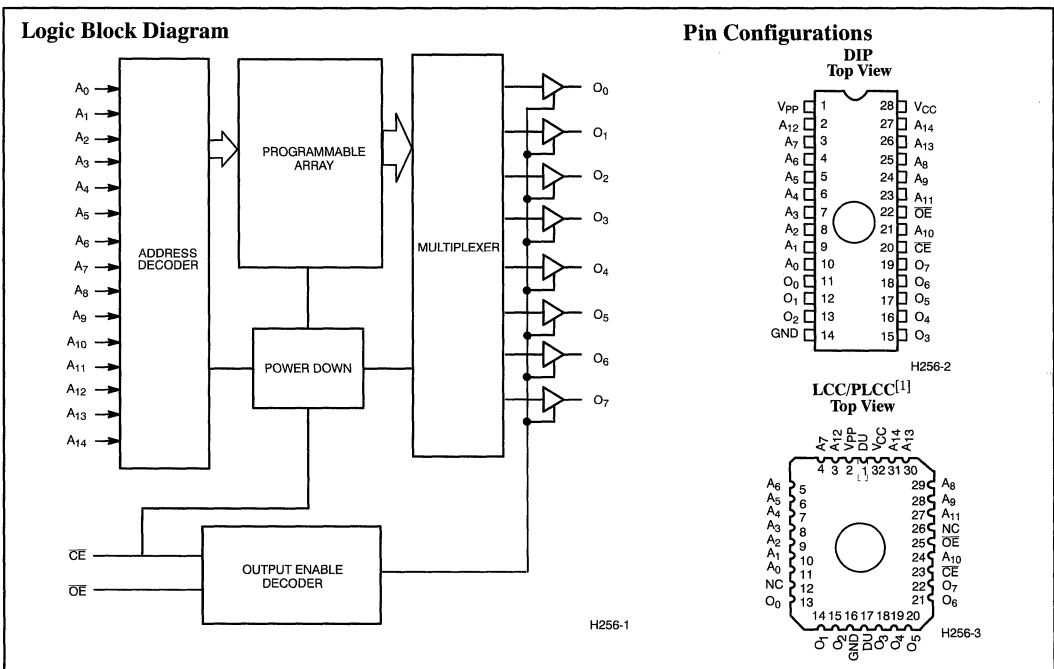
The CY27H256 is a high-performance, 256K CMOS EPROM organized in 32 Kbytes. It is available in industry-standard 28-pin, 600-mil DIP, 32-pin LCC and PLCC, and 28-pin TSOP-I packages. These devices offer high-density storage combined with 40-MHz performance. The CY27H256 is available in windowed and opaque packages. Windowed packages allow the device to be erased with UV light for 100% reprogrammability.

The CY27H256 is equipped with a power-down chip enable (\overline{CE}) input as well as an output enable (\overline{OE}) input. When \overline{CE} is deasserted, the device powers down to a low-power stand-by mode. The \overline{OE} pin three-states the outputs without putting the device into stand-by mode. While \overline{CE} offers lower power, \overline{OE} provides a more

rapid transition to and from three-stated outputs.

The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms. The EPROM cell requires only 12.75 V for the supervoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

The CY27H256 is read by asserting both the \overline{CE} and the \overline{OE} inputs. The contents of the memory location selected by the address on inputs $A_{14}-A_0$ will appear at the outputs O_7-O_0 .



Note:

1. For LCC/PLCC only: Pins 1 and 17 are common and tied to the die attach pad. They should not be used.

Electrical Characteristics Over the Operating Range^[6, 7]

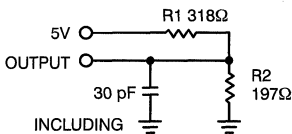
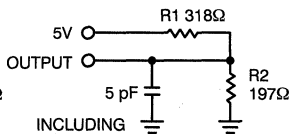
Parameter	Description	Test Conditions	27H256-25 27H256-30		27H256-35		27H256-45 27H256-55 27H256-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 12.0 mA		0.45		0.45		0.45	V
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs	2.0	V _{CC} +0.5	2.0	V _{CC} +0.5	2.0	V _{CC} +0.5	V
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		0.8		0.8		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}	-10	+10	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disable	-10	+10	-10	+10	-10	+10	μA
I _{CC}	Power Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=10 MHz	Com ¹	75		50		50	mA
			Mil			85		60	mA
I _{SB}	Stand-By Current	V _{CC} =Max., CE = V _{IH}	Com ¹	15		15		15	mA
			Mil			25		25	mA

Capacitance^[7]

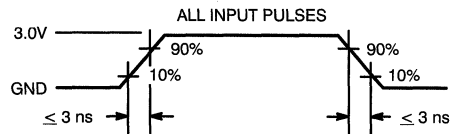
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

6. See the last page of this specification for Group A subgroup testing information. 7. See Introduction to CMOS PROMs in this Data Book for general information on testing.

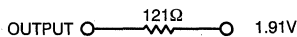
AC Test Loads and Waveforms

(a) Normal Load

(b) High-Z Load

H256-5



H256-6

Equivalent to: THÉVENIN EQUIVALENT



Erase Characteristics

Wavelengths of light less than 4000 Å begin to erase the CY27H256 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm². For an ultraviolet lamp with a 12 mW/cm² power rating, the exposure time would be approximately 35 minutes. The CY27H256 needs to be within 1 inch of the lamp

during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm² is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V _{PP}	Programming Power Supply	12.5	13	V
I _{PP}	Programming Supply Current		50	mA
V _{IHP}	Programming Input Voltage HIGH	3.0	V _{CC}	V
V _{ILP}	Programming Input Voltage LOW	-0.5	0.4	V
V _{CCP}	Programming V _{CC}	6.0	6.5	V

Table 2. Mode Selection

Mode	Pin Function ^[8]					
	\overline{CE}	\overline{OE}	V _{PP}	A ₀	A ₉	Data
Read	V _{IL}	V _{IL}	V _{IH}	A ₀	A ₉	O ₇ - O ₀
Output Disable	V _{IL}	V _{IH}	V _{IH}	A ₀	A ₉	High Z
Stand-by	V _{IH}	X	V _{IH}	X	X	High Z
Program	V _{ILP}	V _{IHP}	V _{PP}	A ₀	A ₉	D ₇ - D ₀
Program Verify	V _{IHP}	V _{ILP}	V _{PP}	A ₀	A ₉	O ₇ - O ₀
Program Inhibit	V _{IHP}	V _{IHP}	V _{PP}	A ₀	A ₉	High Z
Signature Read (MFG)	V _{IL}	V _{IL}	V _{IH}	V _{IL}	V _{HV} ^[9]	34H
Signature Read (DEV)	V _{IL}	V _{IL}	V _{IH}	V _{IH}	V _{HV} ^[9]	21H

Notes:

8. X can be V_{IL} or V_{IH}.

9. V_{HV} = 12 ± 0.5V

Ordering Information^[10]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY27H256-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256-25ZC	Z28	28-Lead Thin Small Outline Package	
30	CY27H256-30JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256-30PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H256-30WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H256-30ZC	Z28	28-Lead Thin Small Outline Package	
35	CY27H256-35JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256-35PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H256-35WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H256-35ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H256-35LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military
	CY27H256-35QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
45	CY27H256-45JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256-45PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H256-45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H256-45ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H256-45DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27H256-45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H256-45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H256-45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
55	CY27H256-55JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256-55PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H256-55WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H256-55ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H256-55DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27H256-55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H256-55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H256-55WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
70	CY27H256-70JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256-70PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H256-70WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H256-70ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H256-70DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27H256-70LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H256-70QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H256-70WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

Note:

10. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

64K x 8 High-Speed CMOS EPROM

Features

- CMOS for optimum speed/power
- High speed
 - $t_{AA} = 25$ ns max. (commercial)
 - $t_{AA} = 35$ ns max. (military)
- Low power
 - 275 mW max.
 - Less than 85 mW when deselected
- Byte-wide memory organization
- 100% reprogrammable in the windowed package
- EPROM technology
- Capable of withstanding >2001V static discharge
- Available in
 - 32-pin PLCC
 - 28-pin TSOP-I
 - 28-pin, 600-mil plastic or hermetic DIP
 - 32-pin hermetic LCC

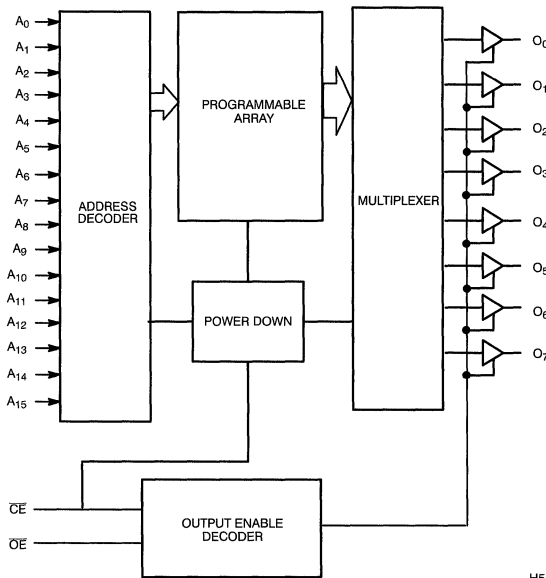
Functional Description

The CY27H512 is a high-performance, 512K CMOS EPROM organized in 64 Kbytes. It is available in industry-standard 28-pin, 600-mil DIP, 32-pin LCC and PLCC, and 28-pin TSOP-I packages. These devices offer high-density storage combined with 40-MHz performance. The CY27H512 is available in windowed and opaque packages. Windowed packages allow the device to be erased with UV light for 100% reprogrammability.

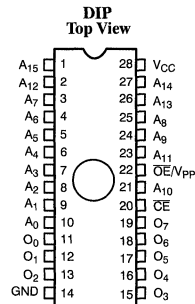
The CY27H512 is equipped with a power-down chip enable (\overline{CE}) input and output enable (\overline{OE}). When \overline{CE} is deasserted, the device powers down to a low-power standby mode. The \overline{OE} pin three-states the outputs without putting the device into standby mode. While \overline{CE} offers lower power, \overline{OE} provides a more rapid transition to and from three-stated outputs.

The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms. The EPROM cell requires only 12.75 V for the supervoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

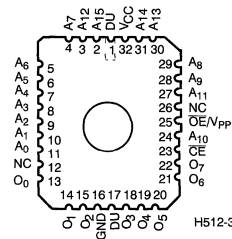
The CY27H512 is read by asserting both the \overline{CE} and the \overline{OE} inputs. The contents of the memory location selected by the address on inputs $A_{15}-A_0$ will appear at the outputs O_7-O_0 .

Logic Block Diagram


H512-1

Pin Configurations


H512-2

LCC/PLCC^[1] Top View


H512-3

Note:

1. For LCC/PLCC only; Pins 1 and 17 are common and tied to the die attach pad. They should not be used.

Electrical Characteristics Over the Operating Range^[6, 7]

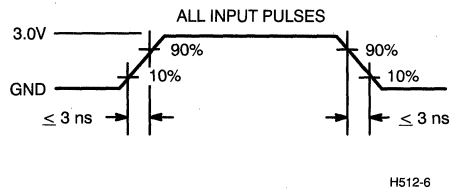
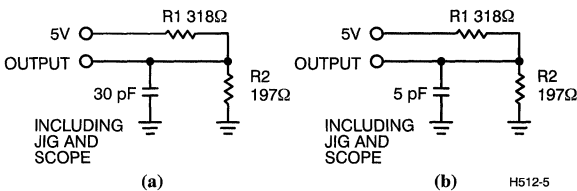
Parameter	Description	Test Conditions	27H512-25 27H512-30		27H512-35		27H512-45 27H512-55 27H512-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 12.0 mA		0.45		0.45		0.45	V
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs	2.0	V _{CC} +0.5	2.0	V _{CC} +0.5	2.0	V _{CC} +0.5	V
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		0.8		0.8		0.8	V
I _{Ix}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}	-10	+10	-10	+10	-10	+10	μA
I _{Oz}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disable	-10	+10	-10	+10	-10	+10	μA
I _{CC}	Power Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=10 MHz	Com'l	75		50		50	mA
			Mil			85		60	mA
I _{SB}	Stand-By Current	V _{CC} =Max., CE = V _{IH}	Com'l	15		15		15	mA
			Mil			25		25	mA

Capacitance^[7]

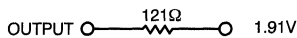
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

6. See the last page of this specification for Group A subgroup testing information. 7. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT



Erasure Characteristics

Wavelengths of light less than 4000 Å begin to erase the CY27H512 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm². For an ultraviolet lamp with a 12 mW/cm² power rating, the exposure time would be approximately 35 minutes. The CY27H512 needs to be within 1 inch of the lamp

during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm² is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V _{PP}	Programming Power Supply	12.5	13	V
I _{PP}	Programming Supply Current		50	mA
V _{IHP}	Programming Input Voltage HIGH	3.0	V _{CC}	V
V _{ILP}	Programming Input Voltage LOW	-0.5	0.4	V
V _{CCP}	Programming VCC	6.0	6.5	V

Table 2. Mode Selection

Mode	Pin Function ^[8]				
	\overline{CE}	\overline{OE}/V_{PP}	A ₀	A ₉	Data
Read	V _{IL}	V _{IL}	A ₀	A ₉	O ₇ - O ₀
Output Disable	X	V _{IH}	A ₀	A ₉	High Z
Stand-by	V _{IH}	X	X	X	High Z
Program	V _{ILP}	V _{PP}	A ₀	A ₉	D ₇ - D ₀
Program Verify	V _{ILP}	V _{ILP}	A ₀	A ₉	O ₇ - O ₀
Program Inhibit	V _{IHP}	V _{PP}	A ₀	A ₉	High Z
Signature Read (MFG)	V _{IL}	V _{IL}	V _{IL}	V _{HV} ^[9]	34H
Signature Read (DEV)	V _{IL}	V _{IL}	V _{IH}	V _{HV} ^[9]	1FH

Note:

8. X can be V_{IL} or V_{IH}.

9. V_{HV}=12±0.5V.

Ordering Information^[10]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY27H512-25HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H512-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H512-25ZC	Z28	28-Lead Thin Small Outline Package	
30	CY27H512-30HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H512-30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H512-30PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H512-30WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H512-30ZC	Z28	28-Lead Thin Small Outline Package	
35	CY27H512-35HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H512-35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H512-35PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H512-35WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H512-35ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H512-35HMB	H65	32-Pin Windowed Leaded Chip Carrier	Military
	CY27H512-35LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H512-35QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
45	CY27H512-45HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H512-45JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H512-45PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H512-45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H512-45ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H512-45DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27H512-45HMB	H65	32-Pin Windowed Leaded Chip Carrier	
	CY27H512-45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H512-45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H512-45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
55	CY27H512-55HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H512-55JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H512-55PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H512-55WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H512-55ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H512-55DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27H512-55HMB	H65	32-Pin Windowed Leaded Chip Carrier	
	CY27H512-55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H512-55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H512-55WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

Notes:

10. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.



512 x 8 Registered PROM

Features

- CMOS for optimum speed/power
- High speed
 - 18 ns address set-up
 - 12 ns clock to output
- Low power
 - 495 mW (commercial)
 - 660 mW (military)
- Synchronous and asynchronous output enables
- On-chip edge-triggered registers
- Buffered common PRESET and CLEAR inputs
- EPROM technology, 100% programmable

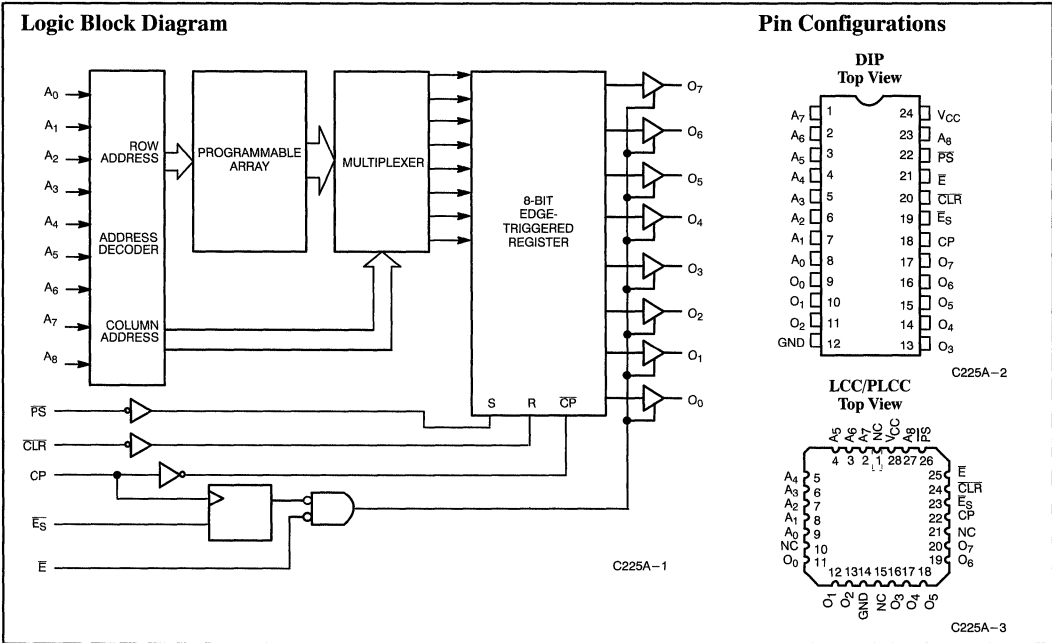
- Slim 300-mil, 24-pin plastic or hermetic DIP, 28-pin LCC, or 28-pin PLCC
- $5V \pm 10\% V_{CC}$, commercial and military
- TTL-compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 2001V static discharge

Functional Description

The CY7C225A is a high-performance 512 word by 8 bit electrically programmable read only memory packaged in a slim 300-mil plastic or hermetic DIP, 28-pin leadless chip carrier, and 28-pin PLCC.

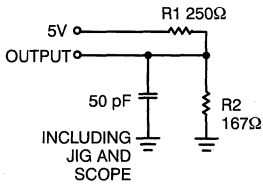
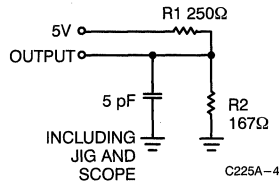
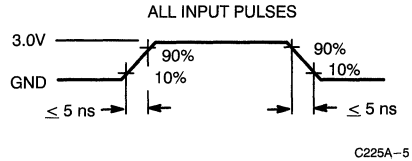
The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C225A replaces bipolar devices and offers the advantages of lower power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

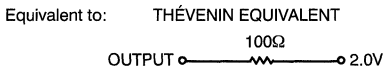


Selection Guide

	7C225A-18	7C225A-25	7C225A-30	7C225A-35	7C225A-40
Minimum Address Set-Up Time (ns)	18	25	30	35	40
Maximum Clock to Output (ns)	12	12	15	20	25
Maximum Operating Current (mA)	Commercial	90	90	90	90
	Military		120	120	120

AC Test Loads and Waveforms^[4]

(a) Normal Load

(b) High Z Load


C225A-5


Operating Modes

The CY7C225A incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous (\overline{E}_S) and asynchronous (\overline{E}) output enables and \overline{CLEAR} and \overline{PRESET} inputs.

Upon power-up, the synchronous enable (\overline{E}_S) flip-flop will be in the set condition causing the outputs ($O_0 - O_7$) to be in the OFF or high-impedance state. Data is read by applying the memory location to the address inputs ($A_0 - A_8$) and a logic LOW to the enable (\overline{E}_S) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs ($O_0 - O_7$) provided the asynchronous enable (\overline{E}) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable (\overline{E}) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Regardless of the condition of \overline{E} , the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable (\overline{E}_S) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if \overline{E} is LOW. Following a positive clock edge, the address and syn-

chronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C225A decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge-triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C225A has buffered asynchronous \overline{CLEAR} and \overline{PRESET} inputs. Applying a LOW to the \overline{PRESET} input causes an immediate load of all ones into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). Applying a LOW to the \overline{CLEAR} input, resets the flip-flops to all zeros. The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable (\overline{E}) LOW.

When power is applied, the (internal) synchronous enable flip-flop will be in a state such that the outputs will be in the high-impedance state. In order to enable the outputs, a clock must occur and the \overline{E}_S input pin must be LOW at least a set-up time prior to the clock LOW-to-HIGH transition. The \overline{E} input may then be used to enable the outputs.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please

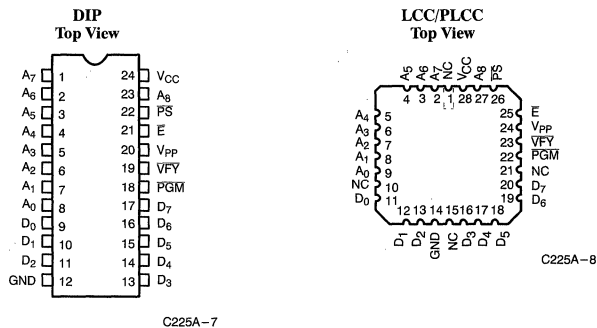
see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode	Pin Function ^[8]							
	Read or Output Disable	A ₈ - A ₀	CP	\bar{E}_S	CLR	\bar{E}	PS	O ₇ - O ₀
	Other	A ₈ - A ₀	PGM	VFY	V _{PP}	\bar{E}	PS	D ₇ - D ₀
Read		A ₈ - A ₀	X	V _{IL}	V _{IH}	V _{IL}	V _{IH}	O ₇ - O ₀
Output Disable		A ₈ - A ₀	X	V _{IH}	V _{IH}	X	V _{IH}	High Z
Output Disable		A ₈ - A ₀	X	X	V _{IH}	V _{IH}	V _{IH}	High Z
Clear		A ₈ - A ₀	X	V _{IL}	V _{IL}	V _{IL}	V _{IH}	Zeros
Preset		A ₈ - A ₀	X	V _{IL}	V _{IH}	V _{IL}	V _{IL}	Ones
Program		A ₈ - A ₀	V _{ILP}	V _{IHP}	V _{PP}	V _{IHP}	V _{IHP}	D ₇ - D ₀
Program Verify		A ₈ - A ₀	V _{IHP}	V _{ILP}	V _{PP}	V _{IHP}	V _{IHP}	O ₇ - O ₀
Program Inhibit		A ₈ - A ₀	V _{IHP}	V _{IHP}	V _{PP}	V _{IHP}	V _{IHP}	High Z
Intelligent Program		A ₈ - A ₀	V _{ILP}	V _{IHP}	V _{PP}	V _{IHP}	V _{IHP}	D ₇ - D ₀
Blank Check		A ₈ - A ₀	V _{IHP}	V _{ILP}	V _{PP}	V _{IHP}	V _{IHP}	Zeros

Note:

8. X = "don't care" but not to exceed V_{CC} ±5%.


Figure 1. Programming Pinouts

Ordering Information^[9]

Speed (ns)		Ordering Code	Package Type	Package Type	Operating Range
t _{SA}	t _{CO}				
18	12	CY7C225A-18DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225A-18JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225A-18PC	P13	24-Lead (300-Mil) Molded DIP	
25	12	CY7C225A-25DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225A-25JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225A-25PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C225A-25DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225A-25LMB	L64	28-Square Leadless Chip Carrier	
30	15	CY7C225A-30DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225A-30JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225A-30PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C225A-30DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225A-30LMB	L64	28-Square Leadless Chip Carrier	
35	20	CY7C225A-35DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225A-35LMB	L64	28-Square Leadless Chip Carrier	
40	25	CY7C225A-40DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225A-40JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225A-40PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C225A-40DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225A-40LMB	L64	28-Square Leadless Chip Carrier	

Note:

9. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

**MILITARY SPECIFICATIONS
Group A Subgroup Testing**
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{SA}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{CO}	7, 8, 9, 10, 11
t _{DP}	7, 8, 9, 10, 11
t _{RP}	7, 8, 9, 10, 11

Document #: 38-00228-C

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12 for DIP)	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-3.0V to +7.0V
DC Program Voltage (Pins 7, 18, 20 for DIP)	13.0V

Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial ^[1]	-40°C to +85°C	5V ±10%
Military ^[2]	-55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range^[3]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA V _{IN} = V _{IH} or V _{IL}	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 16 mA V _{IN} = V _{IH} or V _{IL}		0.4	V
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs ^[4]	2.0		V
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs ^[4]		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}	-10	+10	μA
V _{CD}	Input Clamp Diode Voltage	Note 5			
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} Output Disabled ^[4]	-10	+10	μA
I _{OS}	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = 0.0V ^[6]	-20	-90	mA
I _{CC}	Power Supply Current	I _{OUT} = 0 mA, V _{CC} = Max.	Commercial	90	mA
			Military	120	
V _{PP}	Programming Supply Voltage		12	13	V
I _{PP}	Programming Supply Current			50	mA
V _{IHP}	Input HIGH Programming Voltage		3.0		V
V _{ILP}	Input LOW Programming Voltage			0.4	V

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

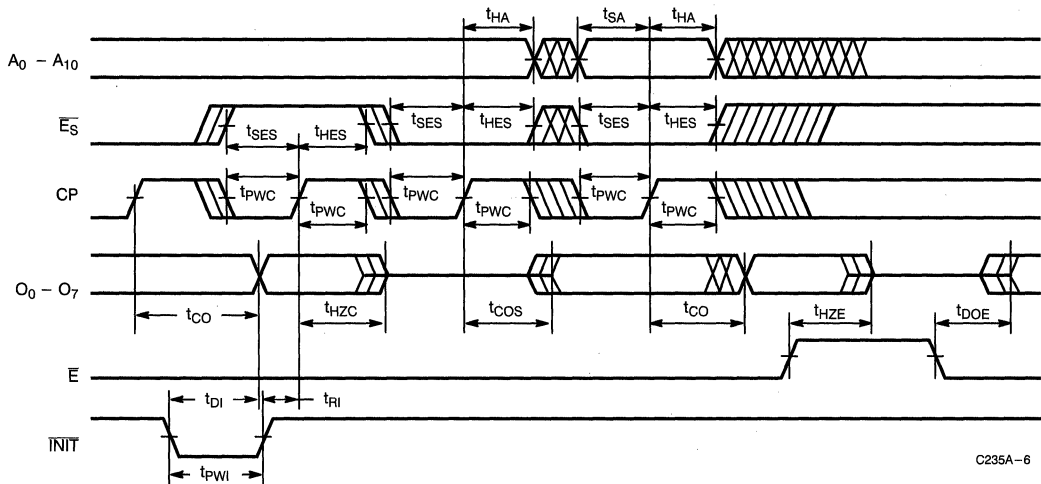
- Contact a Cypress representative for industrial temperature range specifications.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
- See Introduction to CMOS PROMs in this Data Book for general information on testing.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

Switching Characteristics Over Operating Range^[3,5]

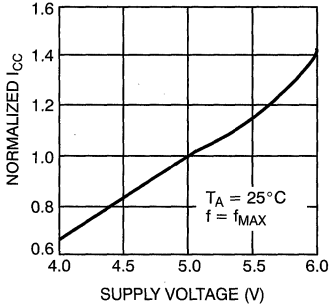
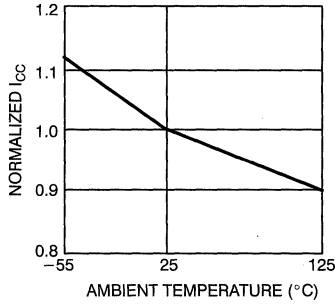
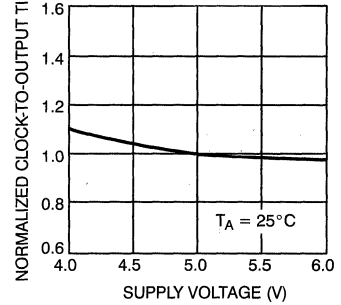
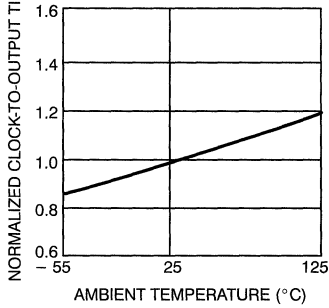
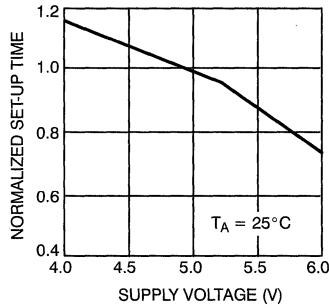
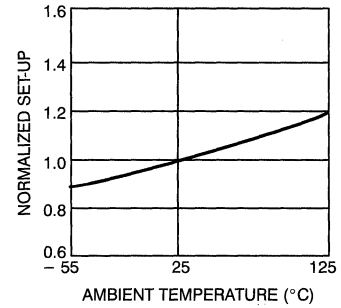
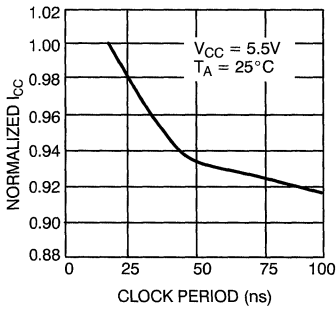
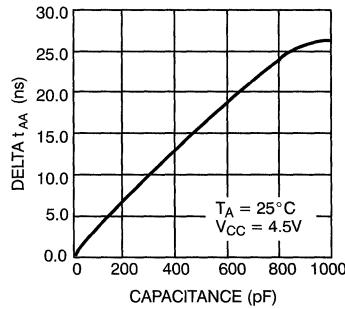
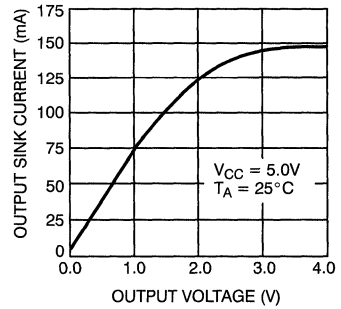
Parameter	Description	7C235A-18		7C235A-25		7C235A-30		7C235A-40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	18		25		30		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		12		15		20	ns
t_{PWC}	Clock Pulse Width	12		12		15		20		ns
t_{SES}	\overline{E}_S Set-Up to Clock HIGH	10		10		10		15		ns
t_{HES}	\overline{E}_S Hold from Clock HIGH	5		5		5		5		ns
t_{DI}	Delay from \overline{INIT} to Valid Output		20		25		25		35	ns
t_{RI}	\overline{INIT} Recovery to Clock HIGH	15		20		20		20		ns
t_{PWI}	\overline{INIT} Pulse Width	15		20		20		25		ns
t_{COS}	Inactive to Valid Output from Clock HIGH ^[7]		15		20		20		25	ns
t_{HZC}	Inactive Output from Clock HIGH ^[7]		15		20		20		25	ns
t_{DOE}	Valid Output from \overline{E} LOW		15		20		20		25	ns
t_{HZE}	Inactive Output from \overline{E} HIGH		15		20		20		25	ns

Note:

 7. Applies only when the synchronous (\overline{E}_S) function is used.

Switching Waveforms^[5]


C235A-6

Typical DC and AC Characteristics
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE

CLOCK TO OUTPUT TIME vs. VCC

CLOCK TO OUTPUT TIME vs. TEMPERATURE

NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE

NORMALIZED SET-UP TIME vs. TEMPERATURE

NORMALIZED SUPPLY CURRENT vs. CLOCK PERIOD

TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING

OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE


4K x 8 Reprogrammable PROM

Features

- CMOS for optimum speed/power
- Windowed for reprogrammability
- High speed
 - 20 ns (commercial)
 - 25 ns (military)
- Low power
 - 550 mW (commercial)
 - 660 mW (military)
- EPROM technology 100% programmable
- 300-mil or 600-mil packaging available
- $5V \pm 10\% V_{CC}$, commercial and military

- Capable of withstanding greater than 2001V static discharge
- TTL-compatible I/O
- Direct replacement for bipolar PROMs

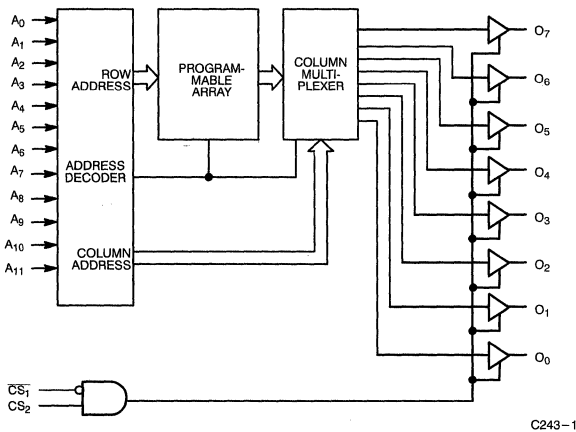
Functional Description

The CY7C243 and CY7C244 are high-performance 4K x 8 CMOS PROMs. The CY7C243 and CY7C244 are packaged in 300-mil-wide and 600-mil-wide packages respectively. The reprogrammable packages are equipped with an erasure window. When exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

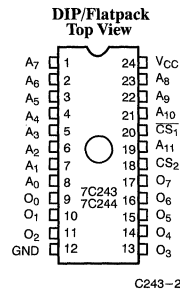
The CY7C243 and CY7C244 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each cell is programmed, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Read is accomplished by placing an active LOW signal on \overline{CS}_1 and an active HIGH on CS_2 . The contents of the memory location addressed by the address line ($A_0 - A_{11}$) will become available on the output lines ($O_0 - O_7$).

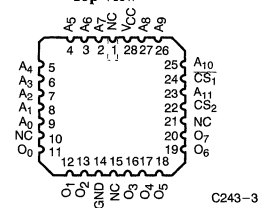
Logic Block Diagram



Pin Configurations

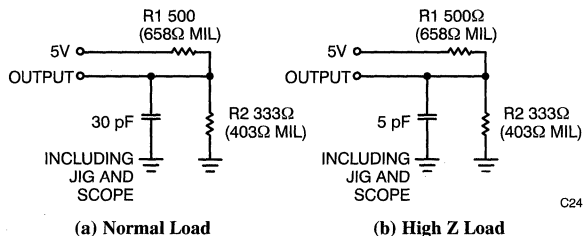


LCC/PLCC (Opaque Only) Top View



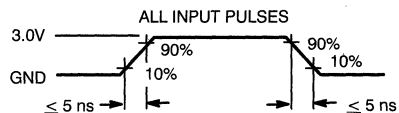
Selection Guide

		7C243-20 7C244-20	7C243-25 7C244-25	7C243-35 7C244-35	7C243-45 7C244-45	7C243-55 7C244-55
Maximum Access Time (ns)		20	25	35	45	55
Maximum Operating Current (mA)	Commercial	100	100	80	80	80
	Military		120	100	100	100

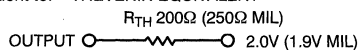
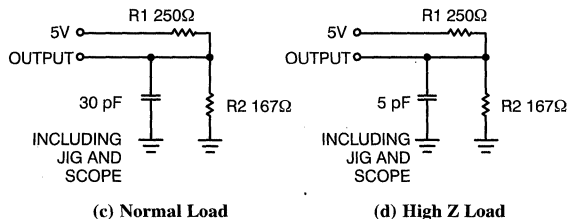
AC Test Loads and Waveforms^[4]
Test Load for -20 through -25 speeds


C243-4

C243-5

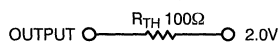


Equivalent to: THÉVENIN EQUIVALENT

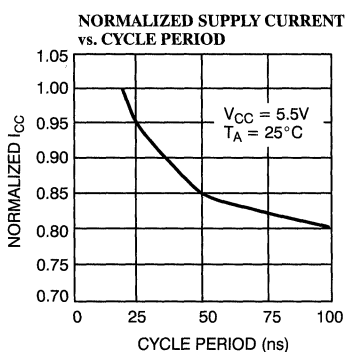
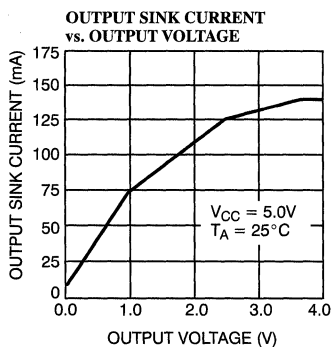
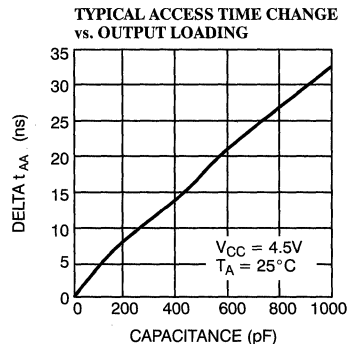
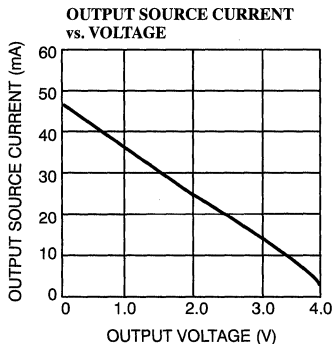
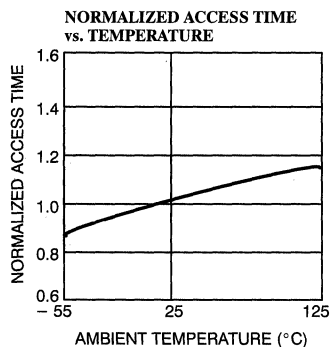
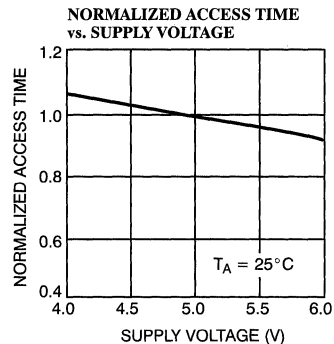
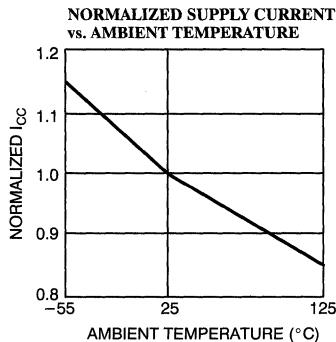
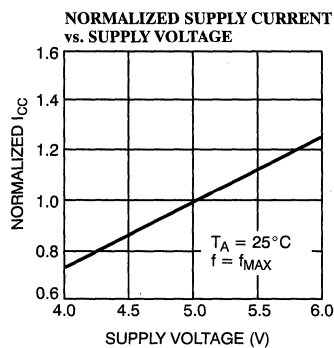

Test Load for -35 through -55 speeds


C243-6

Equivalent to: THÉVENIN EQUIVALENT


Switching Characteristics Over the Operating Range^[2, 3, 4]

Parameter	Description	7C243-20 7C244-20		7C243-25 7C244-25		7C243-35 7C244-35		7C243-45 7C244-45		7C243-55 7C244-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		20		25		35		45		55	ns
t_{HZCS} (Com'l)	Chip Select Inactive to High Z		12		12		20		25		25	ns
t_{HZCS} (Mil)	Chip Select Inactive to High Z				15		20		25		25	ns
t_{ACS} (Com'l)	Chip Select Active to Output Valid		12		12		20		25		25	ns
t_{ACS} (Mil)	Chip Select Active to Output Valid				15		20		25		25	ns

Typical DC and AC Characteristics


Ordering Information (continued)^[7]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C244-20PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
	CY7C244-20WC	W12	24-Lead (600-Mil) Windowed CerDIP	
25	CY7C244-25PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
	CY7C244-25WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C244-25DMB	D12	24-Lead (600-Mil) CerDIP	Military
35	CY7C244-25WMB	W12	24-Lead (600-Mil) Windowed CerDIP	Commercial
	CY7C244-35PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C244-35WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C244-35DMB	D12	24-Lead (600-Mil) CerDIP	
45	CY7C244-35WMB	W12	24-Lead (600-Mil) Windowed CerDIP	Commercial
	CY7C244-45PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C244-45WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C244-45DMB	D12	24-Lead (600-Mil) CerDIP	
55	CY7C244-45WMB	W12	24-Lead (600-Mil) Windowed CerDIP	Commercial
	CY7C244-55PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C244-55WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C244-55DMB	D12	24-Lead (600-Mil) CerDIP	
	CY7C244-55WMB	W12	24-Lead (600-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{AA}	7, 8, 9, 10, 11
t _{ACS}	7, 8, 9, 10, 11

Document #: 38-00360-A

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12)	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-3.0V to +7.0V
DC Program Voltage (Pins 7, 18, 20)	13.0V
UV Erasure	7258 Wsec/cm ²

Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial ^[1]	-40°C to +85°C	5V ±10%
Military ^[2]	-55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range^[3, 4]

Parameter	Description	Test Conditions	7C245A-15		7C245A-18		7C245A-25 7C245A-35 7C245A-45		7C245AL-25 7C245AL-35 7C245AL-45		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA V _{IN} = V _{IH} or V _{IL}	2.4		2.4		2.4		2.4		V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 16 mA V _{IN} = V _{IH} or V _{IL}		0.4		0.4		0.4		0.4	V	
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage, for All Inputs	2.0	V _{CC}	2.0	V _{CC}	2.0	V _{CC}	2.0	V _{CC}	V	
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage, for All Inputs		0.8		0.8		0.8		0.8	V	
I _{IX}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}	-10	+10	-10	+10	-10	+10	-10	+10	µA	
V _{CD}	Input Clamp Diode Voltage	Note 4										
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} Output Disabled ^[5]	-10	+10	-10	+10	-10	+10	-10	+10	µA	
I _{OS}	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = 0.0V ^[6]	-20	-90	-20	-90	-20	-90	-20	-90	mA	
I _{CC}	Power Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com ¹		120		120		90		60	
			Mil				120		120			
V _{PP}	Programming Supply Voltage		12	13	12	13	12	13	12	13	V	
I _{PP}	Programming Supply Current			50		50		50		50	mA	
V _{IHP}	Input HIGH Programming Voltage		3.0		3.0		3.0		3.0		V	
V _{ILP}	Input LOW Programming Voltage			0.4		0.4		0.4		0.4	V	

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

- Contact a Cypress representative for industrial temperature range specifications.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
- For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

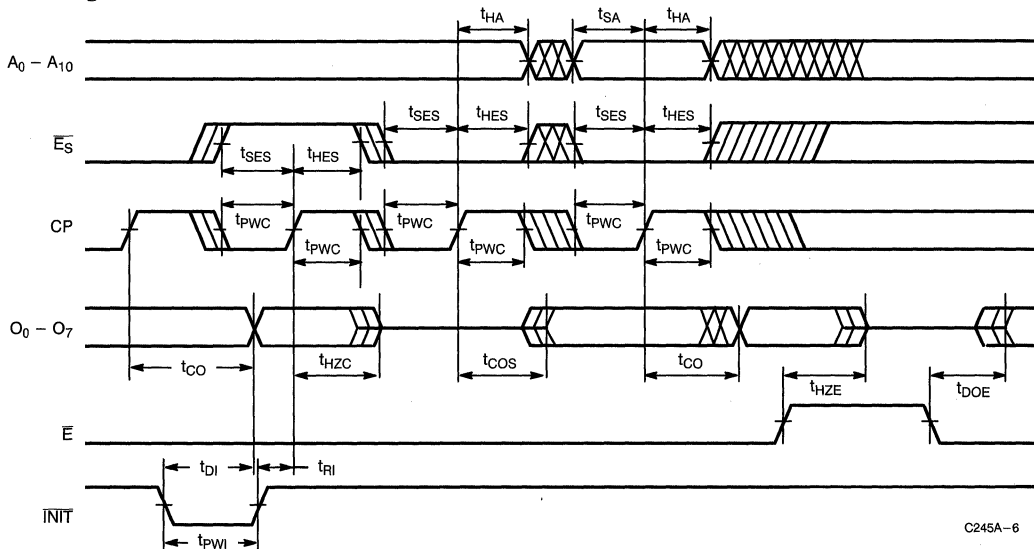
Operating Modes (continued)

sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C245A has an asynchronous initialize input ($\overline{\text{INIT}}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated, the initialize control input causes the contents of a user-programmed 2049th 8-bit word to be loaded into the on-chip register.

Switching Waveforms^[4]



C245A-6

Erase Characteristics

Wavelengths of light less than 4000 Å begin to erase the 7C245A. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm². For an ultraviolet lamp with a 12 mW/cm² power rating the exposure time would be approximately 35 minutes. The 7C245A needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm² is the recommended maximum dosage.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of

grammed 2049th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of 1s and 0s into the register. In the unprogrammed state, activating $\overline{\text{INIT}}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{\text{INIT}}$ performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\overline{\text{INIT}}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable (\overline{E}) LOW.

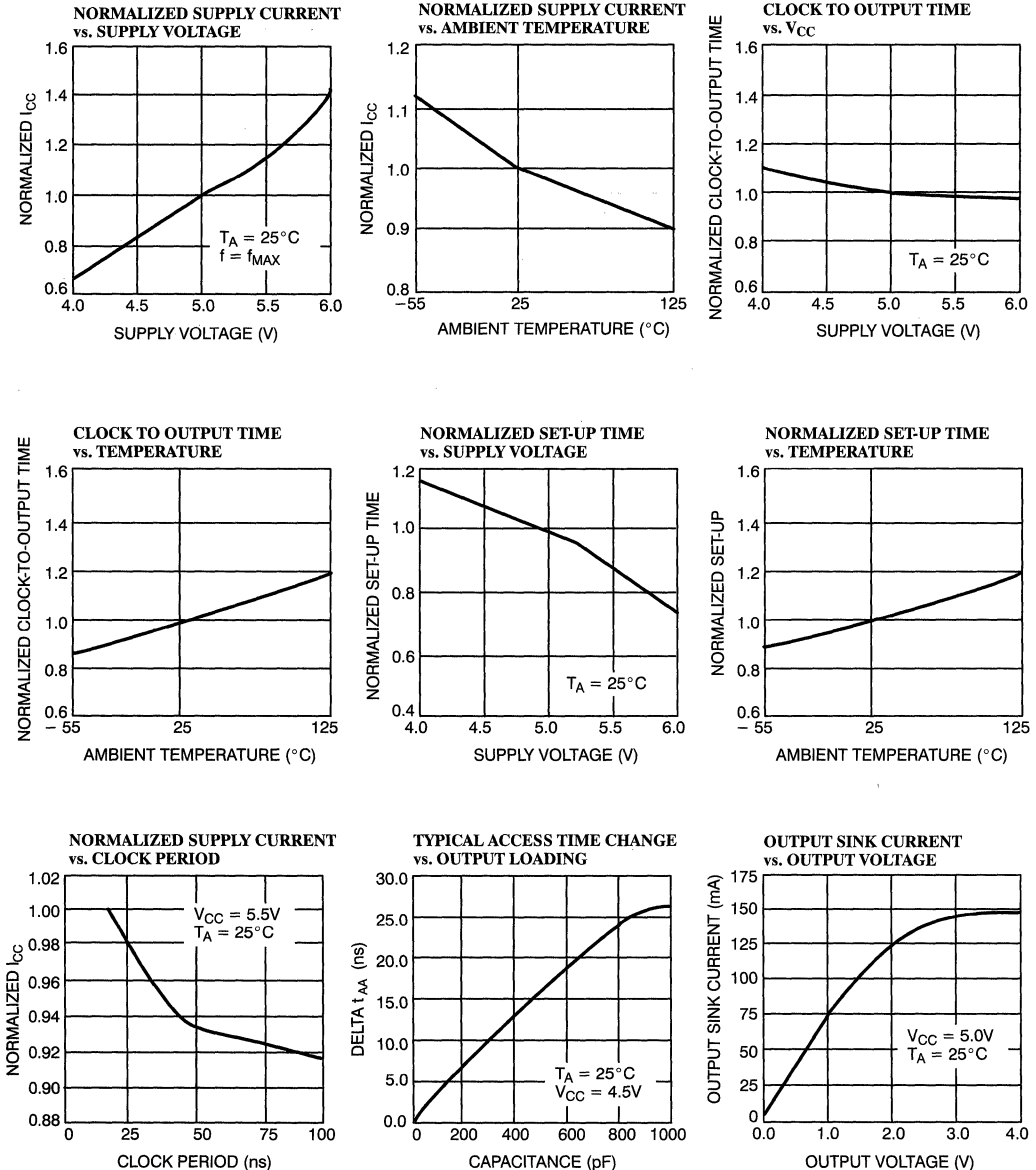
this section. Programming algorithms can be obtained from any Cypress representative.

Bit Map Data

Programmer Address		RAM Data
Decimal	Hex	Contents
0	0	Data
.	.	.
.	.	.
2047	7FF	Data
2048	800	Init Byte
2049	801	Control Byte

Control Byte

- 00 Asynchronous output enable (default state)
- 01 Synchronous output enable

Typical DC and AC Characteristics


**MILITARY SPECIFICATIONS
Group A Subgroup Testing**
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{Ix}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{SA}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{CO}	7, 8, 9, 10, 11

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962-88735	01KX	CY7C245A-45KMB
5962-88735	01LX	CY7C245A-45DMB
5962-88735	013X	CY7C245A-45LMB
5962-88735	02KX	CY7C245A-35KMB
5962-88735	02LX	CY7C245A-35DMB
5962-88735	023X	CY7C245A-35LMB
5962-88735	03KX	CY7C245A-35KMB
5962-88735	03LX	CY7C245A-35DMB
5962-88735	033X	CY7C245A-25LMB
5962-88735	04KX	CY7C245A-25KMB
5962-88735	04LX	CY7C245A-25DMB
5962-88735	043X	CY7C245A-25LMB
5962-87529	01KX	CY7C245A-45TMB
5962-87529	01LX	CY7C245A-45WMB
5962-87529	013X	CY7C245A-45QMB
5962-87529	02KX	CY7C245A-35TMB
5962-87529	02LX	CY7C245A-35WMB
5962-87529	023X	CY7C245A-35QMB
5962-89815	01LX	CY7C245A-35WMB
5962-89815	01KX	CY7C245A-35TMB
5962-89815	013X	CY7C245A-35QMB
5962-89815	02LX	CY7C245A-25WMB
5962-89815	02KX	CY7C245A-25TMB
5962-89815	023X	CY7C245A-25QMB
5962-89815	03LX	CY7C245A-18WMB
5962-89815	03KX	CY7C245A-18TMB
5962-89815	033X	CY7C245A-18QMB

Document #: 38-00074-G

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 28 to Pin 14)	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-3.0V to +7.0V
DC Program Voltage (Pin 22)	13.5V

Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	>200 mA
UV Exposure	7258 Wsec/cm ²

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial ^[1]	-40°C to +85°C	5V ±10%
Military ^[2]	-55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range^[3, 4]

Parameter	Description	Test Conditions	7C251-45, 55, 65 7C254-45, 55, 65		Unit
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 16.0 mA		0.5	V
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs	2.0		V
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		0.8	V
I _{IX}	Input Current	GND ≤ V _{IN} ≤ V _{CC}	-10	+10	µA
V _{CD}	Input Diode Clamp Voltage		Note 4		
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled	-40	+40	µA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND	-20	-90	mA
I _{CC}	Power Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	100	mA
			Mil	120	
I _{SB}	Standby Supply Current (7C251)	V _{CC} = Max., CS ₁ = V _{IH} , I _{OUT} = 0 mA	Com'l	30	mA
			Mil	35	
V _{PP}	Programming Supply Voltage		12	13	V
I _{PP}	Programming Supply Current			50	mA
V _{IHP}	Input HIGH Programming Voltage		3.0		V
V _{ILP}	Input LOW Programming Voltage			0.4	V

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

- Contact a Cypress representative regarding industrial temperature range specification.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

Erase Characteristics

Wavelengths of light less than 4000 Å begin to erase the 7C251 and 7C254 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity x exposure time) of 25 Wsec/cm². For an ultraviolet lamp with a 12 mW/cm² power rating, the exposure time would be approximately 35 minutes. The 7C251 or 7C254 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm² is the recommended maximum dosage.

Blankcheck

Blankcheck is accomplished by performing a verify cycle (\overline{VFY} toggles on each address), sequencing through all memory address locations, where all the data read will be zeros.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode	Pin Function ^[8]						
	Read or Output Disable	A ₁₃ - A ₀	\overline{CS}_4	CS ₃	\overline{CS}_2	\overline{CS}_1	O ₇ - O ₀
	Other	A ₁₃ - A ₀	NA	\overline{VFY}	V _{PP}	\overline{PGM}	D ₇ - D ₀
Read		A ₁₃ - A ₀	V _{IL}	V _{IH}	V _{IL}	V _{IL}	O ₇ - O ₀
Output Disable		A ₁₃ - A ₀	X	X	X	V _{IH}	High Z
Output Disable		A ₁₃ - A ₀	X	X	V _{IH}	X	High Z
Output Disable		A ₁₃ - A ₀	X	V _{IL}	X	X	High Z
Output Disable		A ₁₃ - A ₀	V _{IH}	X	X	X	High Z
Program		A ₁₃ - A ₀	X	V _{IHP}	V _{PP}	V _{ILP}	D ₇ - D ₀
Program Verify		A ₁₃ - A ₀	X	V _{ILP}	V _{PP}	V _{IHP}	O ₇ - O ₀
Program Inhibit		A ₁₃ - A ₀	X	V _{IHP}	V _{PP}	V _{IHP}	High Z
Blank Check		A ₁₃ - A ₀	X	V _{ILP}	V _{PP}	V _{IHP}	O ₇ - O ₀

Note:

8. X = "don't care" but not to exceed V_{CC} ±5%.

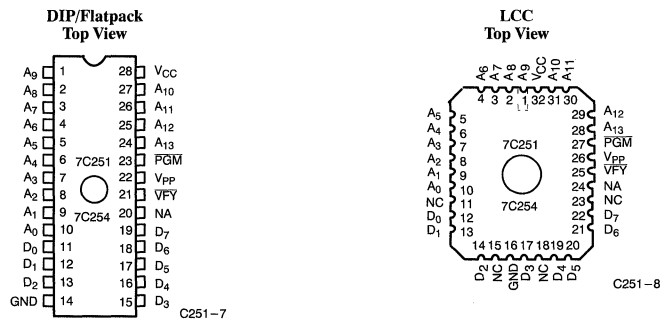


Figure 1. Programming Pinout

Ordering Information^[9]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY7C251-45PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C251-45WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C251-45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C251-45WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
55	CY7C251-55PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C251-55WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C251-55DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C251-55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C251-55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C251-55WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
65	CY7C251-65PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C251-65WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C251-65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C251-65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C251-65QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C251-65WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY7C254-45PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C254-45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C254-45DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C254-45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
55	CY7C254-55PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C254-55WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C254-55DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C254-55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C254-55WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
65	CY7C254-65PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C254-65WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C254-65DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C254-65QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C254-65WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

Note:

9. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.



CY7C261 CY7C263/CY7C264

8K x 8 Power-Switched and Reprogrammable PROM

Features

- CMOS for optimum speed/power
- Windowed for reprogrammability
- High speed
 - 20 ns (commercial)
 - 25 ns (military)
- Low power
 - 660 mW (commercial)
 - 770 mW (military)
- Super low standby power (7C261)
 - Less than 220 mW when deselected
 - Fast access: 20 ns
- EPROM technology 100% programmable
- Slim 300-mil or standard 600-mil packaging available
- 5V ± 10% V_{CC}, commercial and military

- Capable of withstanding greater than 2001V static discharge
- TTL-compatible I/O
- Direct replacement for bipolar PROMs

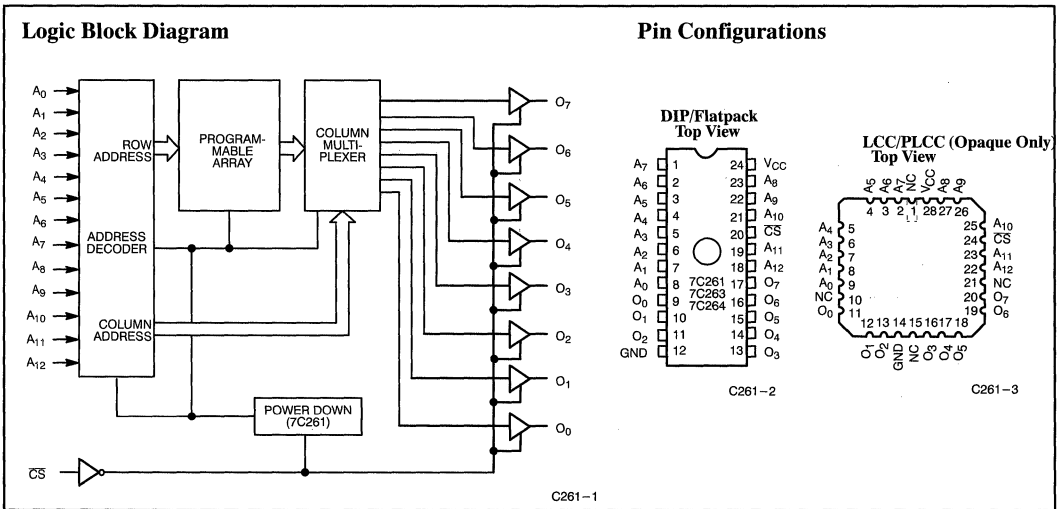
Functional Description

The CY7C261, CY7C263, and CY7C264 are high-performance 8192-word by 8-bit CMOS PROMs. When deselected, the 7C261 automatically powers down into a low-power standby mode. It is packaged in a 300-mil-wide package. The 7C263 and 7C264 are packaged in 300-mil-wide and 600-mil-wide packages respectively, and do not power down when deselected. The reprogrammable packages are equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM

floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C261, CY7C263, and CY7C264 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

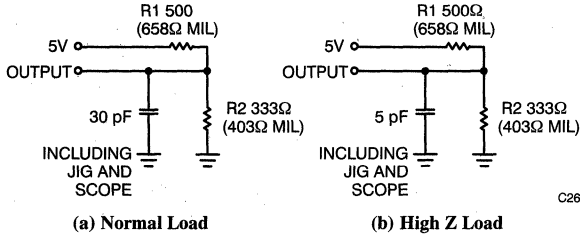
Read is accomplished by placing an active LOW signal on CS. The contents of the memory location addressed by the address line (A₀ – A₁₂) will become available on the output lines (O₀ – O₇).



Selection Guide

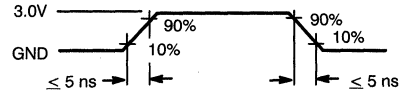
		7C261-20 7C263-20 7C264-20	7C261-25 7C263-25 7C264-25	7C261-35 7C263-35 7C264-35	7C261-45 7C263-45 7C264-45	7C261-55 7C263-55 7C264-55
Maximum Access Time (ns)		20	25	35	45	55
Maximum Operating Current (mA)	Commercial	120	120	100	100	100
	Military		140	120	120	120
Maximum Standby Current (mA) (7C261 only)	Commercial	40	40	30	30	30
	Military		40	30	30	30

For an 8K x 8 Registered PROM, see the CY7C265.

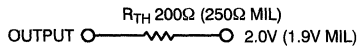
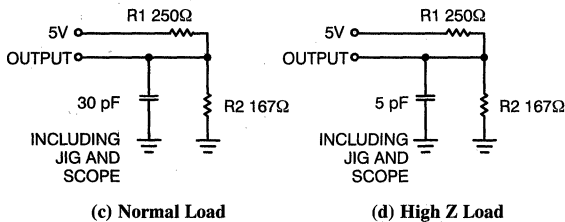
AC Test Loads and Waveforms^[4]
Test Load for -20 through -30 speeds


C261-4

C261-5

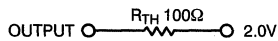


Equivalent to: THEVENIN EQUIVALENT


Test Load for -35 through -55 speeds


C261-6

Equivalent to: THEVENIN EQUIVALENT


Switching Characteristics Over the Operating Range^[2, 3, 4]

Parameter	Description	7C261-20		7C261-25		7C261-35		7C261-45		7C261-55		Unit
		7C263-20		7C263-25		7C263-35		7C263-45		7C263-55		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		20		25		35		45		55	ns
t_{HZCS1}	Chip Select Inactive to High Z (7C263 and 7C264)		12		12		20		30		35	ns
t_{HZCS2}	Chip Select Inactive to High Z (7C261)		20		25		35		45		55	ns
t_{ACS1}	Chip Select Active to Output Valid (7C263 and 7C264)		12		12		20		30		35	ns
t_{ACS2}	Chip Select Active to Output Valid (7C261)		20		25		35		45		55	ns
t_{PU}	Chip Select Active to Power-Up (7C261)	0		0		0		0		0		ns
t_{PD}	Chip Select Inactive to Power-Down (7C261)		20		25		35		45		55	ns

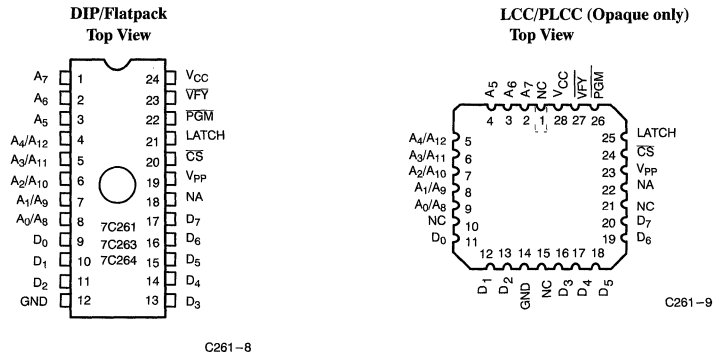


Figure 1. Programming Pinouts

Ordering Information^[8]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C261-20JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C261-20PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C261-20WC	W14	24-Lead (300-Mil) Windowed CerDIP	
25	CY7C261-25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C261-25PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C261-25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C261-25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C261-25LMB	L64	28-Square Leadless Chip Carrier	
	CY7C261-25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C261-25TMB	T73	24-Lead Windowed Cerpack	
	CY7C261-25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
35	CY7C261-35JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C261-35PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C261-35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C261-35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C261-35LMB	L64	28-Square Leadless Chip Carrier	
	CY7C261-35QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C261-35TMB	T73	24-Lead Windowed Cerpack	
	CY7C261-35WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
45	CY7C261-45JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C261-45PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C261-45WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C261-45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C261-45LMB	L64	28-Square Leadless Chip Carrier	
	CY7C261-45QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C261-45TMB	T73	24-Lead Windowed Cerpack	
	CY7C261-45WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
55	CY7C261-55JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C261-55PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C261-55WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C261-55DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C261-55LMB	L64	28-Square Leadless Chip Carrier	
	CY7C261-55QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C261-55TMB	T73	24-Lead Windowed Cerpack	
	CY7C261-55WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

Note:

8. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Ordering Information (continued)^[8]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C264-20DC	D12	24-Lead (600-Mil) CerDIP	Commercial
	CY7C264-20PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C264-20WC	W12	24-Lead (600-Mil) Windowed CerDIP	
25	CY7C264-25DC	D12	24-Lead (600-Mil) CerDIP	Commercial
	CY7C264-25PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C264-25WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C264-25DMB	D12	24-Lead (600-Mil) CerDIP	Military
	CY7C264-25WMB	W12	24-Lead (600-Mil) Windowed CerDIP	
35	CY7C264-35DC	D12	24-Lead (600-Mil) CerDIP	Commercial
	CY7C264-35PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C264-35WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C264-35DMB	D12	24-Lead (600-Mil) CerDIP	Military
	CY7C264-35WMB	W12	24-Lead (600-Mil) Windowed CerDIP	
45	CY7C264-45DC	D12	24-Lead (600-Mil) CerDIP	Commercial
	CY7C264-45PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C264-45WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C264-45DMB	D12	24-Lead (600-Mil) CerDIP	Military
	CY7C264-45WMB	W12	24-Lead (600-Mil) Windowed CerDIP	
55	CY7C264-55DC	D12	24-Lead (600-Mil) CerDIP	Commercial
	CY7C264-55PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C264-55WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C264-55DMB	D12	24-Lead (600-Mil) CerDIP	Military
	CY7C264-55WMB	W12	24-Lead (600-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB} ^[9]	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{AA}	7, 8, 9, 10, 11
t _{ACS1} ^[10]	7, 8, 9, 10, 11
t _{ACS2} ^[9]	7, 8, 9, 10, 11

Notes:

9. 7C261 only.

10. 7C263 and 7C264 only.

Document #: 38-00005-J

Functional Description (continued)

If the \bar{E}/I pin is used for \overline{INIT} (asynchronous), then the outputs are permanently enabled. The initialize function is useful during power-up and time-out sequences, and can facilitate implementation of other sophisticated functions such as a built-in “jump start” address. When activated, the initialize control input causes the contents of a user programmed 8193rd 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combina-

tion of 1's and 0's into the register. In the unprogrammed state, activating \overline{INIT} will generate a register clear (all outputs LOW). If all the bits of the initialize word are programmed to be a 1, activating \overline{INIT} performs a register preset (all outputs HIGH).

Applying a LOW to the \overline{INIT} input causes an immediate load of the programmed initialize word into the pipeline register and onto the outputs. The \overline{INIT} LOW disables clock and must return HIGH to enable clock independent of all other inputs, including the clock.

Selection Guides

		7C265-15	7C265-25	7C265-40	7C265-50
Minimum Address Set-Up Time (ns)		15	25	40	50
Maximum Clock to Output (ns)		12	15	20	25
Maximum Operating Current (mA)	Com'l	120	120	100	80
	Mil	140	140		120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Ambient Temperature with
 Power Applied -55°C to $+125^{\circ}\text{C}$
 Supply Voltage to Ground Potential -0.5V to $+7.0\text{V}$
 DC Voltage Applied to Outputs
 in High Z State -0.5V to $+7.0\text{V}$
 DC Input Voltage -3.0V to $+7.0\text{V}$
 DC Program Voltage 13.0V
 UV Exposure 7258 Wsec/cm^2
 Static Discharge Voltage $>2001\text{V}$
 (per MIL-STD-883, Method 3015)

Latch-Up Current $>200\text{ mA}$

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 10\%$
Industrial ^[1]	-40°C to $+85^{\circ}\text{C}$	$5\text{V} \pm 10\%$
Military ^[2]	-55°C to $+125^{\circ}\text{C}$	$5\text{V} \pm 10\%$

Notes:

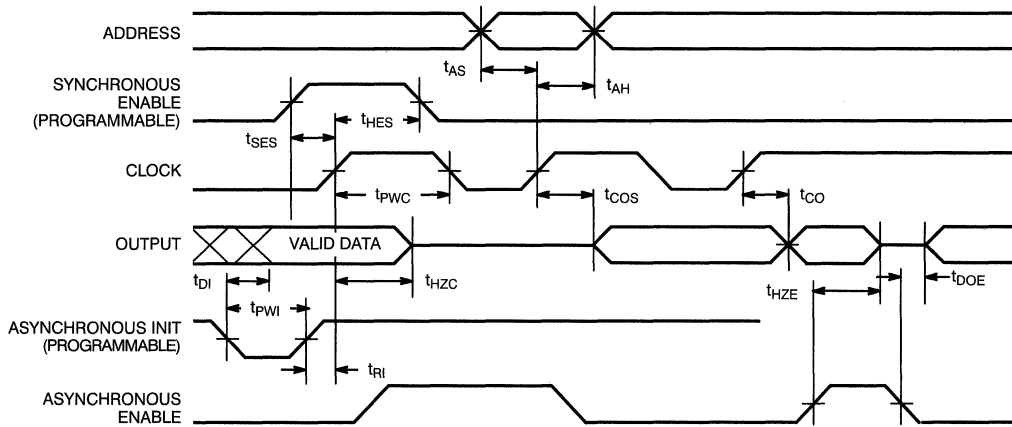
- Contact a Cypress representative for industrial temperature range specifications.
- T_A is the “instant on” case temperature.

Electrical Characteristics Over the Operating Range^[3]

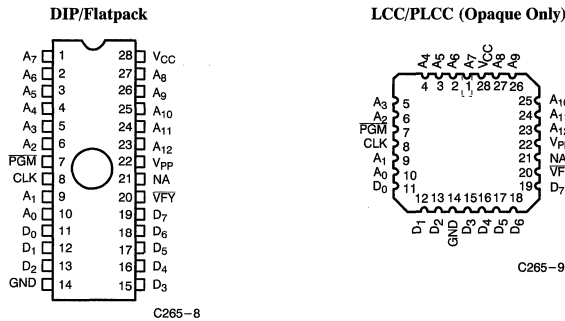
Parameter	Description	Test Conditions	7C265-15, 25		7C265-40		7C265-50		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -2.0\text{ mA}$	2.4						V
		$V_{CC} = \text{Min.}, I_{OH} = -4.0\text{ mA}$			2.4		2.4		
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0\text{ mA}$	Com'l	0.4					V
		$V_{CC} = \text{Min.}, I_{OL} = 12.0\text{ mA}$				0.4	0.4		
		$V_{CC} = \text{Min.}, I_{OL} = 6.0\text{ mA}$	Mil	0.4					
		$V_{CC} = \text{Min.}, I_{OL} = 8.0\text{ mA}$					0.4		
V_{IH}	Input HIGH Voltage		2.0		2.0		2.0	V	
V_{IL}	Input LOW Voltage			0.8		0.8		0.8	V
I_{IX}	Input Load Current	$GND \leq V_{IN} \leq V_{CC}$	-10	+10	-10	+10	-10	+10	μA
I_{OZ}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$, Output Disabled	-40	+40	-40	+40	-40	+40	μA
$I_{OS}^{[4]}$	Output Short Circuit Current	$V_{CC} = \text{Max.}, V_{OUT} = GND$		90		90		90	mA
I_{CC}	V_{CC} Operating Supply Current	Com'l		120		100		80	mA
		Mil		140			120		
V_{PP}	Programming Supply Voltage		12	13	12	13	12	13	V
I_{PP}	Programming Supply Current			50		50		50	mA

Switching Characteristics Over the Operating Range^[3, 5]

Parameter	Description	7C265-15		7C265-25		7C265-40		7C265-50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AS}	Address Set-Up to Clock	15		25		40		50		ns
t_{HA}	Address Hold from Clock	0		0		0		0		ns
t_{CO}	Clock to Output Valid		12		15		20		25	ns
t_{PWC}	Clock Pulse Width	12		15		15		20		ns
t_{SES}	\overline{E}_S Set-Up to Clock (Sync. Enable Only)	12		15		15		15		ns
t_{HES}	\overline{E}_S Hold from Clock	5		5		5		5		ns
t_{DI}	\overline{INIT} to Output Valid		15		18		25		35	ns
t_{RI}	\overline{INIT} Recovery to Clock	12		15		20		25		ns
t_{PWI}	\overline{INIT} Pulse Width	12		15		25		35		ns
t_{COS}	Output Valid from Clock (Sync. Mode)		12		15		20		25	ns
t_{HZC}	Output Inactive from Clock (Sync. Mode)		12		15		20		25	ns
t_{DOE}	Output Valid from \overline{E} LOW (Async. Mode)		12		15		20		25	ns
t_{HZE}	Output Inactive from \overline{E} HIGH (Async. Mode)		12		15		20		25	ns

Switching Waveform


C265-7

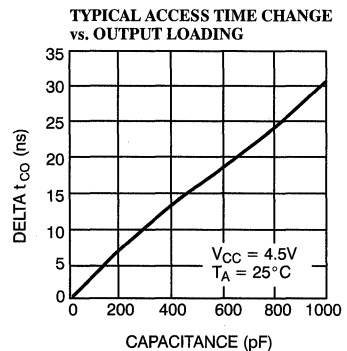
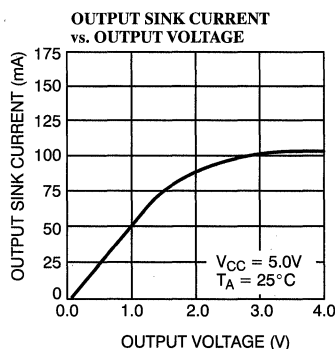
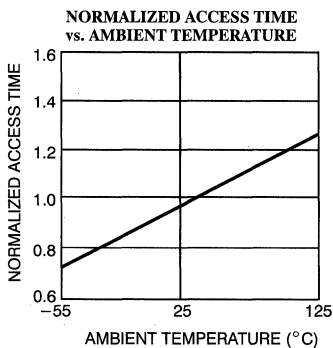
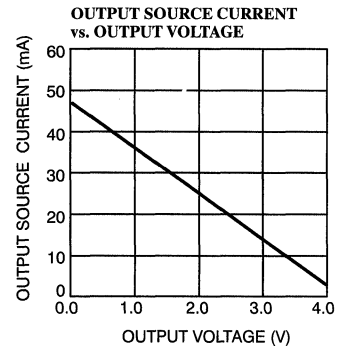
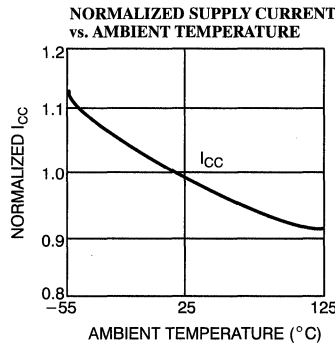
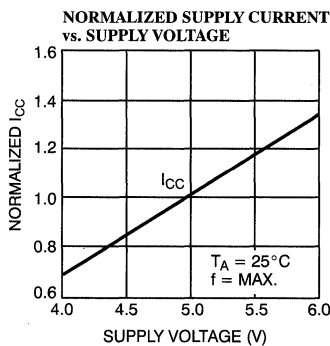

Figure 1. Programming Pinout

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed program-

ming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Typical DC and AC Characteristics



Ordering Information^[6]

Speed (ns)	I _{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
40	100	CY7C265-40JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C265-40PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C265-40WC	W22	28-Lead (300-Mil) Windowed CerDIP	
50	80	CY7C265-50JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C265-50PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C265-50WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	120	CY7C265-50DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C265-50LMB	L64	28-Square Leadless Chip Carrier	
		CY7C265-50QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C265-50WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{Ix}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{AS}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{CO}	7, 8, 9, 10, 11
t _{pw}	7, 8, 9, 10, 11
t _{SES}	7, 8, 9, 10, 11
t _{HES}	7, 8, 9, 10, 11
t _{COS}	7, 8, 9, 10, 11

Document #: 38-00084-E

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 28 to Pin 14)	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-3.0V to +7.0V
DC Program Voltage	13.0V

Static Discharge Voltage	> 2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	> 200 mA
UV Exposure	7258 Wsec/cm ²

Operating Range

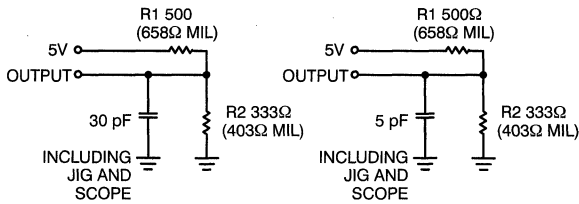
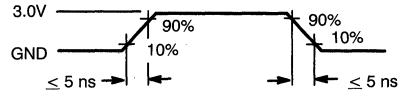
Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial ^[1]	-40°C to +85°C	5V ± 10%
Military ^[2]	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3, 4]

Parameter	Description	Test Conditions	7C266-20		7C266-25		Unit	
			Min.	Max.	Min.	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -2.0 mA	Com'l	2.4		2.4		V
			Mil			2.4		
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA	Com'l		0.4		0.4	V
		V _{CC} = Min., I _{OL} = 6.0 mA	Mil				0.4	
V _{IH}	Input HIGH Voltage			2.0		2.0		V
V _{IL}	Input LOW Voltage				0.8		0.8	V
I _{IX}	Input Current	GND ≤ V _{IN} ≤ V _{CC}		-10	+10	-10	+10	µA
V _{CD}	Input Diode Clamp Voltage		Note 4					
I _{OZ}	Output Leakage Current	V _{OL} ≤ V _{OUT} ≤ V _{OH} , Output Disabled		-40	+40	-40	+40	µA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND		-20	-90	-20	-90	mA
I _{CC}	Power Supply Current	V _{CC} = Max., V _{IN} = 2.0V, I _{OUT} = 0 mA	Com'l		120		120	mA
			Mil				140	
I _{SB}	Standby Supply Current	Chip Enable Inactive, CE ≥ V _{IH} , I _{OUT} = 0 mA	Com'l		15		15	mA
			Mil				15	

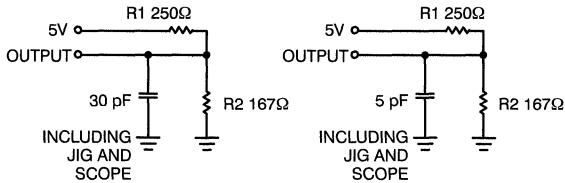
Notes:

- Contact a Cypress representative regarding industrial temperature range specification.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms
Test Load for -20 through -25 speeds

(a) Normal Load
(b) High Z Load


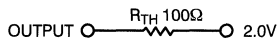
C266-5

Equivalent to: THEVENIN EQUIVALENT

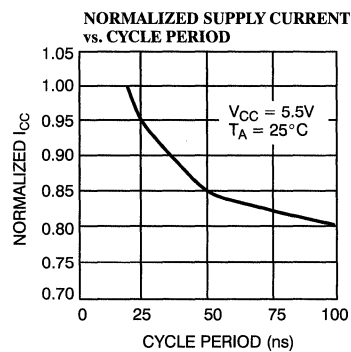
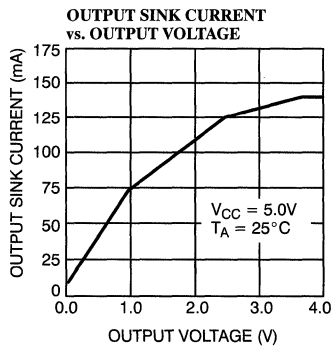
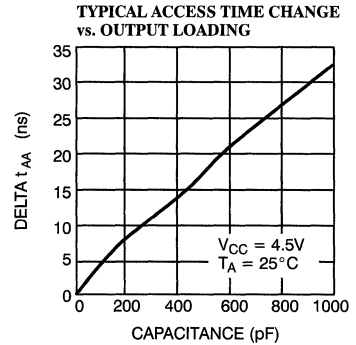
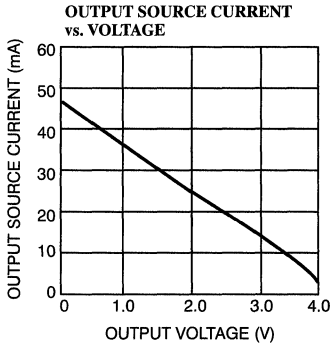
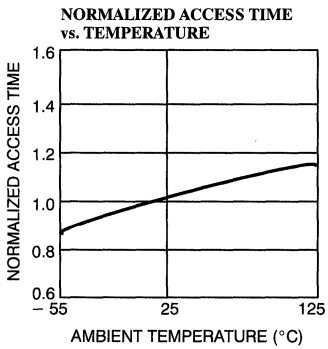
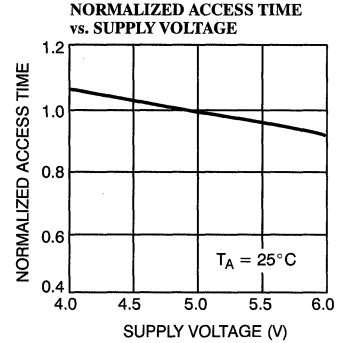
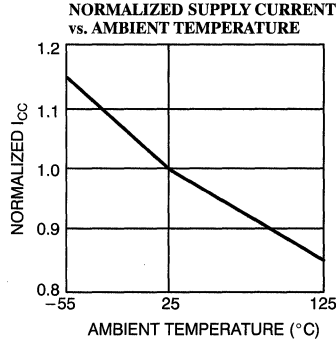
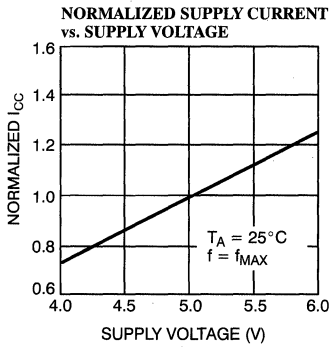

Test Load for -35 through -55 speeds

(c) Normal Load
(d) High Z Load

C266-6

Equivalent to: THEVENIN EQUIVALENT


Switching Characteristics Over the Operating Range^[2, 3, 5]

Parameter	Description	7C266-20		7C266-25		7C266-35		7C266-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		20		25		35		45	ns
t_{HZCE}	Chip Enable Inactive to High Z		25		30		40		45	ns
t_{HZOE}	Output Enable Inactive to High Z		12		12		20		25	ns
t_{AOE}	Output Enable Active to Output Valid		12		12		20		25	ns
t_{ACE}	Chip Enable Active to Output Valid		25		30		40		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{PU}	Chip Enable Active to Power-Up		25		30		40		45	ns
t_{PD}	Chip Enable Inactive to Power-Down		25		30		40		45	ns

Typical DC and AC Characteristics


8K x 8 Registered Diagnostic PROM

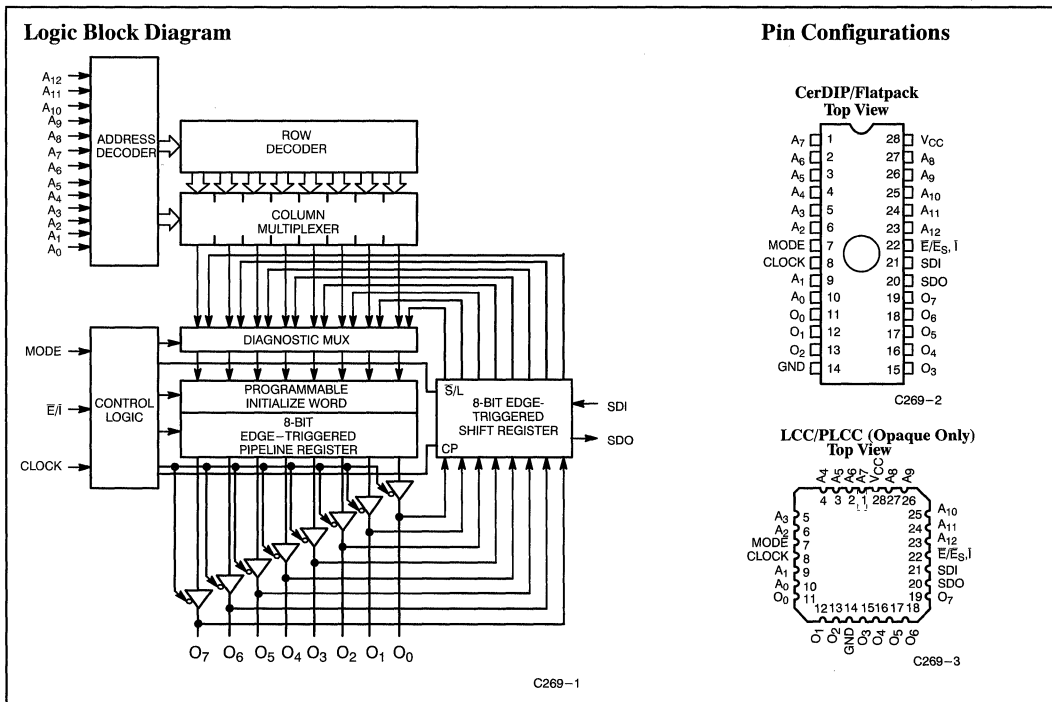
Features

- CMOS for optimum speed/power
- High speed (commercial and military)
 - 15-ns address set-up
 - 12-ns clock to output
- Low power
 - 660 mW (commercial)
 - 770 mW (military)
- On-chip edge-triggered registers
 - Ideal for pipelined microprogrammed systems

- On-chip diagnostic shift register
 - For serial observability and controllability of the output register
- EPROM technology
 - 100% programmable
 - Reprogrammable (7C269W)
- 5V ± 10% V_{CC}, commercial and military
- Capable of withstanding >2001V static discharge
- Slim 300-mil, 28-pin plastic or hermetic DIP

Functional Description

The CY7C269 is a 8K x 8 registered diagnostic PROM. It is organized as 8,192 words by 8 bits wide, and has both a pipeline output register and an onboard diagnostic shift register. The device features a programmable initialize byte that may be loaded into the pipeline register with the initialize signal. The programmable initialize byte is the 8,193rd byte in the PROM, and may be programmed to any desired value.



Selection Guide

	7C269-15	7C269-25	7C269-40	7C269-50
Minimum Address Set-Up Time (ns)	15	25	40	50
Maximum Clock to Output (ns)	12	15	20	25
Maximum Operating Current (mA)	Commercial	120	100	80
	Military	140	140	120

Electrical Characteristics Over the Operating Range^[3, 4]

Parameter	Description	Test Conditions	7C269-15, 25		7C269-40		7C269-50		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -2.0 mA	2.4						V
		V _{CC} = Min., I _{OH} = -4.0 mA			2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA	Com'l	0.4					V
		V _{CC} = Min., I _{OL} = 6.0 mA	Mil	0.4					
		V _{CC} = Min., I _{OL} = 12.0 mA	Com'l			0.4		0.4	V
		V _{CC} = Min., I _{OL} = 8.0 mA	Mil			0.4		0.4	
V _{IH}	Input HIGH Voltage		2.0		2.0		2.0		V
V _{IL}	Input LOW Voltage			0.8		0.8		0.8	V
I _{Ix}	Input Load Current	GND ≤ V _{IN} ≤ V _{CC}	-10	+10	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled	-40	+40	-40	+40	-40	+40	μA
I _{OS} ^[5]	Output Short Circuit Current			90		90		90	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	120		100		80	mA
			Mil	140				120	
V _{PP}	Programming Supply Voltage		12	13	12	13	12	13	V
I _{PP}	Programming Supply Current			50		50		50	mA
V _{IHP}	Input HIGH Programming Voltage		3.0		3.0		3.0		V
V _{ILP}	Input LOW Programming Voltage			0.4		0.4		0.4	V

Capacitance^[4, 6]

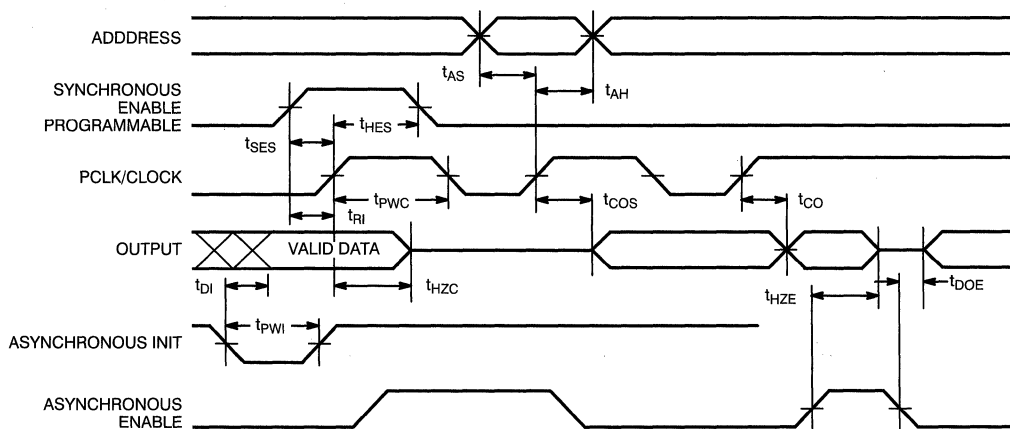
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

- See the last page of this specification for Group A subgroup testing information.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- See Introduction to CMOS PROMs in this Data Book for general information on testing.
- Tested initially and after any design or process changes that may affect these parameters.

Diagnostic Mode Switching Characteristics Over the Operating Range^[3, 4]

Parameter	Description		7C269-15		7C269-25		7C269-40,50		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{SSDI}	Set-Up SDI to Clock	Com'l	20		25		30		ns
		Mil	25		30		35		
t _{HSDI}	SDI Hold from Clock	Com'l	0		0		0		ns
		Mil	0		0		0		
t _{DSDO}	SDO Delay from Clock	Com'l		20		25		30	ns
		Mil		25		30		40	
t _{DCL}	Minimum Clock LOW	Com'l	20		25		25		ns
		Mil	25		25		25		
t _{DCH}	Minimum Clock HIGH	Com'l	20		25		25		ns
		Mil	25		25		25		
t _{SM}	Set-Up to Mode Change	Com'l	20		25		25		ns
		Mil	25		30		30		
t _{HM}	Hold from Mode Change	Com'l	0		0		0		ns
		Mil	0		0		0		
t _{MS}	Mode to SDO	Com'l		20		25		25	ns
		Mil		25		30		30	
t _{SS}	SDI to SDO	Com'l		30		40		40	ns
		Mil		35		40		45	
t _{SO}	Data Set-Up to DCLK	Com'l	20		25		25		ns
		Mil	25		30		30		
t _{HO}	Data Hold from DCLK	Com'l	10		10		10		ns
		Mil	13		13		15		

Switching Waveforms^[3, 4]
Pipeline Operation (Mode = 0)


Bit Map Data

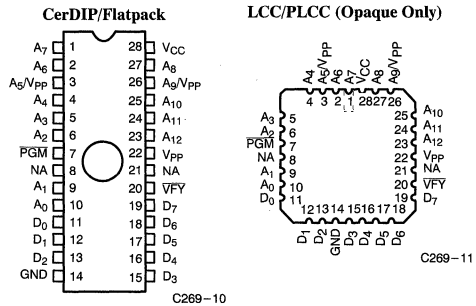
Programmer Address (Hex.)		RAM Data
Decimal	Hex	Contents
0	0	Data
.	.	.
8191	1FFF	Data
8192	2000	Init Byte
8193	2001	Control Byte

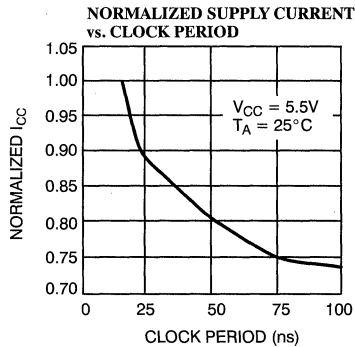
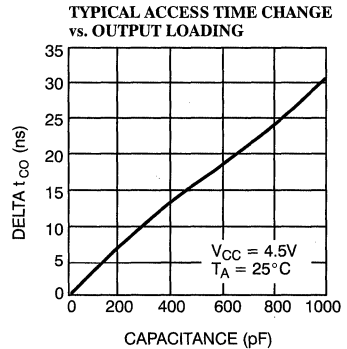
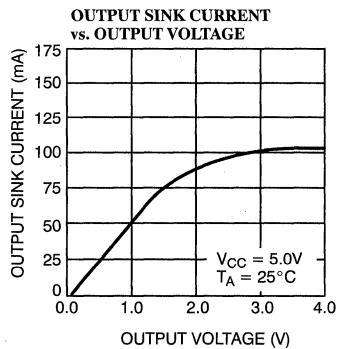
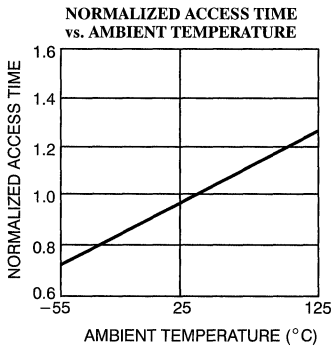
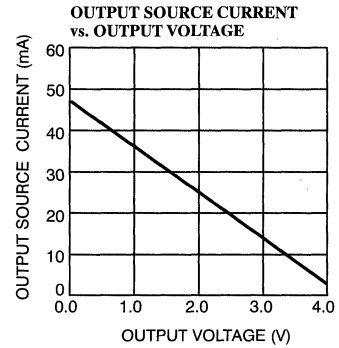
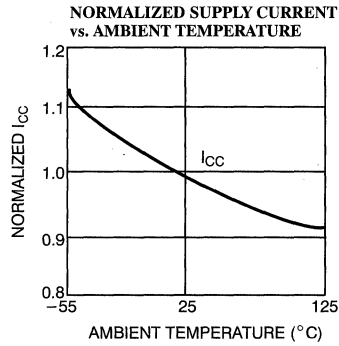
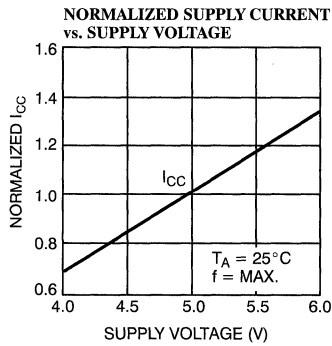
Control Byte

- 00 Asynchronous output enable (default condition)
- 01 Synchronous output enable
- 02 Asynchronous initialize

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.


Figure 1. Programming Pinouts

Typical DC and AC Characteristics


MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{Ix}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t _{AS}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{CO}	7, 8, 9, 10, 11
t _{PW}	7, 8, 9, 10, 11
t _{SES}	7, 8, 9, 10, 11
t _{HES}	7, 8, 9, 10, 11
t _{COS}	7, 8, 9, 10, 11

Diagnostic Mode Switching Characteristics

Parameters	Subgroups
t _{SSDI}	7, 8, 9, 10, 11
t _{HSDI}	7, 8, 9, 10, 11
t _{DSDO}	7, 8, 9, 10, 11
t _{DCL}	7, 8, 9, 10, 11
t _{DCH}	7, 8, 9, 10, 11
t _{HM}	7, 8, 9, 10, 11
t _{MS}	7, 8, 9, 10, 11
t _{SS}	7, 8, 9, 10, 11

Document #: 38-00069-G



32K x 8 Power-Switched and Reprogrammable PROM

Features

- CMOS for optimum speed/power
- Windowed for reprogrammability
- High speed
 - 25 ns (commercial)
 - 35 ns (military)
- Low power
 - 275 mW (commercial)
 - 330 mW (military)
- Super low standby power
 - Less than 85 mW when deselected
- EPROM technology 100% programmable
- Slim 300-mil package
- Direct replacement for bipolar PROMs

- Capable of withstanding >4001V static discharge

Functional Description

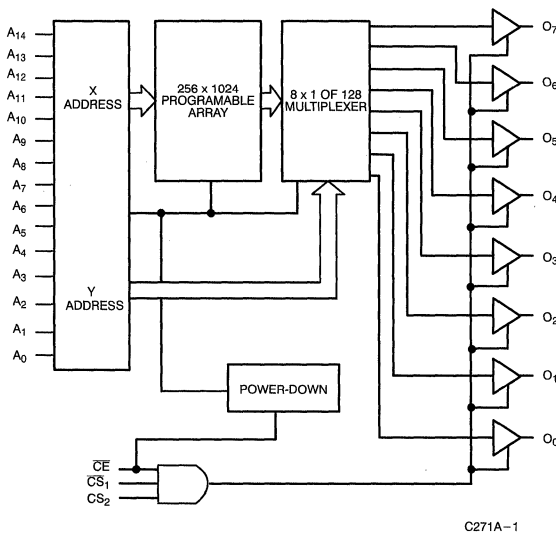
The CY7C271A is a high-performance 32,768-word by 8-bit CMOS PROM. When disabled (\overline{CE} HIGH), the 7C271A automatically powers down into a low-power stand-by mode. The CY7C271A is packaged in the 300-mil slim package and is available in a cerDIP package equipped with an erasure window to provide for reprogrammability. When exposed to UV light, the PROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C271A offers the advantages of lower power, superior performance, and

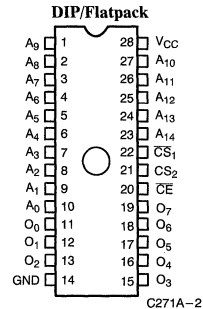
programming yield. The EPROM cell requires only 12.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

Reading the 7C271A is accomplished by placing active LOW signals on \overline{CS}_1 and \overline{CE} , and an active HIGH on CS_2 . The contents of the memory location addressed by the address lines ($A_0 - A_{14}$) will become available on the output lines ($O_0 - O_7$).

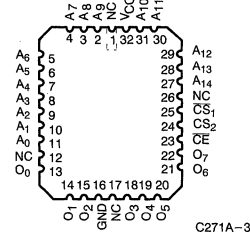
Logic Block Diagram



Pin Configurations

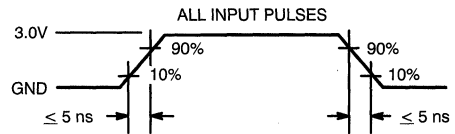
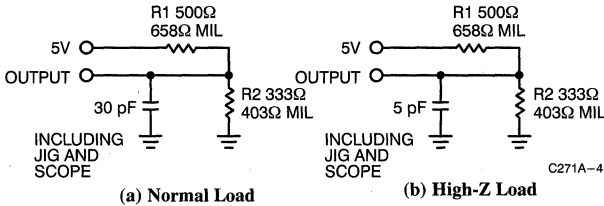


LCC/PLCC (Opaque Only)



Selection Guide

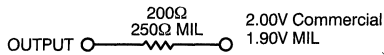
	7C271A-25	7C271A-30	7C271A-35	7C271A-45	7C271A-55
Maximum Access Time (ns)	25	30	35	45	55
Maximum Operating Current (mA)	Com'l	75	75	50	50
	Military			85	60
Standby Current (mA)	Com'l	15	15	15	15
	Military			25	25

AC Test Loads and Waveforms


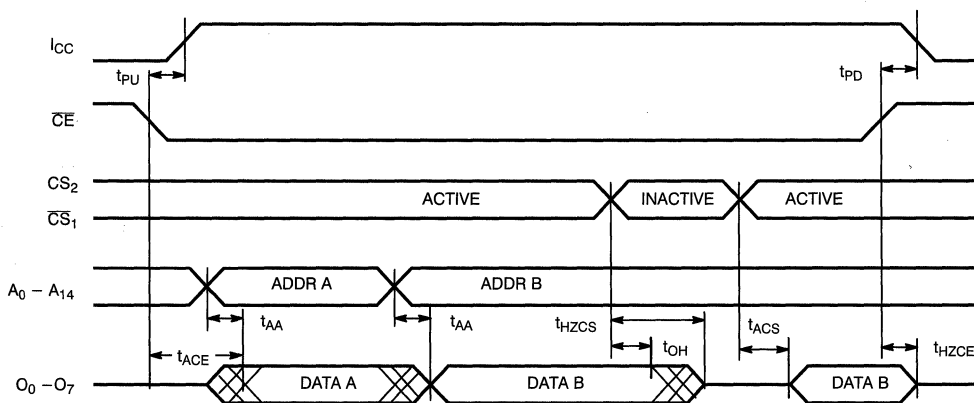
C271A-4

C271A-5

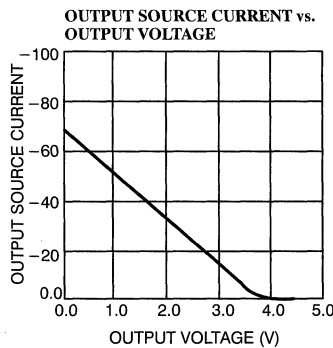
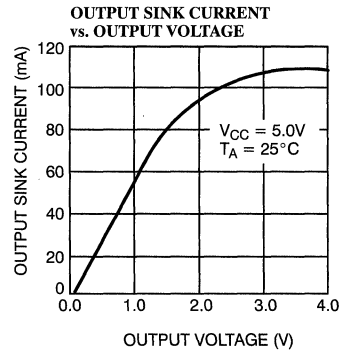
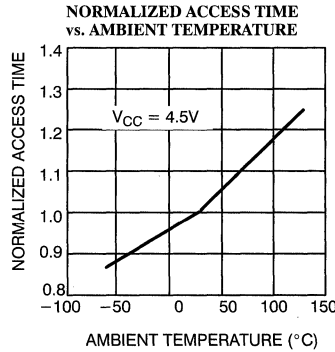
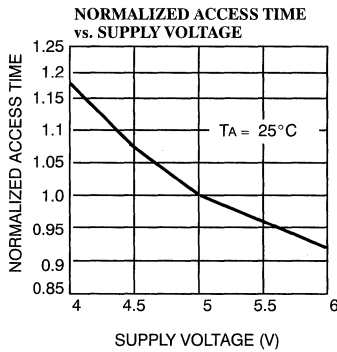
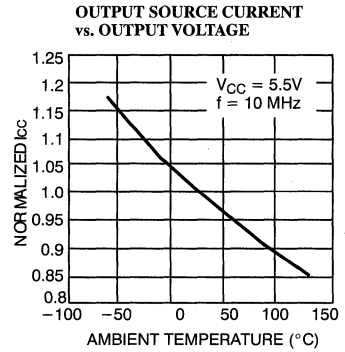
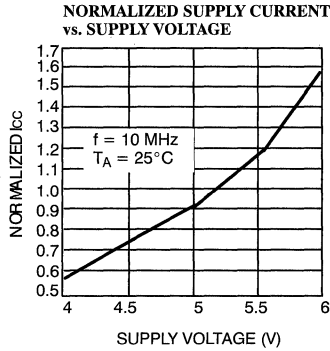
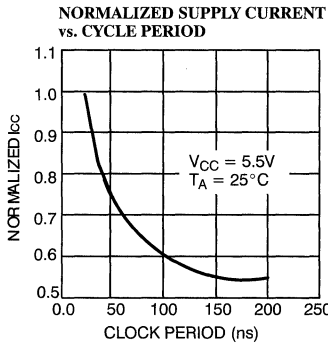
Equivalent to: THÉVENIN EQUIVALENT


Switching Characteristics Over the Operating Range^[3,4]

Parameter	Description	7C271A-25		7C271A-30		7C271A-35		7C271A-45		7C271A-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		25		30		35		45		55	ns
t_{ACS}	\overline{CS}_1/CS_2 Active to Output Valid		12		15		15		15		20	ns
t_{ACE}	\overline{CE} Active to Output Valid		30		35		35		45		55	ns
t_{HZCS}	\overline{CS}_1/CS_2 Inactive to High Z		12		15		15		15		20	ns
t_{HZCE}	\overline{CE} Inactive to High Z		12		15		15		15		20	ns
t_{PU}	\overline{CE} Active to Power-Up	0		0		0		0		0		ns
t_{PD}	\overline{CE} Inactive to Power-Down		30		35		40		40		50	ns
t_{OH}	Output Data Hold	0		0		0		0		0		ns

Switching Waveform


C271A-6

Typical DC and AC Characteristics


MILITARY SPECIFICATIONS
Group A Subgroup Testing**DC Characteristics**

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{AA}	7, 8, 9, 10, 11
t _{ACS}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11

Document #: 38-00424

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	- 65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-3.0V to +7.0V
DC Program Voltage	13.0V
UV Erasure	7258 Wsec/cm ²

Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial ^[1]	-40°C to +85°C	5V ±10%
Military ^[2]	-55°C to +125°C	5V ±10%

Electrical Characteristics^[3, 4]

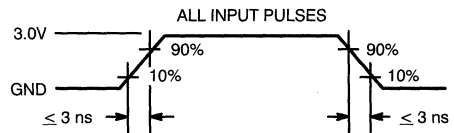
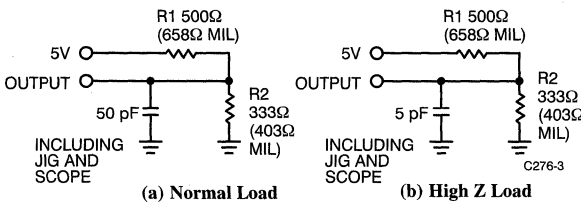
Parameter	Description	Test Conditions	CY7C276-25 CY7C276-30 CY7C276-35		Unit
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -2.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA (6.0 mA Mil)		0.4	V
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs	2.0	V _{CC}	V
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs	-3.0	0.8	V
I _{Ix}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}	-10	+10	µA
V _{CD}	Input Clamp Diode Voltage		Note 3		µA
I _{OZ}	Output Leakage Current	V _{CC} = Max., V _{OL} ≤ V _{OUT} ≤ V _{OH} , Output Disabled	-40	+40	µA
I _{OS}	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = 0.0V ^[5]	-20	-90	mA
I _{CC}	Power Supply Current	V _{CC} = Max., I _{OUT} = 0.0 mA	Com'l	175	mA
			Military	200	mA

Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

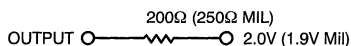
Notes:

- Contact a Cypress representative for industrial temperature range specifications.
- T_A is the "instant on" case temperature
- See Introduction to CMOS PROMs in this Data Book for general information on testing.
- See the last page of this specification for Group A subgroup testing information.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms


C276-4

Equivalent to: THÉVENIN EQUIVALENT



Architecture Configuration Bits

The CY7C276 has four user-programmable options in addition to the reprogrammable data array. For detailed programming information contact your local Cypress representative.

The programmable options determine the active polarity for the three chip selects (CS₂ – CS₀) and OE. When these control bits are programmed with a 0 the inputs are active LOW. When these control bits are programmed with a 1 the inputs are active HIGH.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Control Word for Architecture Configuration

Control Option	Control Word		Function
	Bit	Programmed Level	
OE	D ₀	0=Default 1=Programmed	OE Active LOW OE Active HIGH
CS ₀	D ₁₂	0=Default 1=Programmed	CS ₀ Active LOW CS ₀ Active HIGH
CS ₁	D ₁₃	0=Default 1=Programmed	CS ₁ Active LOW CS ₁ Active HIGH
CS ₂	D ₁₄	0=Default 1=Programmed	CS ₂ Active LOW CS ₂ Active HIGH

Bit Map

Programmer Address (Hex)	RAM Data
0000	Data
.	.
.	.
3FFF	Data
4000	Control Word

Table 2. Program Mode Table

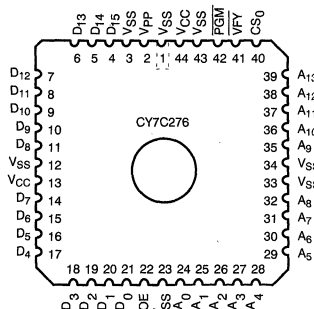
Mode	V _{PP}	PGM	VFY	D ₀ – D ₁₅
Program Inhibit	V _{PP}	V _{IHP}	V _{IHP}	High Z
Program Enable	V _{PP}	V _{ILP}	V _{IHP}	Data
Program Verify	V _{PP}	V _{IHP}	V _{ILP}	Data

Control Word (4000H)

D₁₅ D₀
X CS₂ CS₁ CS₀ X X X X X X X X 1 X X OE

Table 3. Configuration Mode Table

Mode	V _{PP}	PGM	VFY	A ₂	D ₀ – D ₁₅
Program Inhibit	V _{PP}	V _{IHP}	V _{IHP}	V _{PP}	High Z
Program Control Word	V _{PP}	V _{ILP}	V _{IHP}	V _{PP}	Control Word
Verify Control Word	V _{PP}	V _{IHP}	V _{ILP}	V _{PP}	Control Word



C276-7

Figure 1. Programming Pinout

Ordering Information^[7]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C276-25HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C276-25JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C276-25HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C276-25QMB	Q67	44-Pin Windowed Leadless Chip Carrier	
30	CY7C276-30HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C276-30JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C276-30HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C276-30QMB	Q67	44-Pin Windowed Leadless Chip Carrier	
35	CY7C276-35HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C276-35JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C276-35HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C276-35QMB	Q67	44-Pin Windowed Leadless Chip Carrier	

Note:

7. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

**MILITARY SPECIFICATIONS
Group A Subgroup Testing**
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{AA}	7, 8, 9, 10, 11
t _{CSOV}	7, 8, 9, 10, 11
t _{OEV}	7, 8, 9, 10, 11

Document #: 38-00183-D

Functional Description (continued)

The CY7C277 offers the advantages of low power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

On the 7C277, the outputs are pipelined through a master-slave register. On the rising edge of CP, data is loaded into the 8-bit edge

triggered output register. The $\overline{E}/\overline{E}_S$ input provides a programmable bit to select between asynchronous and synchronous operation. The default condition is asynchronous. When the asynchronous mode is selected, the $\overline{E}/\overline{E}_S$ pin operates as an asynchronous output enable. If the synchronous mode is selected, the $\overline{E}/\overline{E}_S$ pin is sampled on the rising edge of CP to enable and disable the outputs. The 7C277 also provides a programmable bit to enable the Address Latch input. If this bit is not programmed, the device will ignore the ALE pin and the address will enter the device asynchronously. If the ALE function is selected, the address enters the PROM while the ALE pin is active, and is captured when ALE is deasserted. The user may define the polarity of the ALE signal, with the default being active HIGH.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12)	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-3.0V to +7.0V
DC Program Voltage (Pins 7, 18, 20)	13.0V

UV Erasure	7258 Wsec/cm ²
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial ^[1]	-40°C to +85°C	5V ±10%
Military ^[2]	-55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range^[3, 4]

Parameter	Description	Test Conditions	7C277-30		7C277-40, 50		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -2.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs	2.0	V _{CC}	2.0	V _{CC}	V
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		0.8		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}	-10	+10	-10	+10	μA
V _{CD}	Input Clamp Diode Voltage		Note 4				
I _{OZ}	Output Leakage Current	0 ≤ V _{OUT} ≤ V _{CC} , Output Disabled ^[5]	-40	+40	-40	+40	μA
I _{OS}	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = 0.0V ^[6]	-20	-90	-20	-90	mA
I _{CC}	Power Supply Current	V _{CC} = Max., $\overline{CS} \geq V_{IH}$ I _{OUT} = 0 mA	Commercial	120		120	mA
			Military			130	
V _{PP}	Programming Supply Voltage		12	13	12	13	V
I _{PP}	Programming Supply Current			50		50	mA
V _{IHP}	Input HIGH Programming Voltage		3.0		3.0		V
V _{ILP}	Input LOW Programming Voltage			0.4		0.4	V

Notes:

- Contact a Cypress representative for industrial temperature range specifications.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- See "Introduction to CMOS PROMs" in this Book for general information on testing.
- For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

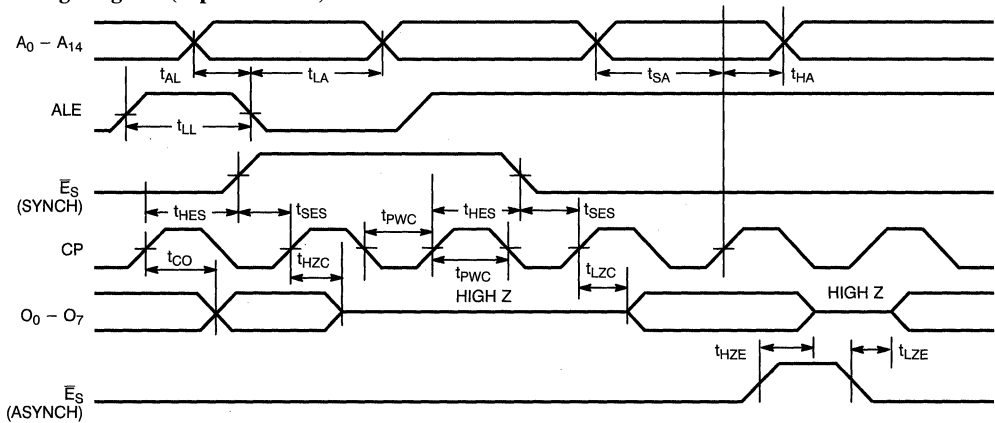
Architecture Configuration Bits

Architecture Bit	Architecture Verify D ₇ - D ₀		Function
ALE	D ₁	0 = DEFAULT	Input Transparent
		1 = PGMED	Input Latched
ALEP	D ₂	0 = DEFAULT	ALE = Active HIGH
		1 = PGMED	ALE = Active LOW
\bar{E}/\bar{E}_S	D ₀	0 = DEFAULT	Asynchronous Output Enable (\bar{E})
		1 = PGMED	Synchronous Output Enable (\bar{E}_S)

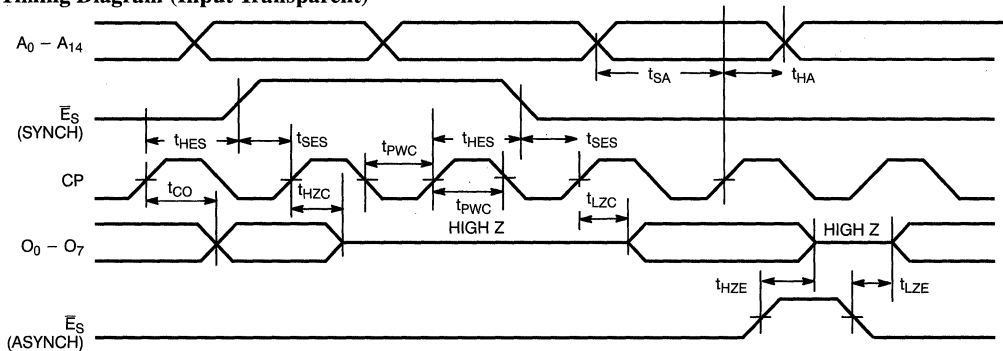
Bit Map

Programmer Address (Hex.)	RAM Data
0000	Data
⋮	⋮
7FFF	Data
8000	Control Byte

Architecture Byte (8000)
 D₇ D₆ D₅ D₄ D₃ D₂ D₁ D₀
 C₇ C₆ C₅ C₄ C₃ C₂ C₁ C₀

Timing Diagram (Input Latched)^[9]


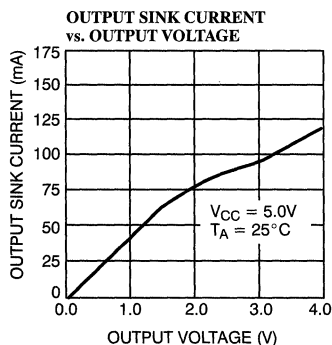
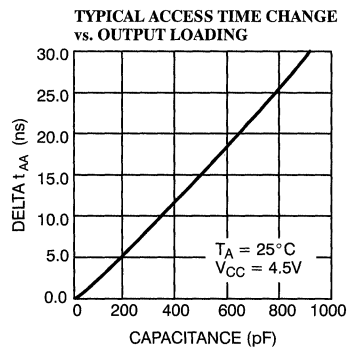
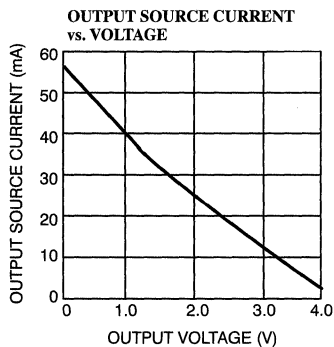
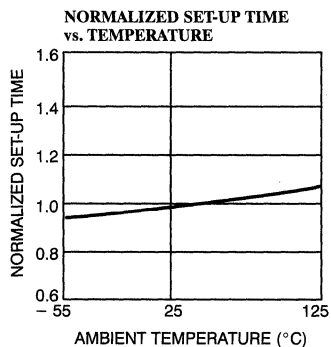
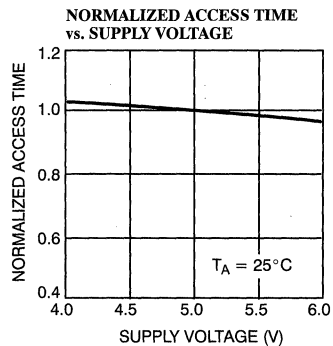
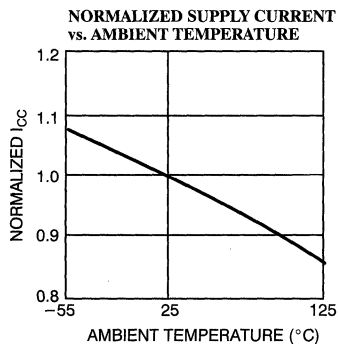
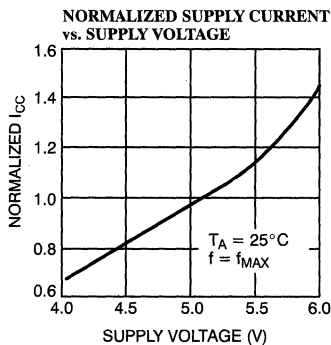
C277-6

Timing Diagram (Input Transparent)


C277-7

Note:

9. ALE is shown with positive polarity.

Typical DC and AC Characteristics




CY7C281A CY7C282A

1K x 8 PROM

Features

- CMOS for optimum speed/power
- High speed
 - 25 ns (commercial)
 - 30 ns (military)
- Low power
 - 495 mW (commercial)
 - 660 mW (military)
- EPROM technology 100% programmable
- Slim 300-mil or standard 600-mil DIP or 28-pin LCC
- 5V $\pm 10\%$ V_{CC}, commercial and military
- TTL-compatible I/O
- Direct replacement for bipolar PROMs

- Capable of withstanding >2001V static discharge

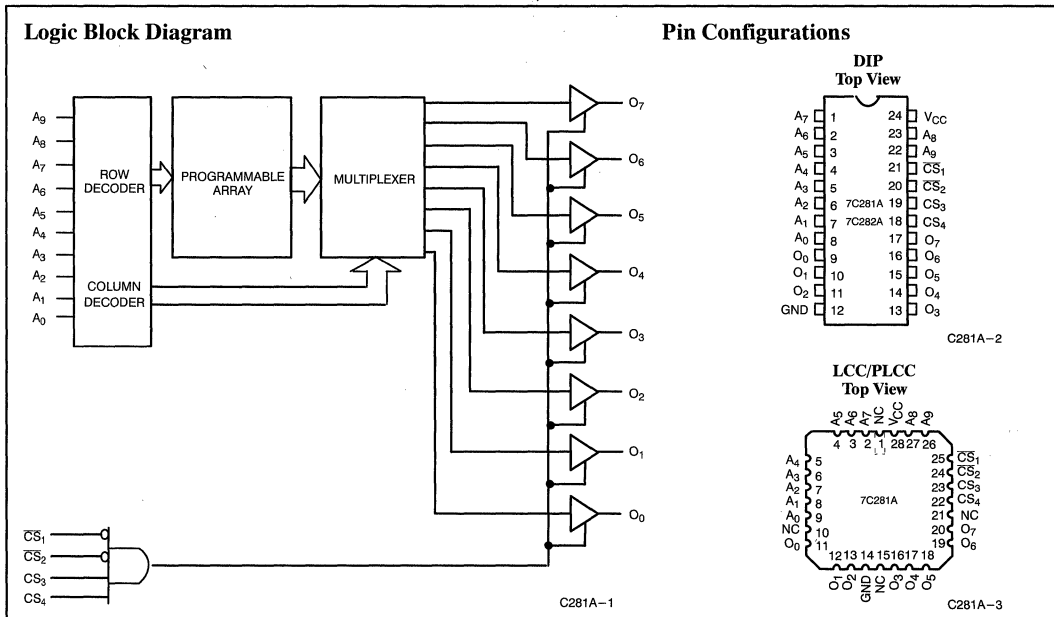
Functional Description

The CY7C281A and CY7C282A are high-performance 1024-word by 8-bit CMOS PROMs. They are functionally identical, but are packaged in 300-mil and 600-mil-wide packages respectively. The CY7C281A is also available in a 28-pin leadless chip carrier. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C281A and CY7C282A are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance, and programming

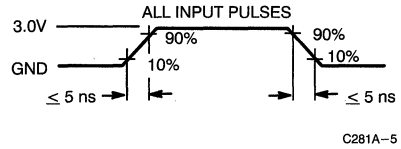
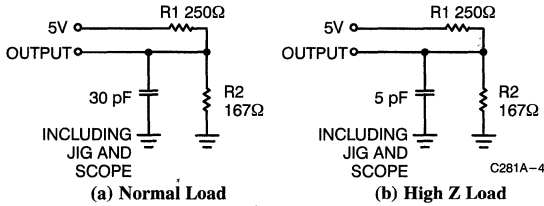
yield. The EPROM cell requires only 12.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on CS₁ and CS₂, and active HIGH signals on CS₃ and CS₄. The contents of the memory location addressed by the address lines (A₀ – A₉) will become available on the output lines (O₀ – O₇).

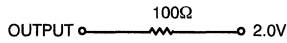


Selection Guide

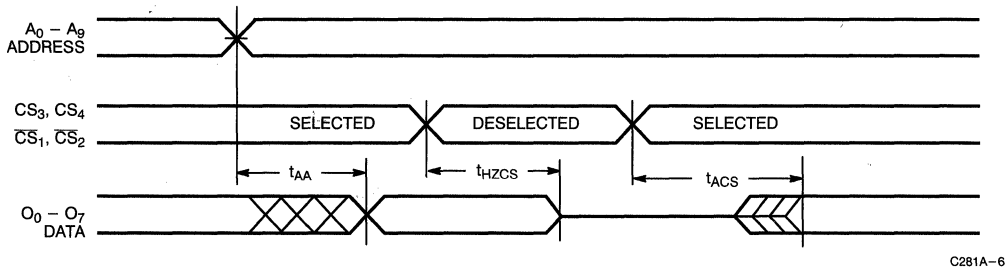
		7C281A-25 7C282A-25	7C281A-30 7C282A-30	7C281A-45 7C282A-45
Maximum Access Time (ns)		25	30	45
Maximum Operating Current (mA)	Commercial	100	100	90
	Military		120	120

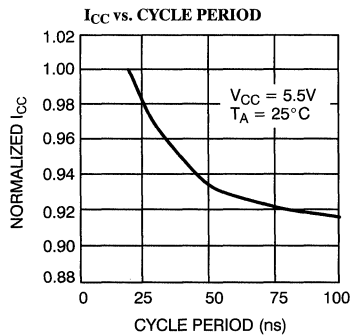
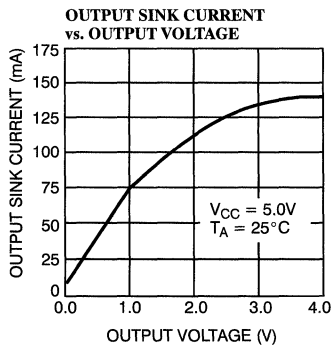
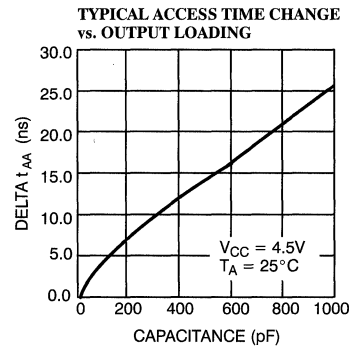
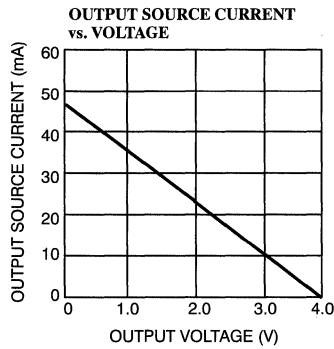
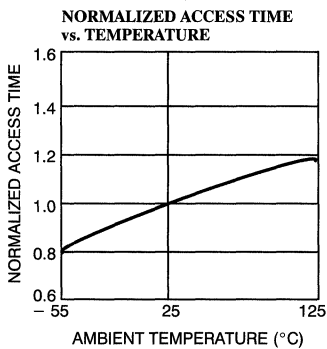
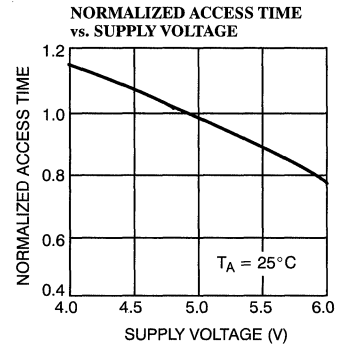
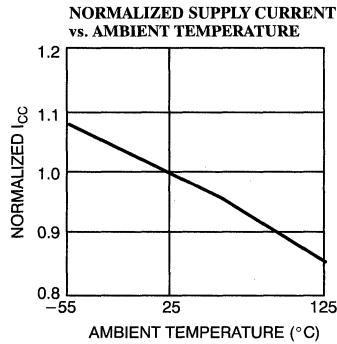
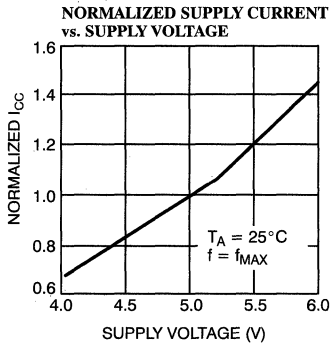
AC Test Loads and Waveforms^[4]


Equivalent to: THÉVENIN EQUIVALENT


Switching Characteristics Over the Operating Range^[2,4]

Parameter	Description	7C281A-25 7C282A-25		7C281A-30 7C282A-30		7C281A-45 7C282A-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		25		30		45	ns
t_{HZCS}	Chip Select Inactive to High Z		15		20		25	ns
t_{ACS}	Chip Select Active to Output Valid		15		20		25	ns

Switching Waveforms


Typical DC and AC Characteristics




64K x 8 Reprogrammable Registered PROM

Features

- CMOS for optimum speed/power
- Windowed for reprogrammability
- High speed
 - $t_{SA} = 45 \text{ ns}$
 - $t_{CO} = 15 \text{ ns}$
- Low power
 - 120 mA
- On-chip, edge-triggered output registers
- Programmable synchronous or asynchronous output enable
- EPROM technology, 100% programmable
- $5V \pm 10\% V_{CC}$, commercial and military
- TTL-compatible I/O

- Slim 300-mil package
- Capable of withstanding >2001V static discharge

Functional Description

The CY7C287 is a high-performance 64K x 8 CMOS PROM. The CY7C287 is equipped with an output register and an output enable that can be programmed to be synchronous (\bar{E}_S) or asynchronous (\bar{E}). It is available in a 28-pin, 300-mil package. The address set-up time is 45 ns and the time from clock HIGH to output valid is 15 ns.

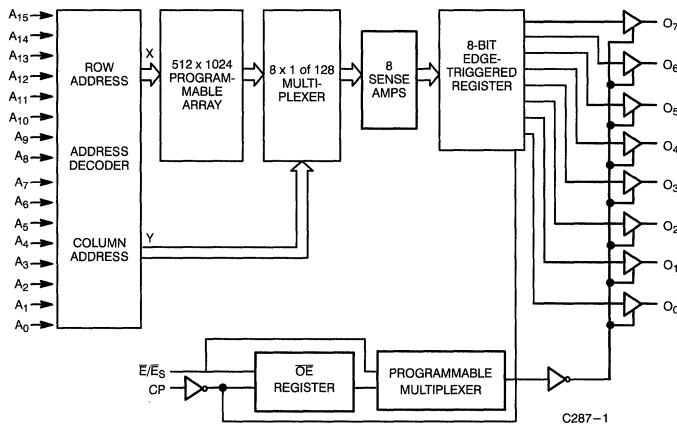
The CY7C287 is available in a cerDIP package equipped with an erasure window to provide reprogrammability. When exposed to UV light, the PROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating-gate

technology and byte-wide intelligent programming algorithms.

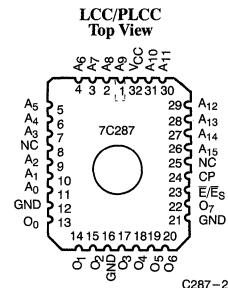
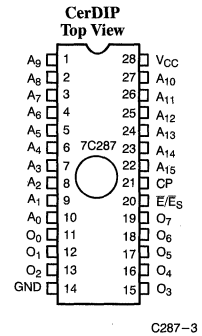
The CY7C287 offers the advantage of low power, superior performance, and programming yield. The EPROM cell requires only 12.5V for the supravoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested with each cell being programmed, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

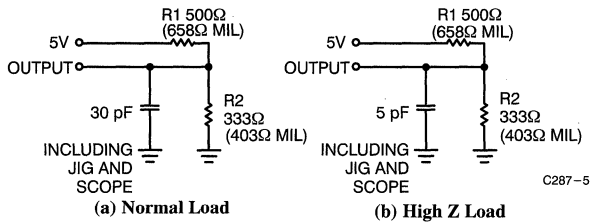
Reading the CY7C287 is accomplished by placing an active LOW signal on \bar{E}/\bar{E}_S . The contents of the memory location addressed by the address lines ($A_0 - A_{15}$) will become available on the output lines ($O_0 - O_7$) on the next rising of CP.

Logic Block Diagram

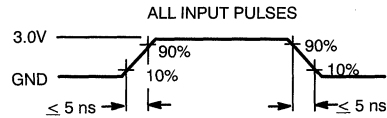


Pin Configurations



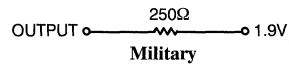
AC Test Loads and Waveform^[4]


C287-5



C287-4

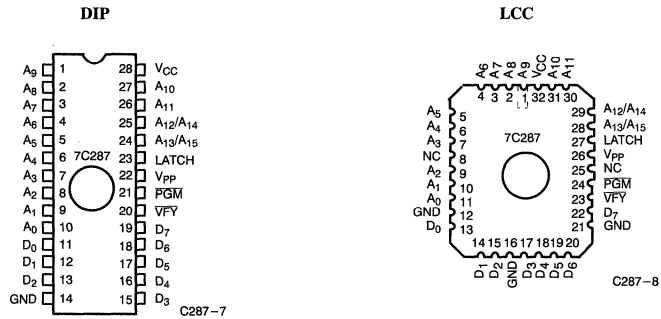
Equivalent to: THÉVENIN EQUIVALENT


Switching Characteristics Over the Operating Range^[3, 4]

Parameter	Description	7C287-45		7C287-55		7C287-65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{SA}	Address Set-Up to Clock HIGH	45		55		65		ns
t _{HA}	Address Hold from Clock HIGH	0		0		0		ns
t _{CO}	Clock HIGH to Output Valid		15		20		25	ns
t _{HZE}	Output High Z from \bar{E}		15		20		25	ns
t _{DOE}	Output Valid from \bar{E}		15		20		25	ns
t _{PWC}	Clock Pulse Width	15		20		25		ns
t _{SEs} ^[6]	\bar{E}_S Set-Up to Clock HIGH	12		15		18		ns
t _{HEs} ^[6]	\bar{E}_S Hold from Clock HIGH	5		8		10		ns
t _{HZC} ^[6]	Output High Z from CLK/ \bar{E}_S		20		25		30	ns
t _{COs} ^[6]	Output Valid from CLK/ \bar{E}_S		20		25		30	ns

Note:

 6. Parameters with synchronous \bar{E}_S option.


Figure 1. Programming Pinouts
Architecture Configuration Bits

Architecture Bit	Device	Architecture Verify D ₀		Function
\bar{E}/\bar{E}_S	7C287	D ₀	0 = Erased	Asynchronous Output Enable (Pin 20 = \bar{E})
			1 = PGMED	Synchronous Output Enable (Pin 20 = \bar{E}_S)

Bit Map

Programmer Address (Hex.)	RAM Data
0000	Data
·	·
FFFF	Data
10000	Control Byte

Architecture Byte (10000H)

 D₇ D₀
 C₇ C₆ C₅ C₄ C₃ C₂ C₁ C₀



CY7C291A CY7C292A/CY7C293A

2K x 8 Reprogrammable PROM

Features

- **Windowed for reprogrammability**
- **CMOS for optimum speed/power**
- **High speed**
 - 20 ns (commercial)
 - 25 ns (military)
- **Low power**
 - 660 mW (commercial and military)
- **Low standby power**
 - 220 mW (commercial and military)
- **EPROM technology 100% program-mable**
- **Slim 300-mil or standard 600-mil packaging available**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**

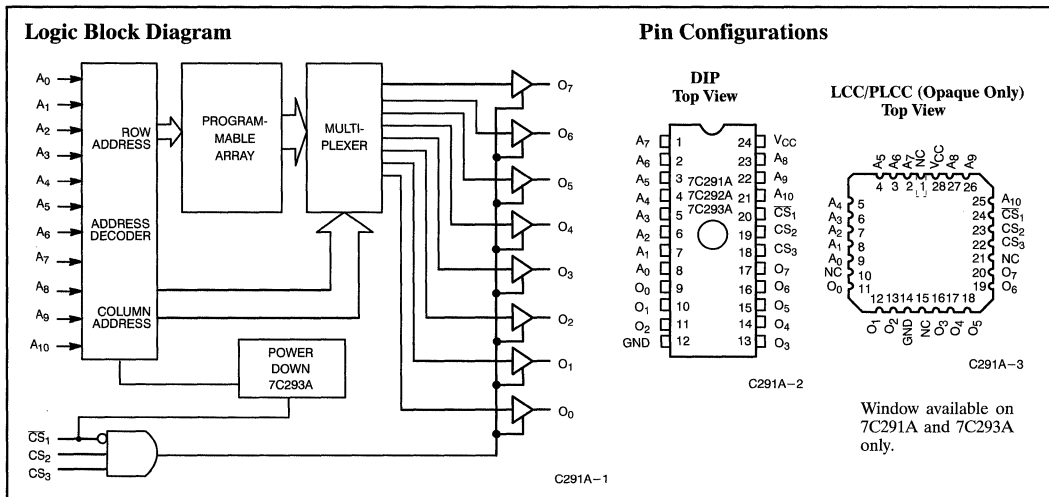
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2001V static discharge**

Functional Description

The CY7C291A, CY7C292A, and CY7C293A are high-performance 2K-word by 8-bit CMOS PROMs. They are functionally identical, but are packaged in 300-mil (7C291A, 7C293A) and 600-mil wide plastic and hermetic DIP packages (7C292A). The CY7C293A has an automatic power down feature which reduces the power consumption by over 70% when deselected. The 300-mil ceramic package may be equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C291A, CY7C292A, and CY7C293A are plug-in replacements for bipolar devices and offer the advantages of lower power, reprogrammability, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

A read is accomplished by placing an active LOW signal on CS₁, and active HIGH signals on CS₂ and CS₃. The contents of the memory location addressed by the address line (A₀ - A₁₀) will become available on the output lines (O₀ - O₇).



Selection Guide

		7C291A-20 7C292A-20 7C293A-20	7C291A-25 7C292A-25 7C293A-25 7C291AL-25 7C292AL-25 7C293AL-25	7C291A-35 7C292A-35 7C293A-35 7C291AL-35 7C292AL-35 7C293AL-35	7C291A-50 7C292A-50 7C293A-50 7C291AL-50 7C292AL-50 7C293AL-50
Maximum Access Time (ns)		20	25	35	50
Maximum Operating Current (mA)	Standard	Commercial	120	90	90
		Military		120	90
Standby Current (mA) 7C293A Only	L	Commercial	40	30	30
		Military		40	40

Electrical Characteristics Over the Operating Range^[3, 4] (continued)

Parameter	Description	Test Conditions	7C291AL-35, 50 7C292AL-35, 50 7C293AL-35, 50		7C291A-35, 50 7C292A-35, 50 7C293A-35, 50		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 16.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs	2.0		2.0		V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs		0.8		0.8	V
I _{IX}	Input Load Current	GND ≤ V _{IN} ≤ V _{CC}	-10	+10	-10	+10	μA
V _{CD}	Input Diode Clamp Voltage		Note 4				
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND	-20	-90	-20	-90	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., V _{IN} = 2.0V I _{OUT} = 0 mA	Commercial	60		90	mA
			Military			90	
I _{SB}	Standby Supply Current (7C293A Only)	V _{CC} = Max., CS ₁ = V _{IH}	Commercial	30		30	mA
			Military			40	
V _{PP}	Programming Supply Voltage		12	13	12	13	V
I _{PP}	Programming Supply Current			50		50	mA
V _{IHP}	Input HIGH Programming Voltage		3.0		3.0		V
V _{ILP}	Input LOW Programming Voltage			0.4		0.4	V

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase these PROMs. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity x exposure time) of 25 Wsec/cm². For an ultraviolet lamp with a 12 mW/cm² power rating, the exposure time would be approximately 35 minutes.

These PROMs need to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm² is the recommended maximum dosage.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode	Pin Function ^[7]					
	Read or Output Disable	A ₁₀ - A ₀	CS ₃	CS ₂	\overline{CS}_1	O ₇ - O ₀
	Other	A ₁₀ - A ₀	PGM	VFY	V _{PP}	D ₇ - D ₀
Read		A ₁₀ - A ₀	V _{IH}	V _{IH}	V _{IL}	O ₇ - O ₀
Output Disable ^[8]		A ₁₀ - A ₀	X	X	V _{IH}	High Z
Output Disable		A ₁₀ - A ₀	X	V _{IL}	X	High Z
Output Disable		A ₁₀ - A ₀	V _{IL}	X	X	High Z
Program		A ₁₀ - A ₀	V _{ILP}	V _{IHP}	V _{PP}	D ₇ - D ₀
Program Verify		A ₁₀ - A ₀	V _{IHP}	V _{ILP}	V _{PP}	O ₇ - O ₀
Program Inhibit		A ₁₀ - A ₀	V _{IHP}	V _{IHP}	V _{PP}	High Z
Intelligent Program		A ₁₀ - A ₀	V _{ILP}	V _{IHP}	V _{PP}	D ₇ - D ₀
Blank Check Zeros		A ₁₀ - A ₀	V _{IHP}	V _{ILP}	V _{PP}	Zeros

Notes:

7. X = "don't care" but not to exceed V_{CC} + 5%.

8. The power-down mode for the CY7C293A is activated by deselecting CS₁.

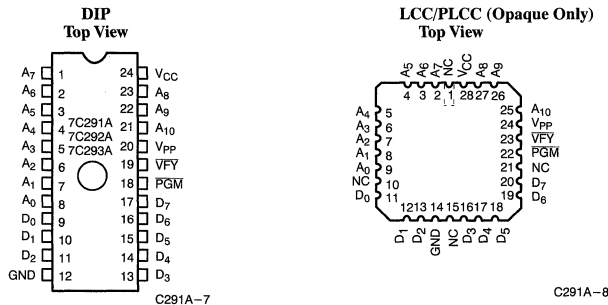


Figure 1. Programming Pinouts



Ordering Information^[9]

Speed (ns)	I _{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range	
20	120	CY7C291A-20JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial	
		CY7C291A-20PC	P13	24-Lead (300-Mil) Molded DIP		
		CY7C291A-20SC	S13	24-Lead Molded SOIC		
		CY7C291A-20WC	W14	24-Lead (300-Mil) Windowed CerDIP		
25	60	CY7C291AL-25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial	
		CY7C291AL-25PC	P13	24-Lead (300-Mil) Molded DIP		
		CY7C291AL-25WC	W14	24-Lead (300-Mil) Windowed CerDIP		
	90	60	CY7C291A-25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
			CY7C291A-25PC	P13	24-Lead (300-Mil) Molded DIP	
			CY7C291A-25SC	S13	24-Lead Molded SOIC	
			CY7C291A-25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	120	60	CY7C291A-25DMB	D14	24-Lead (300-Mil) CerDIP	Military
			CY7C291A-25LMB	L64	28-Square Leadless Chip Carrier	
			CY7C291A-25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
			CY7C291A-25TMB	T73	24-Lead Windowed Cerpack	
			CY7C291A-25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
30	120	CY7C291A-30DMB	D14	24-Lead (300-Mil) CerDIP	Military	
		CY7C291A-30LMB	L64	28-Square Leadless Chip Carrier		
		CY7C291A-30QMB	Q64	28-Pin Windowed Leadless Chip Carrier		
		CY7C291A-30TMB	T73	24-Lead Windowed Cerpack		
		CY7C291A-30WMB	W14	24-Lead (300-Mil) Windowed CerDIP		
35	60	CY7C291AL-35JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial	
		CY7C291AL-35PC	P13	24-Lead (300-Mil) Molded DIP		
		CY7C291AL-35WC	W14	24-Lead (300-Mil) Windowed CerDIP		
	90	60	CY7C291A-35SC	S13	24-Lead Molded SOIC	Commercial
			CY7C291A-35PC	P13	24-Lead (300-Mil) Molded DIP	
			CY7C291A-35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	120	60	CY7C291A-35DMB	D14	24-Lead (300-Mil) CerDIP	Military
			CY7C291A-35LMB	L64	28-Square Leadless Chip Carrier	
			CY7C291A-35QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
			CY7C291A-35TMB	T73	24-Lead Windowed Cerpack	
			CY7C291A-35WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
	50	60	CY7C291AL-50JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
CY7C291AL-50PC			P13	24-Lead (300-Mil) Molded DIP		
CY7C291AL-50WC			W14	24-Lead (300-Mil) Windowed CerDIP		
90		60	CY7C291A-50SC	S13	24-Lead Molded SOIC	Commercial
			CY7C291A-50PC	P13	24-Lead (300-Mil) Molded DIP	
			CY7C291A-50WC	W14	24-Lead (300-Mil) Windowed CerDIP	
90		60	CY7C291A-50DMB	D14	24-Lead (300-Mil) CerDIP	Military
			CY7C291A-50LMB	L64	28-Square Leadless Chip Carrier	
			CY7C291A-50QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
			CY7C291A-50TMB	T73	24-Lead Windowed Cerpack	
			CY7C291A-50WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

Note:

9. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.



MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB} ^[10]	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{AA}	7, 8, 9, 10, 11
t _{AC1} ^[11]	7, 8, 9, 10, 11
t _{AC2} ^[10]	7, 8, 9, 10, 11

Notes:

10. 7C293A only.

11. 7C291A and 7C292A only.

Document #: 38-00075-G

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962-87650	01KX	CY7C291-50TMB
5962-87650	01LX	CY7C291-50WMB
5962-87650	013X	CY7C291-50QMB
5962-87650	03KX	CY7C291-35TMB
5962-87650	03LX	CY7C291-35WMB
5962-87650	033X	CY7C291-35QMB
5962-88680	01LX	CY7C293A-50WMB
5962-88680	01KX	CY7C293A-50TMB
5962-88680	013X	CY7C293A-50QMB
5962-88680	02LX	CY7C293A-35WMB
5962-88680	02KX	CY7C293A-35TMB
5962-88680	023X	CY7C293A-35QMB
5962-88680	03LX	CY7C293A-30WMB
5962-88680	03KX	CY7C293A-30TMB
5962-88680	033X	CY7C293A-30QMB
5962-88680	04LX	CY7C293A-25WMB
5962-88680	04KX	CY7C293A-25TMB
5962-88680	043X	CY7C293A-25QMB
5962-88734	02JX	CY7C292A-45DMB
5962-88734	02KX	CY7C291A-45KMB
5962-88734	02LX	CY7C291A-45DMB
5962-88734	023X	CY7C291A-45LMB
5962-88734	03JX	CY7C292A-35DMB
5962-88734	03KX	CY7C291A-35KMB
5962-88734	03LX	CY7C291A-35DMB
5962-88734	033X	CY7C291A-35LMB
5962-88734	04JX	CY7C292A-25DMB
5962-88734	04KX	CY7C291A-25KMB
5962-88734	04LX	CY7C291A-25DMB
5962-88734	043X	CY7C291A-25LMB



Special Features

Depending on the specific CMOS PROM in question, additional features that require programming may be available to the designer. Two of these features are a Programmable Initial Byte and Programmable Synchronous/Asynchronous Enable available in some of the registered devices. Like programming the array, these features make use of EPROM cells and are programmed in a similar manner using supervoltages. The specific timing and programming requirements are specified in the data sheet of the device employing the feature. Several Cypress non-volatile memories feature an automatic device identification mode. This mode is accessed by placing the supervoltage on the A₉ address pin. While A₉ is HIGH, taking A₀ LOW will cause the Cypress manufacturer ID (34H) to appear on the outputs. Taking A₀ HIGH will cause the device identifier to appear on the outputs. See the specific datasheet for details.

Programming Support

Programming support for Cypress CMOS PROMs is available on Cypress's QuickPro II and Impulse 3. Support is also available from a number of programmer manufacturers, some of which are listed below. In addition, Cypress offers factory programming for all of these devices. Parts are programmed and 100% speed tested to your code to ensure performance. Custom marking is available also on programmed plastic (OTP) devices. Minimum quantities apply. Contact a Cypress sales representative for more information.

Cypress Semiconductor, Inc.
3901 North First St.
San Jose, CA 95134
(408) 943-2600

AVAL Data Corp.
M. K. Bldg. 2F 4-8 Nakaitabashi,
Itabashi-ku
Tokyo, Japan 173
03 (5375)-7321

BP Microsystems
10681 Haddington, Ste. #190
Houston, TX 77043
(800) 225-2102

Data I/O
Customer Resource Center
10525 Willows Rd. NE
P.O. Box 97046
Redmond, WA 98073-9746
(800) 247-5700
(206) 881-6444

Logical Devices Inc.
692 South Military Trail
Deerfield, FL 33442
(305) 428-6868

Minato Electronics
4105, Minami Yamada-cho
Kohoku-ku
Yokohama, Japan 223
(045) 591-5611

SMS Mikrocomputersystem GmbH
Im Grund 15
D-7988 Wangen im Allgeu
BRD
(49) 7522-5018

SMS Microcomputer
P.O. Box 1348
Lawrence, MA 01842
(508) 683-4659

Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
(408) 988-1118

System General
510 S. Park Victoria
Milpitas, CA 95035
(408) 263-6667

FIFOs
Page Number

Device	Description	Page Number
CY7C401	64 x 4 Cascadable FIFO	5-1
CY7C402	64 x 5 Cascadable FIFO	5-1
CY7C403	64 x 4 Cascadable FIFO	5-1
CY7C404	64 x 5 Cascadable FIFO	5-1
CY7C408A	64 x 8 Cascadable FIFO	5-12
CY7C409A	64 x 9 Cascadable FIFO	5-12
CY7C419	256 x 9 Cascadable FIFO	5-26
CY7C420	512 x 9 Cascadable FIFO	5-26
CY7C421	512 x 9 Cascadable FIFO	5-26
CY7C424	1K x 9 Cascadable FIFO	5-26
CY7C425	1K x 9 Cascadable FIFO	5-26
CY7C428	2K x 9 Cascadable FIFO	5-26
CY7C429	2K x 9 Cascadable FIFO	5-26
CY7C432	4K x 9 Cascadable FIFO	5-26
CY7C433	4K x 9 Cascadable FIFO	5-26
CY7C4421	64 x 9 Synchronous FIFO	5-48
CY7C4201	256 x 9 Synchronous FIFO	5-48
CY7C4211	512 x 9 Synchronous FIFO	5-48
CY7C4221	1K x 9 Synchronous FIFO	5-48
CY7C4231	2K x 9 Synchronous FIFO	5-48
CY7C4241	4K x 9 Synchronous FIFO	5-48
CY7C4251	8K x 9 Synchronous FIFO	5-48
CY7C4425	64 x 18 Synchronous FIFO	5-67
CY7C4205	256 x 18 Synchronous FIFO	5-67
CY7C4215	512 x 18 Synchronous FIFO	5-67
CY7C4225	1K x 18 Synchronous FIFO	5-67
CY7C4235	2K x 18 Synchronous FIFO	5-67
CY7C4245	4K x 18 Synchronous FIFO	5-67
CY7C439	Bidirectional 2K x 9 FIFO	5-86
CY7C441	Clocked 512 x 9 FIFO	5-99
CY7C443	Clocked 2K x 9 FIFO	5-99
CY7C451	512 x 9 Cascadable Clocked FIFO with Programmable Flags	5-115
CY7C453	2K x 9 Cascadable Clocked FIFO with Programmable Flags	5-115
CY7C455	512 x 18 Cascadable Clocked FIFO with Programmable Flags	5-138
CY7C456	1K x 18 Cascadable Clocked FIFO with Programmable Flags	5-138
CY7C457	2K x 18 Cascadable Clocked FIFO with Programmable Flags	5-138
CY7C460	Cascadable 8K x 9 FIFO	5-158
CY7C462	Cascadable 16K x 9 FIFO	5-158
CY7C464	Cascadable 32K x 9 FIFO	5-158
CY7C470	8K x 9 FIFO with Programmable Flags	5-171
CY7C472	16K x 9 FIFO with Programmable Flags	5-171
CY7C474	32K x 9 FIFO with Programmable Flags	5-171



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied -55°C to +125°C
 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Voltage Applied to Outputs in High Z State -0.5V to +7.0V
 DC Input Voltage -3.0V to +7.0V
 Power Dissipation 1.0W
 Output Current, into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)
 Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ±10%
Military ^[1]	-55°C to +125°C	5V ±10%

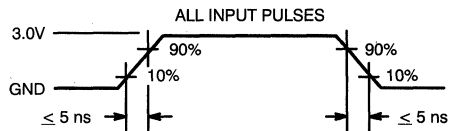
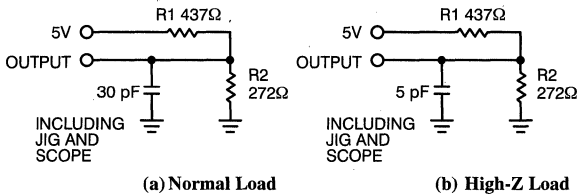
Electrical Characteristics Over the Operating Range (Unless Otherwise Noted)^[2]

Parameter	Description	Test Conditions	7C40X-10, 15, 25		Unit
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.0	6.0	V
V _{IL}	Input LOW Voltage		- 3.0	0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	- 10	+10	µA
V _{CD} ^[3]	Input Diode Clamp Voltage ^[3]				
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , V _{CC} = 5.5V Output Disabled (CY7C403 and CY7C404)	- 50	+50	µA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		- 90	mA
I _{CC}	Power Supply Current	V _{CC} = Max., I _O = 0 mA	Commercial	75	mA
			Military	90	mA

Capacitance^[5]

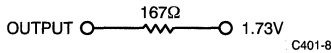
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 4.5V	5	pF
C _{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms



C401-7

Equivalent to: THÉVENIN EQUIVALENT



Notes:

- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- The CMOS process does not provide a clamp diode. However, the FIFO is insensitive to -3V dc input levels and -5V undershoot pulses of less than 10 ns (measured at 50% output).
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

Operational Description

Concept

Unlike traditional FIFOs, these devices are designed using a dual-port memory, read and write pointer, and control logic. The read and write pointers are incremented by the SO and SI respectively. The availability of an empty space to shift in data is indicated by the IR signal, while the presence of data at the output is indicated by the OR signal. The conventional concept of bubble-through is absent. Instead, the delay for input data to appear at the output is the time required to move a pointer and propagate an OR signal. The output enable (\overline{OE}) signal provides the capability to OR tie multiple FIFOs together on a common bus.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a master reset (MR) signal. This causes the FIFO to enter an empty condition signified by the OR signal being LOW at the same time the IR signal is HIGH. In this condition, the data outputs ($DO_0 - DO_n$) will be in a LOW state.

Shifting Data In

Data is shifted in on the rising edge of the SI signal. This loads input data into the first word location of the FIFO. On the falling edge of the SI signal, the write pointer is moved to the next word position and the IR signal goes HIGH, indicating the readiness to accept new data. If the FIFO is full, the IR will remain LOW until a word of data is shifted out.

Shifting Data Out

Data is shifted out of the FIFO on the falling edge of the SO signal. This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and the OR signal will go HIGH. If data is not present, the OR signal will stay LOW indicating the FIFO is empty. Upon the rising edge of SO, the OR signal goes LOW. The data outputs of the FIFO should be sampled with edge-sensitive type D flip-flops (or equivalent), using the SO signal as the clock input to the flip-flop.

Bubble-Through

Two bubble-through conditions exist. The first is when the device is empty. After a word is shifted into an empty device, the data propagates to the output. After a delay, the OR flag goes HIGH, indicating valid data at the output.

The second bubble-through condition occurs when the device is full. Shifting data out creates an empty location that propagates to the input. After a delay, the IR flag goes HIGH. If the SI signal is HIGH at this time, data on the input will be shifted in.

Possible Minimum Pulse Width Violation at the Boundary Conditions

If the handshaking signals IR and OR are not properly used to generate the SI and SO signals, it is possible to violate the minimum (effective) SI and SO positive pulse widths at the full and empty boundaries.

When this violation occurs, the operation of the FIFO is unpredictable. It must then be reset, and all data is lost.

Application of the 7C403–25/7C404–25 at 25 MHz

Application of the CY7C403 or CY7C404 Cypress CMOS FIFOs requires knowledge of characteristics that are not easily specified in a datasheet, but which are necessary for reliable operation under all conditions, so we will specify them here.

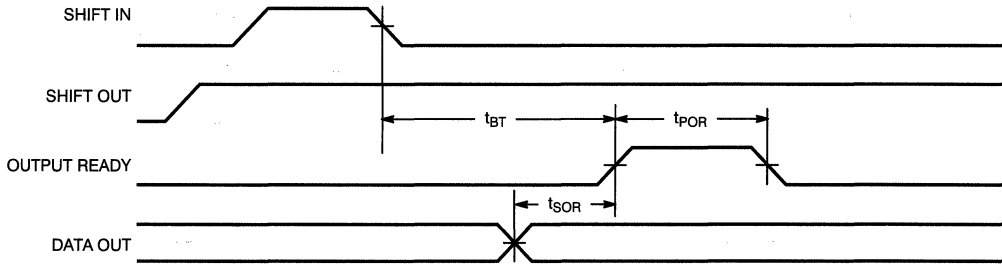
When an empty FIFO is filled with initial information at maximum “shift in” SI frequency, followed by immediate shifting out of the data also at maximum “shift out” SO frequency, the designer must

be aware of a window of time which follows the initial rising edge of the OR signal, during which time the SO signal is not recognized. This condition exists only at high-speed operation where more than one SO may be generated inside the prohibited window. This condition does not inhibit the operation of the FIFO at full-frequency operation, but rather delays the full 25-MHz operation until after the window has passed.

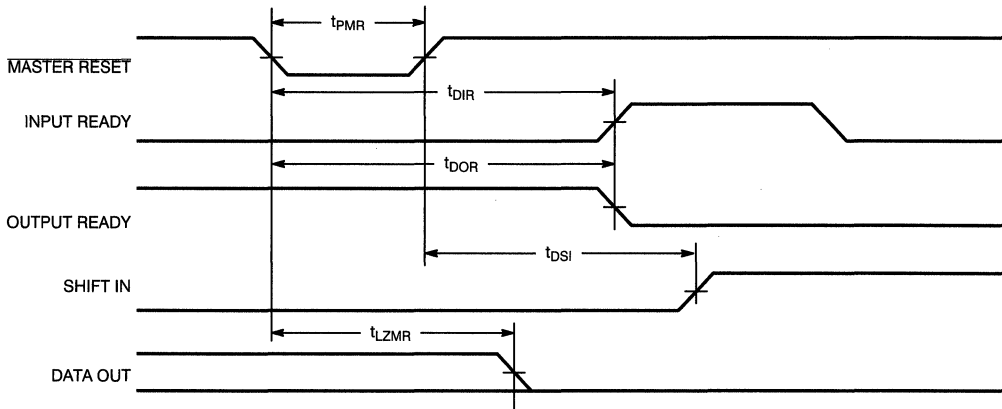
There are several implementation techniques for managing the window so that all SO signals are recognized:

1. The first involves delaying SO operation such that it does not occur in the critical window. This can be accomplished by causing a fixed delay of 40 ns “initiated by the SI signal only when the FIFO is empty” to inhibit or gate the SO activity. However, this requires that the SO operation be at least temporarily synchronized with the input SI operation. In synchronous applications this may well be possible and a valid solution.
2. Another solution not uncommon in synchronous applications is to only begin shifting data out of the FIFO when it is more than half full. This is a common method of FIFO application, as earlier FIFOs could not be operated at maximum frequency when near full or empty. Although Cypress FIFOs do not have this limitation, any system designed in this manner will not encounter the window condition described above.
3. The window may also be managed by not allowing the first SO signal to occur until the window in question has passed. This can be accomplished by delaying the SO 40 ns from the rising edge of the initial OR signal. This however involves the requirement that this only occurs on the first occurrence of data being loaded into the FIFO from an empty condition and therefore requires the knowledge of IR and SI conditions as well as SO.
4. Handshaking with the OR signal is a third method of avoiding the window in question. With this technique the rising edge of SO, or the fact that SO signal is HIGH, will cause the OR signal to go LOW. The SO signal is not taken LOW again, advancing the internal pointer to the next data, until the OR signal goes LOW. This ensures that the SO pulse that is initiated in the window will be automatically extended long enough to be recognized.
5. There remains the decision as to what signal will be used to latch the data from the output of the FIFO into the receiving source. The leading edge of the SO signal is most appropriate because data is guaranteed to be stable prior to and after the SO leading edge for each FIFO. This is a solution for any number of FIFOs in parallel.

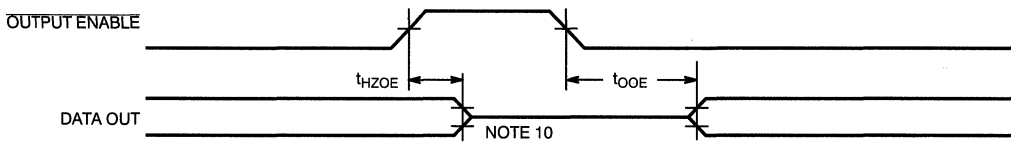
Any of the above solutions will ensure the correct operation of a Cypress FIFO at 25 MHz. The specific implementation is left to the designer and is dependent on the specific application needs.

Switching Waveforms (continued)
Bubble Through, Data In To Data Out Diagram


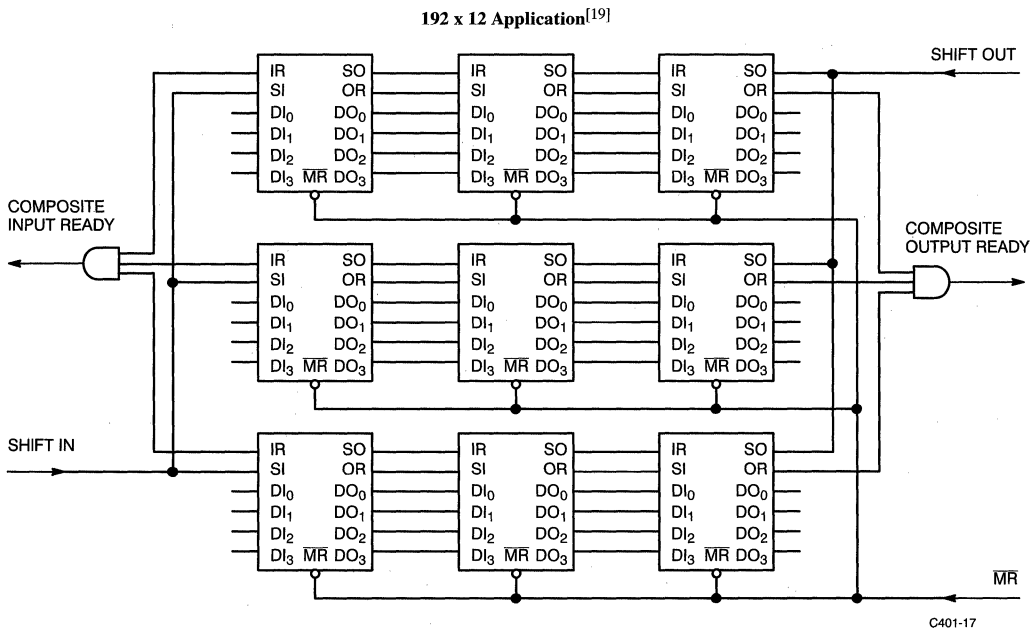
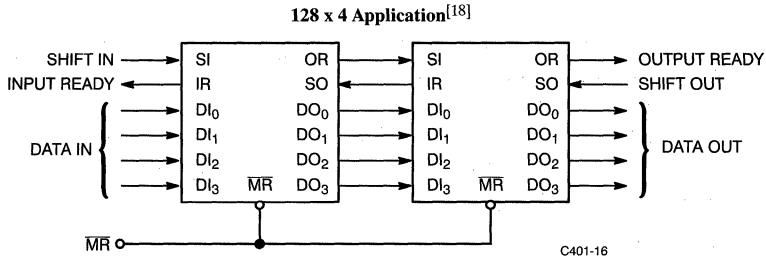
C401-12

Master Reset Timing Diagram


C401-13

Output Enable Timing Diagram


C401-14

FIFO Expansion^[13, 14, 15, 16, 17]

Notes:

13. When the memory is empty, the last word read will remain on the outputs until the master reset is strobed or a new data word bubbles through to the output. However, OR will remain LOW, indicating data at the output is not valid.
14. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data, and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid, stable data on the outputs.
15. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle (at least t_{ORL}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
16. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH, then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, then IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.
17. All Cypress FIFOs will cascade with other Cypress FIFOs. However, they may not cascade with pin-compatible FIFOs from other manufacturers.
18. FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.
19. FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite input and output ready flags. This need is due to the variation of delays of the FIFOs.



Ordering Information (continued)

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C403-10DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C403-10PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C403-10DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C403-10LMB	L61	20-Pin Square Leadless Chip Carrier	
15	CY7C403-15DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C403-15PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C403-15DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C403-15LMB	L61	20-Pin Square Leadless Chip Carrier	
25	CY7C403-25DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C403-25PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C403-25DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C403-25LMB	L61	20-Pin Square Leadless Chip Carrier	

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C404-10DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C404-10PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C404-10DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C404-10LMB	L61	20-Pin Square Leadless Chip Carrier	
15	CY7C404-15DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C404-15PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C404-15DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C404-15LMB	L61	20-Pin Square Leadless Chip Carrier	
25	CY7C404-25DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C404-25PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C404-25DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C404-25LMB	L61	20-Pin Square Leadless Chip Carrier	

64 x 8 Cascadable FIFO
64 x 9 Cascadable FIFO
Features

- 64 x 8 and 64 x 9 first-in first-out (FIFO) buffer memory
- 35-MHz shift in and shift out rates
- Almost Full/Almost Empty and Half Full flags
- Dual-port RAM architecture
- Fast (50-ns) bubble-through
- Independent asynchronous inputs and outputs
- Output enable (CY7C408A)
- Expandable in word width and FIFO depth
- 5V ±10% supply
- TTL compatible
- Capable of withstanding greater than 2001V electrostatic discharge voltage
- 300-mil, 28-pin DIP

Functional Description

The CY7C408A and CY7C409A are 64-word deep by 8- or 9-bit wide first-in first-out (FIFO) buffer memories. In addition to the industry-standard handshaking signals, almost full/almost empty (AFE) and half full (HF) flags are provided.

AFE is HIGH when the FIFO is almost full or almost empty, otherwise AFE is LOW. HF is HIGH when the FIFO is half full, otherwise HF is LOW.

The CY7C408A has an output enable (OE) function.

The memory accepts 8- or 9-bit parallel words at its inputs (DI₀ – DI₈) under the control of the shift in (SI) input when the input ready (IR) control signal is HIGH. The data is output, in the same order as it was stored, on the DO₀ – DO₈ output pins under the control of the shift out (SO) input when the output ready (OR) control signal is HIGH. If the FIFO is full (IR LOW), pulses at the SI input are ignored; if the FIFO is empty (OR LOW), pulses at the SO input are ignored.

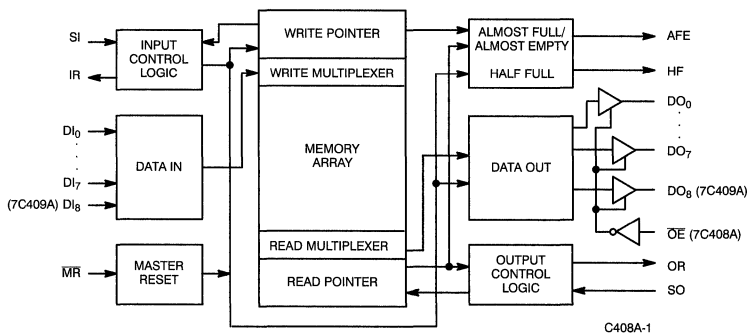
The IR and OR signals are also used to connect the FIFOs in parallel to make a wider word or in series to make a deeper buffer, or both.

Parallel expansion for wider words is implemented by logically ANDing the IR and OR outputs (respectively) of the individual FIFOs together (Figure 5). The AND operation insures that all of the FIFOs are either ready to accept more data (IR HIGH) or ready to output data

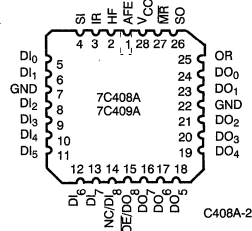
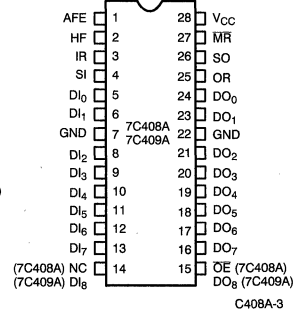
(OR HIGH) and thus compensate for variations in propagation delay times between devices.

Serial expansion (cascading) for deeper buffer memories is accomplished by connecting the data outputs of the FIFO closest to the data source (upstream device) to the data inputs of the following (downstream) FIFO (Figure 4). In addition, to insure proper operation, the SO signal of the upstream FIFO must be connected to the IR output of the downstream FIFO and the SI signal of the downstream FIFO must be connected to the OR output of the upstream FIFO. In this serial expansion configuration, the IR and OR signals are used to pass data through the FIFOs.

Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely differing operating frequencies. The high shift in and shift out rates of these FIFOs, and their high throughput rate due to the fast bubblethrough time, which is due to their dual-port RAM architecture, make them ideal for high-speed communications and controllers.

Logic Block Diagram

Flag Definitions

HF	AFE	Words Stored
L	H	0 – 8
L	L	9 – 31
H	L	32 – 55
H	H	56 – 64

Pin Configurations


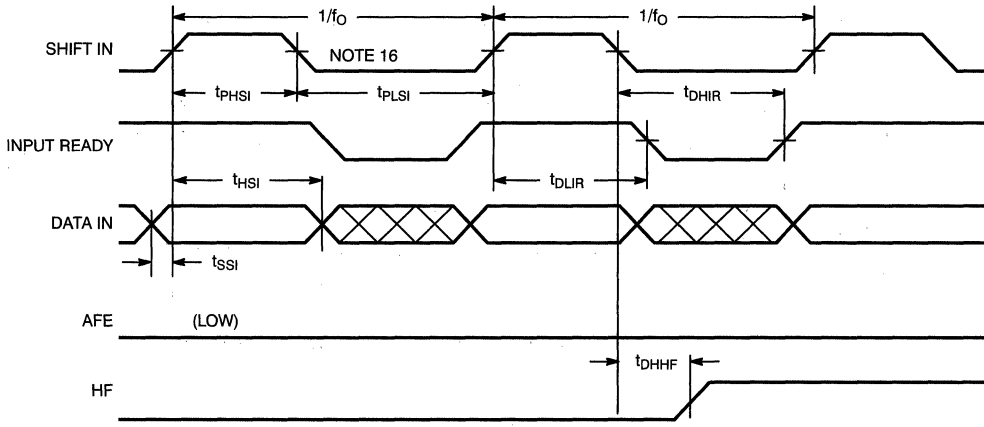


Switching Characteristics Over the Operating Range^[3, 6]

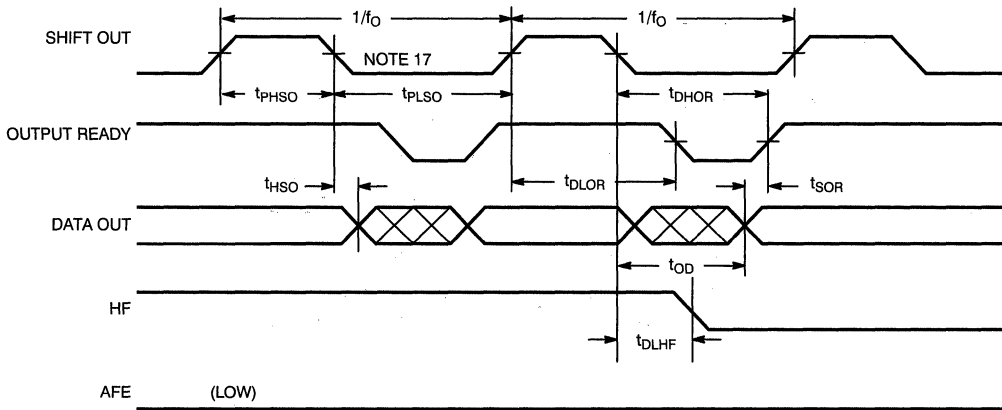
Parameter	Description	Test Conditions	7C408A-15 7C409A-15		7C408A-25 7C409A-25		7C408A-35 7C409A-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
f _O	Operating Frequency	Note 7		15		25		35	MHz
t _{PHSI}	SI HIGH Time	Note 7	23		11		9		ns
t _{PLSI}	SI LOW Time	Note 7	25		24		17		ns
t _{SSI}	Data Set-Up to SI	Note 8	0		0		0		ns
t _{HSI}	Data Hold from SI	Note 8	30		20		12		ns
t _{DLIR}	Delay, SI HIGH to IR LOW			35		21		15	ns
t _{DHIR}	Delay, SI LOW to IR HIGH			40		23		16	ns
t _{PHSO}	SO HIGH Time	Note 7	23		11		9		ns
t _{PLSO}	SO LOW Time	Note 7	25		24		17		ns
t _{DLOR}	Delay, SO HIGH to OR LOW			35		21		15	ns
t _{DHOR}	Delay, SO LOW to OR HIGH			40		23		16	ns
t _{SOR}	Data Set-Up to OR HIGH		0		0		0		ns
t _{HSO}	Data Hold from SO LOW		0		0		0		ns
t _{BT}	Fall-through, Bubble-back Time		10	65	10	60	10	50	ns
t _{SIR}	Data Set-Up to IR	Note 9	5		5		5		ns
t _{HIR}	Data Hold from IR	Note 9	30		20		20		ns
t _{PIR}	Input Ready Pulse HIGH	Note 10	6		6		6		ns
t _{POR}	Output Ready Pulse HIGH	Note 11	6		6		6		ns
t _{DLZOE}	OE LOW to LOW Z (7C408A)	Note 12		35		30		25	ns
t _{DHZOE}	OE HIGH to HIGH Z (7C408A)	Note 7		35		30		25	ns
t _{DHHF}	SI LOW to HF HIGH			65		55		45	ns
t _{DLHF}	SO LOW to HF LOW			65		55		45	ns
t _{DLAFE}	SO or SI LOW to AFE LOW			65		55		45	ns
t _{DHAFE}	SO or SI LOW to AFE HIGH			65		55		45	ns
t _{PMR}	\overline{MR} Pulse Width		55		45		35		ns
t _{DSI}	\overline{MR} HIGH to SI HIGH		25		10		10		ns
t _{DOR}	\overline{MR} LOW to OR LOW			55		45		35	ns
t _{DIR}	\overline{MR} LOW to IR HIGH			55		45		35	ns
t _{LZMR}	\overline{MR} LOW to Output LOW	Note 13		55		45		35	ns
t _{AFE}	\overline{MR} LOW to AFE HIGH			55		45		35	ns
t _{HF}	\overline{MR} LOW to HF LOW			55		45		35	ns
t _{OD}	SO LOW to Next Data Out Valid			28		20		16	ns

Notes:

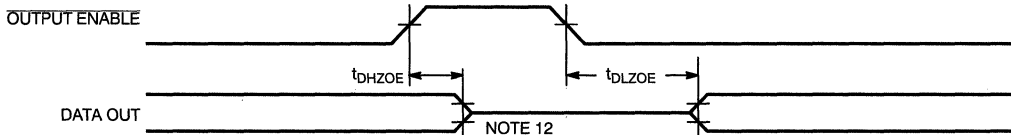
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in parts (a) and (b) of AC Test Loads and Waveforms.
- t_{DHZOE} and t_{DLZOE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. t_{DHZOE} transition is measured ±500 mV from steady-state voltage. t_{DLZOE} transition is measured ±100 mV from steady-state voltage. These parameters are guaranteed and not 100% tested.
- All data outputs will be at LOW level after reset goes HIGH until data is entered into the FIFO.
- 1/f_O ≥ (t_{PHSI} + t_{PLSI}), 1/f_O ≥ (t_{PHSO} + t_{PLSO}).
- t_{SSI} and t_{HSI} apply when memory is not full.
- t_{SIR} and t_{HIR} apply when memory is full, SI is high and minimum bubble-through (t_{BT}) conditions exist.
- At any given operating condition t_{PIR} ≥ (t_{PHSO} required).
- At any given operating condition t_{POR} ≥ (t_{PHSI} required).

Switching Waveforms (continued)
Data In Timing Diagram


C408A-9

Data Out Timing Diagram


C408A-10

Output Enable (CY7C408A only)


C408A-11

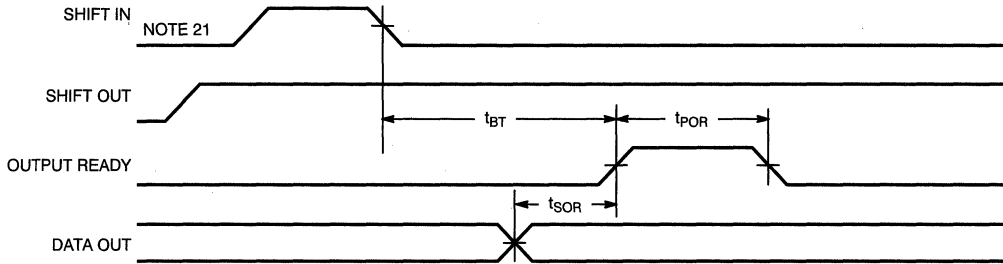
Notes:

16. FIFO contains 31 words.

17. FIFO contains 32 words.

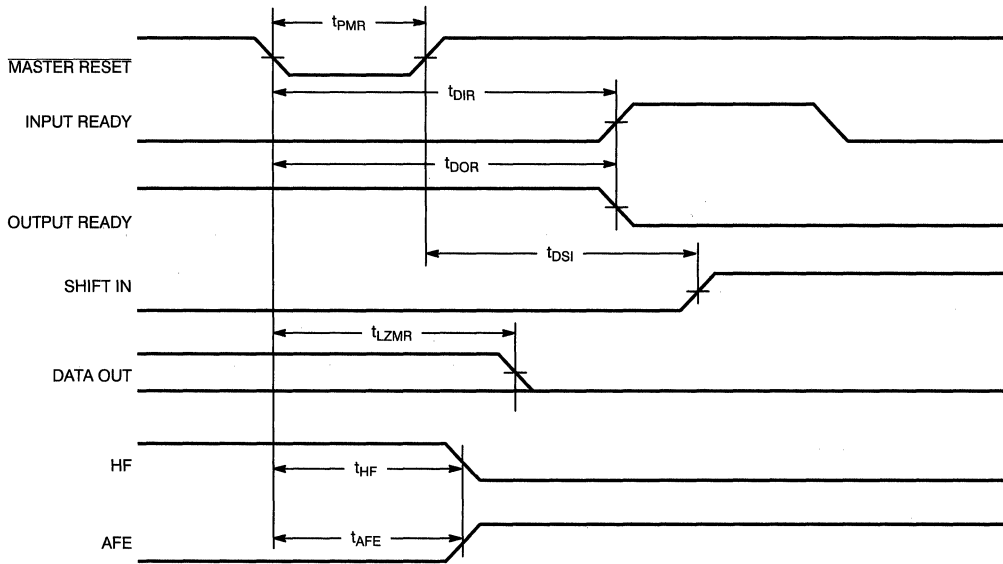
Switching Waveforms (continued)

Fall-Through, Data In to Data Out Diagram



C408A-15

Master Reset Timing Diagram



C408A-16

Note:
21. FIFO is empty.

Cascading the 7C408/9A – 35 Above 25 MHz

First, the capacity of N cascaded FIFOs is decreased from $N \times 64$ to $(N \times 63) + 1$.

If cascaded FIFOs are to be operated with an external clock rate greater than 25 MHz, the interface IR signal must be inverted before being fed back to the interface SO pin (Figure 3). Two things should be noted when this configuration is implemented.

First, the capacity of N cascaded FIFOs is decreased from $N \times 64$ to $(N \times 63) + 1$.

Secondly, the frequency at the cascade interface is less than the 35 MHz rate at which the external clocks may operate. Therefore, the first device has its data shifted in faster than it is shifted out, and eventually this device becomes momentarily full. When this occurs, the maximum sustainable external clock frequency changes from 35 MHz to the cascade interface frequency.^[28]

When data packets^[29] are transmitted, this phenomenon does not occur unless more than three FIFOs are depth cascaded. For example, if two FIFOs are cascaded, a packet of 127 ($= 2 \times 63 + 1$) words may be shifted in at up to 35 MHz and then the entire packet may be shifted out at up to 35 MHz.

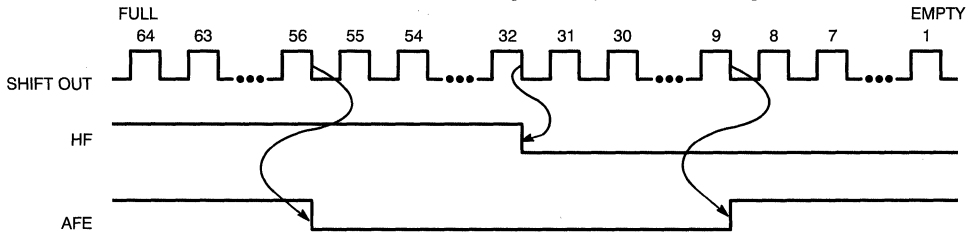


Figure 2. Shifting Words Out

C408A-18

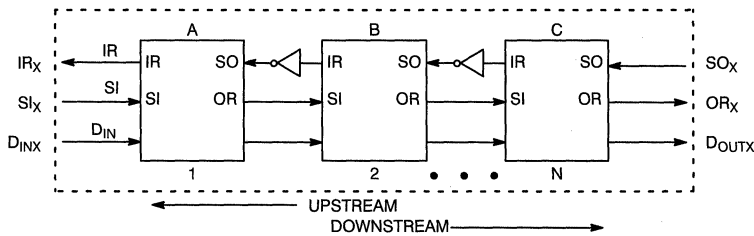


Figure 3. Cascaded Configuration Above 25 MHz

C408A-19

128 x 9 Configuration

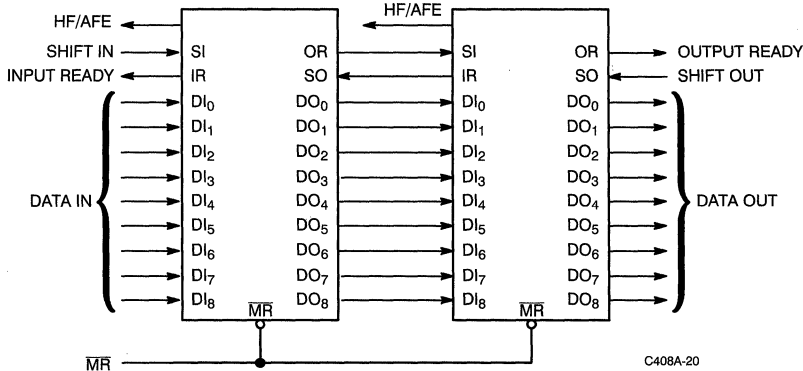
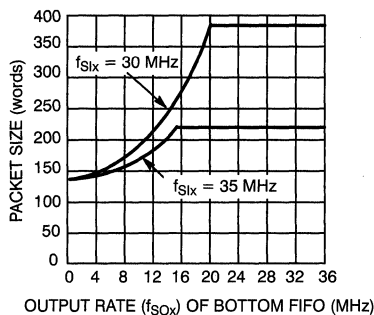


Figure 4. Cascaded Configuration at or below 25 MHz^[22, 23, 24, 25, 26]

C408A-20

If data is to be shifted out simultaneously with the data being shifted in, the concept of “virtual capacity” is introduced. Virtual capacity is simply how large a packet of data can be shifted in at a fixed frequency, e.g., 35 MHz, simultaneously with data being shifted out at any given frequency. *Figure 6* is a graph of packet size^[30] vs. shift out frequency (f_{SOx}) for two different values of shift in frequency (f_{SIx}) when two FIFOs are cascaded.

The exact complement of this occurs if the FIFOs initially contain data and a high shift out frequency is to be maintained, i.e., a 35 MHz f_{SOx} can be sustained when reading data packets from devices cascaded two or three deep.^[31] If data is shifted in simultaneously, *Figure 6* applies with f_{SIx} and f_{SOx} interchanged.



C408A-22

Figure 6. Virtual Capacity vs. Output Rate for Two FIFOs Cascaded Using an Inverter

Notes:

- 28. Because the data throughput in the cascade interface is dependent on the inverter delay, it is recommended that the fastest available inverter be used.
- 29. Transmission of data packets assumes that up to the maximum cumulative capacity of the FIFOs is shifted in without simultaneous shift out

clock occurring. The complement of this holds when data is shifted out as a packet.

- 30. These are typical packet sizes using an inverter whose delay is 4 ns.
- 31. Only devices with the same speed grade are specified to cascade together.

Ordering Information

Frequency (MHz)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C408A-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C408A-15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C408A-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C408A-15LMB	L64	28-Square Leadless Chip Carrier	
25	CY7C408A-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C408A-25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C408A-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C408A-25LMB	L64	28-Square Leadless Chip Carrier	
35	CY7C408A-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C408A-35VC	V21	28-Lead (300-Mil) Molded SOJ	

Frequency (MHz)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C409A-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C409A-15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C409A-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C409A-15LMB	L64	28-Square Leadless Chip Carrier	
25	CY7C409A-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C409A-25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C409A-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C409A-25LMB	L64	28-Square Leadless Chip Carrier	
35	CY7C409A-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C409A-35VC	V21	28-Lead (300-Mil) Molded SOJ	



CY7C419/21/25/29/33

256 x 9, 512 x 9, 1K x 9, 2K x 9, 4K x 9 Cascadable FIFO

Features

- 256 x 9, 512 x 9, 1,024 x 9, 2048 x 9, and 4096 x 9 FIFO buffer memory
- Dual-port RAM cell
- Asynchronous read/write
- High-speed 50.0-MHz read/write independent of depth/width
- Low operating power
— $I_{CC1} = 35 \text{ mA}$
- Half Full flag in standalone
- Empty and Full flags
- Retransmit in standalone
- Expandable in width and depth
- Parallel cascade minimizes bubble-through
- $5V \pm 10\%$ supply
- 300-mil DIP packaging
- 7x7 TQFP
- 300-mil SOJ packaging
- TTL compatible
- Three-state outputs
- Pin compatible and functional equivalent to IDT7200, IDT7201, IDT7202, IDT7203, and IDT7204

Functional Description

The CY7C419, CY7C420/1, CY7C424/5, CY7C428/9, and CY7C432/3 are first-in first-out (FIFO) memories offered in 600-mil wide and 300-mil wide packages. They are, respectively, 256, 512, 1,024, 2,048, and 4,096 words by 9-bits wide. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays, so that throughput is not reduced. Data is steered in a similar manner.

The read and write operations may be asynchronous; each can occur at a rate of 50.0 MHz. The write operation occurs when the write (\bar{W}) signal is LOW. Read occurs when read (\bar{R}) goes LOW. The nine

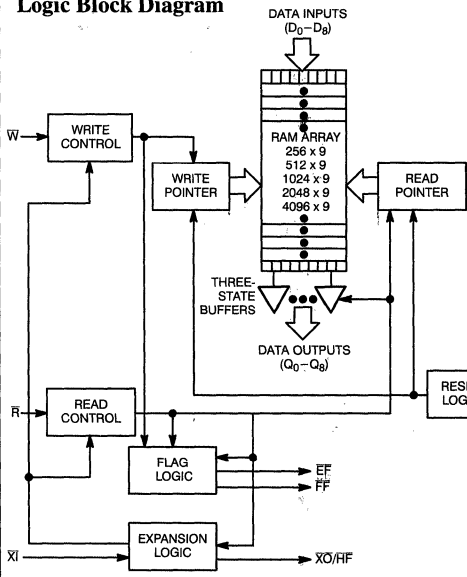
data outputs go to the high-impedance state when \bar{R} is HIGH.

A Half Full (HF) output flag is provided that is valid in the standalone and width expansion configurations. In the depth expansion configuration, this pin provides the expansion out (XO) information that is used to tell the next FIFO that it will be activated.

In the standalone and width expansion configurations, a LOW on the retransmit (RT) input causes the FIFOs to retransmit the data. Read enable (\bar{R}) and write enable (\bar{W}) must both be HIGH during retransmit, and then \bar{R} is used to access the data.

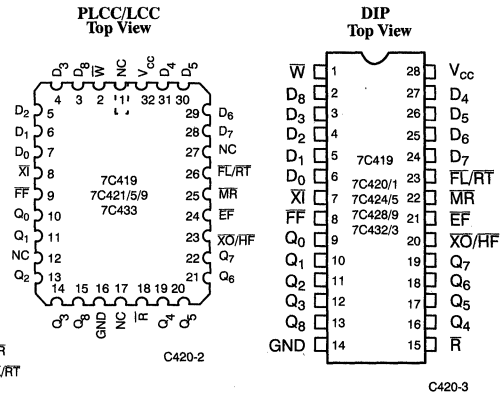
The CY7C419, CY7C420, CY7C421, CY7C424, CY7C425, CY7C428, CY7C429, CY7C432, and CY7C433 are fabricated using an advanced 0.65-micron P-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by careful layout and guard rings.

Logic Block Diagram



C420-1

Pin Configurations



C420-3

Electrical Characteristics Over the Operating Range^[2] (continued)

Parameter	Description	Test Conditions	7C419-10		7C419-15		7C419-20		7C419-25		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
I _{CC}	Operating Current	V _{CC} = Max., I _{OUT} = 0 mA f = f _{MAX}	Com'l		85		65		55		50	mA
			Mil/Ind				100		90		80	
I _{CC1}	Operating Current	V _{CC} = Max., I _{OUT} = 0 mA F = 20 MHz	Com'l		35		35		35		35	mA
I _{SB1}	Standby Current	All Inputs = V _{IH} Min.	Com'l		10		10		10		10	mA
			Mil/Ind				15		15		15	
I _{SB2}	Power-Down Current	All Inputs ≥ V _{CC} - 0.2V	Com'l		5		5		5		5	mA
			Mil/Ind				8		8		8	

Electrical Characteristics Over the Operating Range^[2] (continued)

Parameter	Description	Test Conditions	7C419-30		7C419-40		7C419-65		Units	
			Min.	Max.	Min.	Max.	Min.	Max.		
I _{CC}	Operating Current	V _{CC} = Max., I _{OUT} = 0 mA f = f _{MAX}	Com'l		40		35		35	mA
			Mil/Ind				75		70	
I _{CC1}	Operating Current	V _{CC} = Max., I _{OUT} = 0 mA F = 20 MHz	Com'l		35		35		35	mA
I _{SB1}	Standby Current	All Inputs = V _{IH} Min.	Com'l		10		10		10	mA
			Mil				15		15	
I _{SB2}	Power-Down Current	All Inputs ≥ V _{CC} - 0.2V	Com'l		5		5		5	mA
			Mil				8		8	

Capacitance^[5]

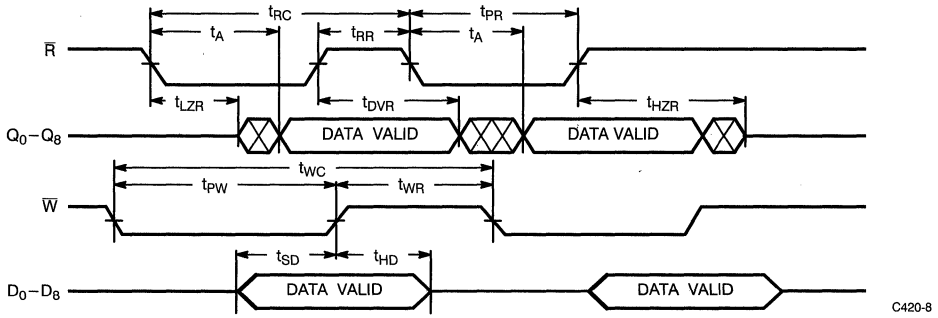
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 4.5V	6	pF
C _{OUT}	Output Capacitance		6	pF

Notes:

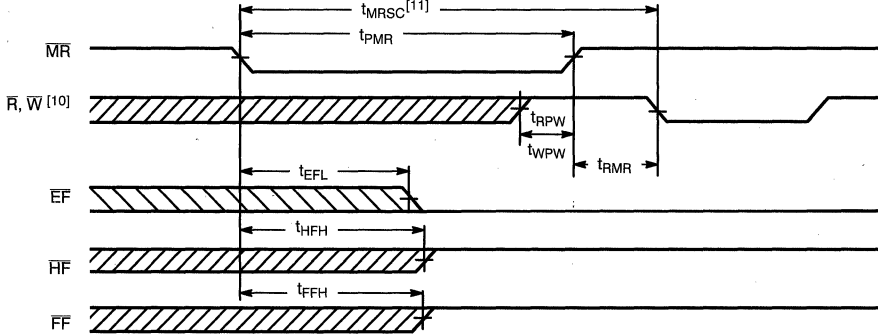
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- V_{IL} (Min.) = -2.0V for pulse durations of less than 20 ns.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range^[6, 7] (continued)

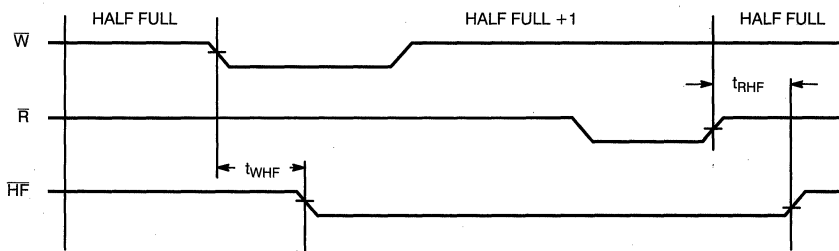
Parameter	Description	7C419-10		7C419-15		7C419-20		7C419-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{EFL}	MR to EF LOW		20		25		30		35	ns
t _{HFH}	MR to HF HIGH		20		25		30		35	ns
t _{FFH}	MR to FF HIGH		20		25		30		35	ns
t _{REF}	Read LOW to EF LOW		10		15		20		25	ns
t _{RFF}	Read HIGH to FF HIGH		10		15		20		25	ns
t _{WEF}	Write HIGH to EF HIGH		10		15		20		25	ns
t _{WFF}	Write LOW to FF LOW		10		15		20		25	ns
t _{WHF}	Write LOW to HF LOW		10		15		20		25	ns
t _{RHF}	Read HIGH to HF HIGH		10		15		20		25	ns
t _{RAE}	Effective Read from Write HIGH		10		15		20		25	ns
t _{RPE}	Effective Read Pulse Width After EF HIGH	10		15		20		25		ns
t _{WAF}	Effective Write from Read HIGH		10		15		20		25	ns
t _{WPF}	Effective Write Pulse Width After FF HIGH	10		15		20		25		ns
t _{XOL}	Expansion Out LOW Delay from Clock		10		15		20		25	ns
t _{XOH}	Expansion Out HIGH Delay from Clock		10		15		20		25	ns

Switching Waveforms
Asynchronous Read and Write


C420-8

Master Reset


C420-9

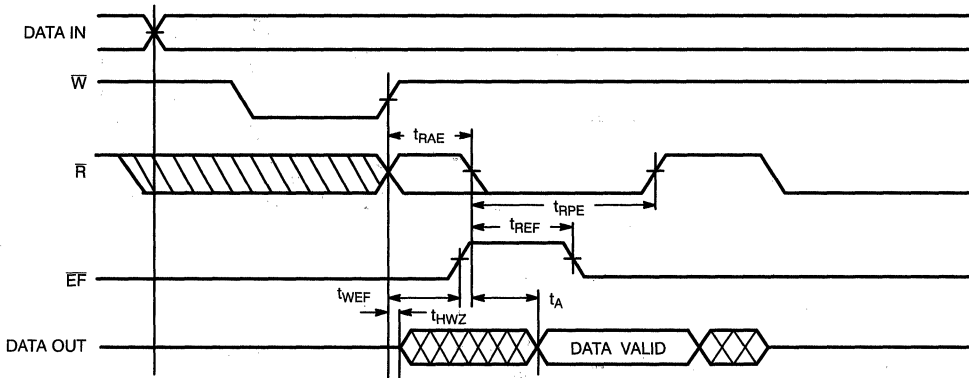
Half-Full Flag


C420-10

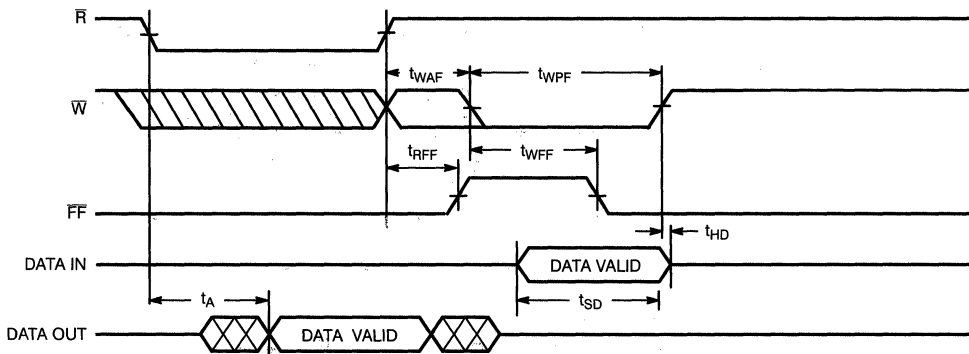
Notes:

 10. \overline{W} and $\overline{R} \geq V_{IH}$ around the rising edge of \overline{MR} .

 11. $t_{MRSC} = t_{PMR} + t_{RMR}$.

Switching Waveforms (continued)
Empty Flag and Read Data Flow-Through Mode


C420-14

Full Flag and Write Data Flow-Through Mode


C420-15

Architecture

The CY7C419, CY7C420/1, CY7C424/5, CY7C428/9, CY7C432/3 FIFOs consist of an array of 256, 512, 1024, 2048, 4096 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals (\bar{W} , \bar{R} , \bar{X} , \bar{XO} , \bar{FL} , \bar{RT} , \bar{MR}), and Full, Half Full, and Empty flags.

Dual-Port RAM

The dual-port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data propagation through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset (\bar{MR}) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag (\bar{EF}) being LOW, and both the Half Full (\bar{HF}) and Full flags (\bar{FF}) being HIGH. Read (\bar{R}) and write (\bar{W}) must be HIGH t_{RPW}/t_{WPW} before and t_{RMR} after the rising edge of \bar{MR} for a valid reset cycle. If reading from the FIFO after a reset cycle is attempted, the outputs will all be in the high-impedance state.

Writing Data to the FIFO

The availability of at least one empty location is indicated by a HIGH \bar{FF} . The falling edge of \bar{W} initiates a write cycle. Data appearing at the inputs ($D_0 - D_8$) t_{SD} before and t_{HD} after the rising edge of \bar{W} will be stored sequentially in the FIFO.

The \bar{EF} LOW-to-HIGH transition occurs t_{WEF} after the first LOW-to-HIGH transition of \bar{W} for an empty FIFO. \bar{HF} goes LOW t_{WHF} after the falling edge of \bar{W} following the FIFO actually being Half Full. Therefore, the \bar{HF} is active once the FIFO is filled to half its capacity plus one word. \bar{HF} will remain LOW while less than one half of total memory is available for writing. The LOW-to-HIGH transition of \bar{HF} occurs t_{RHF} after the rising edge of \bar{R} when the FIFO goes from half full +1 to half full. \bar{HF} is available in standalone and width expansion modes. \bar{FF} goes LOW t_{WFF} after the falling edge of \bar{W} , during the cycle in which the last available location is filled. Internal logic prevents overrunning a full FIFO. Writes to a full FIFO are ignored and the write pointer is not incremented. \bar{FF} goes HIGH t_{RFF} after a read from a full FIFO.

Reading Data from the FIFO

The falling edge of \bar{R} initiates a read cycle if the \bar{EF} is not LOW. Data outputs ($Q_0 - Q_8$) are in a high-impedance condition between read operations (\bar{R} HIGH), when the FIFO is empty, or when the FIFO is not the active device in the depth expansion mode.

When one word is in the FIFO, the falling edge of \bar{R} initiates a HIGH-to-LOW transition of \bar{EF} . The rising edge of \bar{R} causes the data outputs to go to the high-impedance state and remain such until a write is performed. Reads to an empty FIFO are ignored and do not increment the read pointer. From the empty condition, the FIFO can be read t_{WEF} after a valid write.

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit (\bar{RT}) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred since the last \bar{MR} cycle. A LOW pulse on \bar{RT} resets the

internal read pointer to the first physical location of the FIFO. \bar{R} and \bar{W} must both be HIGH while and t_{RTR} after retransmit is LOW. With every read cycle after retransmit, previously accessed data as well as not previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of \bar{RT} are retransmitted also.

Up to the full depth of the FIFO can be repeatedly retransmitted.

Standalone/Width Expansion Modes

Standalone and width expansion modes are set by grounding Expansion In (\bar{XI}) and tying First Load (\bar{FL}) to V_{CC} . FIFOs can be expanded in width to provide word widths greater than nine in increments of nine. During width expansion mode, all control line inputs are common to all devices, and flag outputs from any device can be monitored.

Depth Expansion Mode (see Figure 1)

Depth expansion mode is entered when, during a \bar{MR} cycle, Expansion Out (\bar{XO}) of one device is connected to Expansion In (\bar{XI}) of the next device, with \bar{XO} of the last device connected to \bar{XI} of the first device. In the depth expansion mode the First Load (\bar{FL}) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, \bar{XO} is pulsed LOW when the last physical location of the previous FIFO is written to and pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9. When expanding in depth, a composite \bar{FF} must be created by ORing the \bar{FF} s together. Likewise, a composite \bar{EF} is created by ORing the \bar{EF} s together. \bar{HF} and \bar{RT} functions are not available in depth expansion mode.

Use of the Empty and Full Flags

In order to achieve the maximum frequency, the flags must be valid at the beginning of the next cycle. However, because they can be updated by either edge of the read or write signal, they must be valid by one-half of a cycle. Cypress FIFOs meet this requirement; some competitors' FIFOs do not.

The reason why the flags are required to be valid by the next cycle is fairly complex. It has to do with the "effective pulse width violation" phenomenon, which can occur at the full and empty boundary conditions, if the flags are not properly used. The empty flag must be used to prevent reading from an empty FIFO and the full flag must be used to prevent writing into a full FIFO.

For example, consider an empty FIFO that is receiving read pulses. Because the FIFO is empty, the read pulses are ignored by the FIFO, and nothing happens. Next, a single word is written into the FIFO, with a signal that is asynchronous to the read signal. The (internal) state machine in the FIFO goes from empty to empty+1. However, it does this asynchronously with respect to the read signal, so that it cannot be determined what the effective pulse width of the read signal is, because the state machine does not look at the read signal until it goes to the empty+1 state. In a similar manner, the minimum write pulse width may be violated by attempting to write into a full FIFO, and asynchronously performing a read. The empty and full flags are used to avoid these effective pulse width violations, but in order to do this and operate at the maximum frequency, the flag must be valid at the beginning of the next cycle.

Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
10	CY7C419-10AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419-10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419-10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419-10VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C419-15AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419-15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419-15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C419-15PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419-15VI	V21	28-Lead (300-Mil) Molded SOJ	Military
	CY7C419-15DMB	D22	28-Lead (300-Mil) CerDIP	
20	CY7C419-20AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419-20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419-20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419-20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419-20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C419-20PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419-20VI	V21	28-Lead (300-Mil) Molded SOJ	Military
	CY7C419-20DMB	D22	28-Lead (300-Mil) CerDIP	
25	CY7C419-25AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419-25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419-25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419-25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C419-25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419-25VI	V21	28-Lead (300-Mil) Molded SOJ	Military
	CY7C419-25DMB	D22	28-Lead (300-Mil) CerDIP	
30	CY7C419-30AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419-30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419-30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419-30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419-30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C419-30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419-30VI	V21	28-Lead (300-Mil) Molded SOJ	Military
	CY7C419-30DMB	D22	28-Lead (300-Mil) CerDIP	
40	CY7C419-40AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419-40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419-40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419-40VC	V21	28-Lead (300-Mil) Molded SOJ	



Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
10	CY7C421-10AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421-10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421-10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-10VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C421-15AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421-15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421-15PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-15VI	V21	28-Lead (300-Mil) Molded SOJ	Military
	CY7C421-15DMB	D22	28-Lead (300-Mil) CerDIP	
CY7C421-15LMB	L55	32-Pin Rectangular Leadless Chip Carrier		
20	CY7C421-20AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421-20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421-20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421-20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421-20PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-20VI	V21	28-Lead (300-Mil) Molded SOJ	Military
	CY7C421-20DMB	D22	28-Lead (300-Mil) CerDIP	
CY7C421-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier		
25	CY7C421-25AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421-25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421-25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421-25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-25VI	V21	28-Lead (300-Mil) Molded SOJ	Military
	CY7C421-25DMB	D22	28-Lead (300-Mil) CerDIP	
CY7C421-25LMB	L55	32-Pin Rectangular Leadless Chip Carrier		
30	CY7C421-30AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421-30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421-30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421-30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421-30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-30VI	V21	28-Lead (300-Mil) Molded SOJ	Military
	CY7C421-30DMB	D22	28-Lead (300-Mil) CerDIP	
CY7C421-30LMB	L55	32-Pin Rectangular Leadless Chip Carrier		

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
10	CY7C425-10AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425-10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425-10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425-10VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C425-15AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425-15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425-15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425-15PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425-15VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
CY7C425-15LMB	L55	32-Pin Rectangular Leadless Chip Carrier		
20	CY7C425-20AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425-20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425-20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425-20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425-20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425-20PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425-20VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
CY7C425-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier		
25	CY7C425-25AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425-25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425-25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425-25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425-25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425-25VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
CY7C425-25LMB	L55	32-Pin Rectangular Leadless Chip Carrier		
30	CY7C425-30AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425-30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425-30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425-30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425-30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425-30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425-30VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425-30DMB	D22	28-Lead (300-Mil) CerDIP	Military
CY7C425-30LMB	L55	32-Pin Rectangular Leadless Chip Carrier		

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
10	CY7C429-10AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429-10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429-10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429-10VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C429-15AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429-15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429-15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429-15PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429-15VI	V21	28-Lead (300-Mil) Molded SOJ	Military
	CY7C429-15DMB	D22	28-Lead (300-Mil) CerDIP	
CY7C429-15LMB	L55	32-Pin Rectangular Leadless Chip Carrier		
20	CY7C429-20AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429-20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429-20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429-20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429-20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429-20PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429-20VI	V21	28-Lead (300-Mil) Molded SOJ	Military
	CY7C429-20DMB	D22	28-Lead (300-Mil) CerDIP	
CY7C429-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier		
25	CY7C429-25AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429-25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429-25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429-25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429-25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429-25VI	V21	28-Lead (300-Mil) Molded SOJ	Military
	CY7C429-25DMB	D22	28-Lead (300-Mil) CerDIP	
CY7C429-25LMB	L55	32-Pin Rectangular Leadless Chip Carrier		
30	CY7C429-30AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429-30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429-30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429-30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429-30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429-30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429-30VI	V21	28-Lead (300-Mil) Molded SOJ	Military
	CY7C429-30DMB	D22	28-Lead (300-Mil) CerDIP	
CY7C429-30LMB	L55	32-Pin Rectangular Leadless Chip Carrier		
40	CY7C429-40AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429-40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429-40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429-40VC	V21	28-Lead (300-Mil) Molded SOJ	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C433-20AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433-20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433-20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433-20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433-20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433-20PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433-20VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
CY7C433-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier		
25	CY7C433-25AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433-25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433-25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433-25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433-25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433-25VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
CY7C433-25LMB	L55	32-Pin Rectangular Leadless Chip Carrier		
30	CY7C433-30AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433-30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433-30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433-30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433-30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433-30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433-30VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433-30DMB	D22	28-Lead (300-Mil) CerDIP	Military
CY7C433-30LMB	L55	32-Pin Rectangular Leadless Chip Carrier		
40	CY7C433-40AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433-40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433-40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433-40VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433-40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433-40PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433-40VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433-40DMB	D22	28-Lead (300-Mil) CerDIP	Military
CY7C433-40LMB	L55	32-Pin Rectangular Leadless Chip Carrier		
65	CY7C433-65AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433-65JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433-65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433-65VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433-65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433-65PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433-65VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433-65DMB	D22	28-Lead (300-Mil) CerDIP	Military
CY7C433-65LMB	L55	32-Pin Rectangular Leadless Chip Carrier		



CY7C4421/4201/4211/4221 CY7C4231/4241/4251

64/256/512/1K/2K/4K/8K x 9 Synchronous FIFOs

Features

- 64 x 9 (CY7C4421)
- 256 x 9 (CY7C4201)
- 512 x 9 (CY7C4211)
- 1K x 9 (CY7C4221)
- 2K x 9 (CY7C4231)
- 4K x 9 (CY7C4241)
- 8K x 9 (CY7C4251)
- High-speed 100-MHz operation (10 ns read/write cycle time)
- Pin compatible and functionally equivalent to IDT72421, 72201, 72211, 72221, 72231, 72241
- Fully asynchronous and simultaneous read and write operation
- Four status flags: Empty, Full, and programmable Almost Empty/Almost Full
- Expandable in width

- Low operating power
 $I_{CC2} = 50 \text{ mA}$
- Output Enable (\overline{OE}) pin
- 32-pin PLCC/TQFP

Functional Description

The CY7C42X1 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. All are 9 bits wide. The CY7C42X1 are pin-compatible to IDT722X1. The CY7C42X1 can be cascaded to increase FIFO depth. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

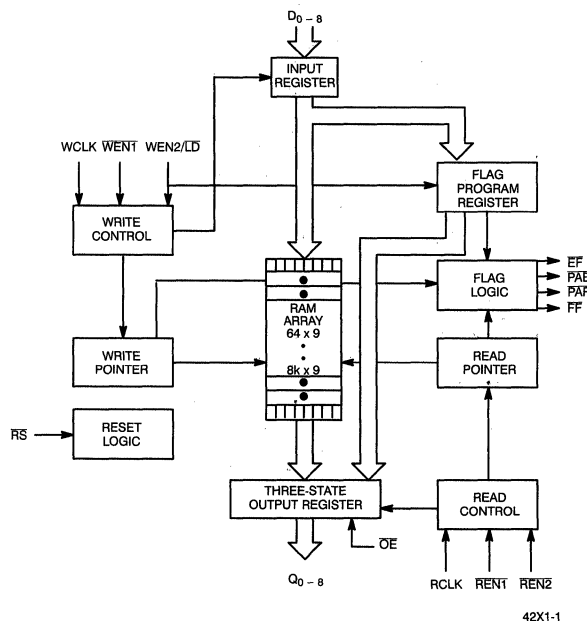
These FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (WCLK)

and two write-enable pins ($\overline{WEN1}$, $\overline{WEN2/LD}$).

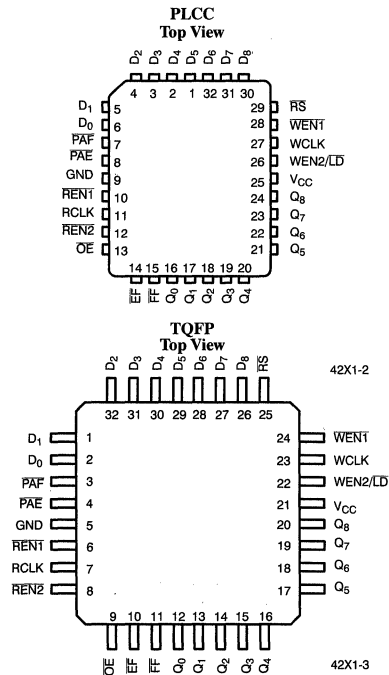
When $\overline{WEN1}$ is LOW and $\overline{WEN2/LD}$ is HIGH, data is written into the FIFO on the rising edge of the WCLK signal. While $\overline{WEN1}$, $\overline{WEN2/LD}$ is held active, data is continually written into the FIFO on each WCLK cycle. The output port is controlled in a similar manner by a free-running read clock (RCLK) and two read enable pins ($\overline{REN1}$, $\overline{REN2}$). In addition, the CY7C42X1 has an output enable pin (\overline{OE}). The read (RCLK) and write (WCLK) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 100 MHz are achievable.

Depth expansion is possible using one enable input for system control, while the other enable is controlled by expansion logic to direct the flow of data.

Logic Block Diagram



Pin Configuration



Pin Definitions

Signal Name	Description	I/O	Description
$D_0 - 8$	Data Inputs	I	Data Inputs for 9-bit bus
$Q_0 - 8$	Data Outputs	O	Data Outputs for 9-bit bus
$\overline{WEN1}$	Write Enable 1	I	The only write enable when device is configured to have programmable flags. Data is written on a LOW-to-HIGH transition of WCLK when $\overline{WEN1}$ is asserted and FF is HIGH. If the FIFO is configured to have two write enables, data is written on a LOW-to-HIGH transition of WCLK when $\overline{WEN1}$ is LOW and $\overline{WEN2/LD}$ and FF are HIGH.
$\overline{WEN2/LD}$ Dual Mode Pin	Write Enable 2	I	If HIGH at reset, this pin operates as a second write enable. If LOW at reset, this pin operates as a control to write or read the programmable flag offsets. $\overline{WEN1}$ must be LOW and $\overline{WEN2}$ must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the FF is LOW. If the FIFO is configured to have programmable flags, $\overline{WEN2/LD}$ is held LOW to write or lead the programmable flag offsets.
	Load		
$\overline{REN1}, \overline{REN2}$	Read Enable Inputs	I	Enables the device for Read operation.
WCLK	Write Clock	I	The rising edge clocks data into the FIFO when $\overline{WEN1}$ is LOW and $\overline{WEN2/LD}$ is HIGH and the FIFO is not Full. When \overline{LD} is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	The rising edge clocks data out of the FIFO when $\overline{REN1}$ and $\overline{REN2}$ are LOW and the FIFO is not Empty. When $\overline{WEN2/LD}$ is LOW, RCLK reads data out of the programmable flag-offset register.
\overline{EF}	Empty Flag	O	When \overline{EF} is LOW, the FIFO is empty. \overline{EF} is synchronized to RCLK.
\overline{FF}	Full Flag	O	When \overline{FF} is LOW, the FIFO is full. \overline{FF} is synchronized to WCLK.
\overline{PAE}	Programmable Almost Empty	O	When \overline{PAE} is LOW, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO.
\overline{PAF}	Programmable Almost Full	O	When \overline{PAF} is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO.
\overline{RS}	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power-up.
\overline{OE}	Output Enable	I	When \overline{OE} is LOW, the FIFO's data outputs drive the bus to which they are connected. If \overline{OE} is HIGH, the FIFO's outputs are in High Z (high-impedance) state.

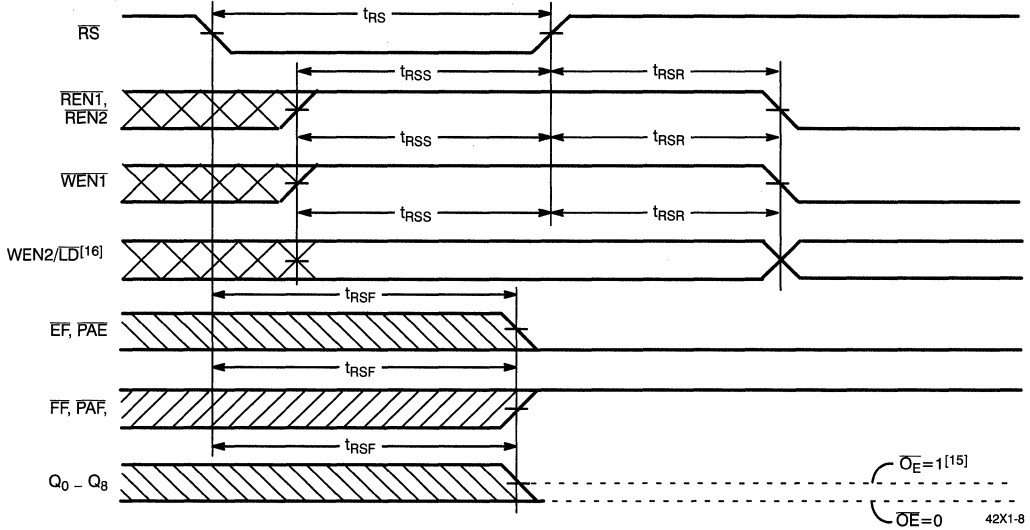
Switching Characteristics Over the Operating Range

Parameter	Description	7C42X1-10		7C42X1-15		7C42X1-25		7C42X1-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _S	Clock Cycle Frequency		100		66.7		40		28.6	ns
t _A	Data Access Time	2	8	2	10	2	15	2	20	ns
t _{CLK}	Clock Cycle Time	10		15		25		35		ns
t _{CLKH}	Clock HIGH Time	4.5		6		10		14		ns
t _{CLKL}	Clock LOW Time	4.5		6		10		14		ns
t _{DS}	Data Set-Up Time	3		4		6		7		ns
t _{DH}	Data Hold Time	0.5		1		1		2		ns
t _{ENS}	Enable Set-Up Time	3		4		6		7		ns
t _{ENH}	Enable Hold Time	0.5		1		1		2		ns
t _{RS}	Reset Pulse Width ^[10]	10		15		25		35		ns
t _{RSS}	Reset Set-Up Time	8		10		15		20		ns
t _{RSR}	Reset Recovery Time	8		10		15		20		ns
t _{RSF}	Reset to Flag and Output Time		10		15		25		35	ns
t _{OLZ}	Output Enable to Output in Low Z ^[11]	0		0		0		0		ns
t _{OE}	Output Enable to Output Valid	3	7	3	8	3	12	3	15	ns
t _{OHZ}	Output Enable to Output in High Z ^[11]	3	7	3	8	3	12	3	15	ns
t _{WFF}	Write Clock to Full Flag		8		10		15		20	ns
t _{REF}	Read Clock to Empty Flag		8		10		15		20	ns
t _{PAF}	Clock to Programmable Almost-Full Flag		8		10		15		20	ns
t _{PAE}	Clock to Programmable Almost-Full Flag		8		10		15		20	ns
t _{SKEW1}	Skew Time between Read Clock and Write Clock for Full Flag	5		6		10		12		ns
t _{SKEW2}	Skew Time between Read Clock and Write Clock for Empty Flag	10		15		18		20		ns

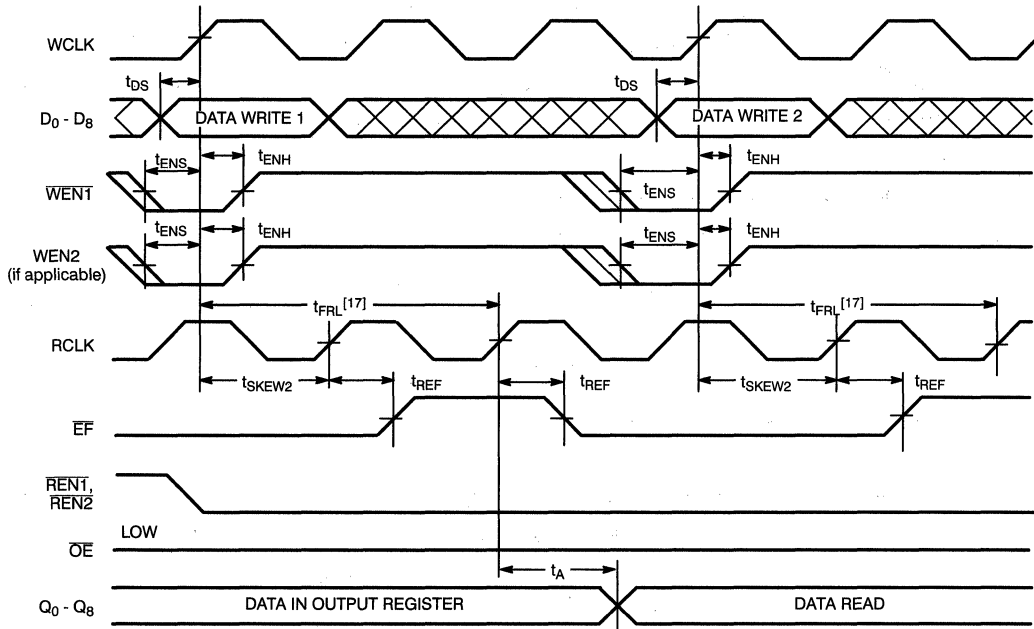
Notes:

10. Pulse widths less than minimum values are not allowed.

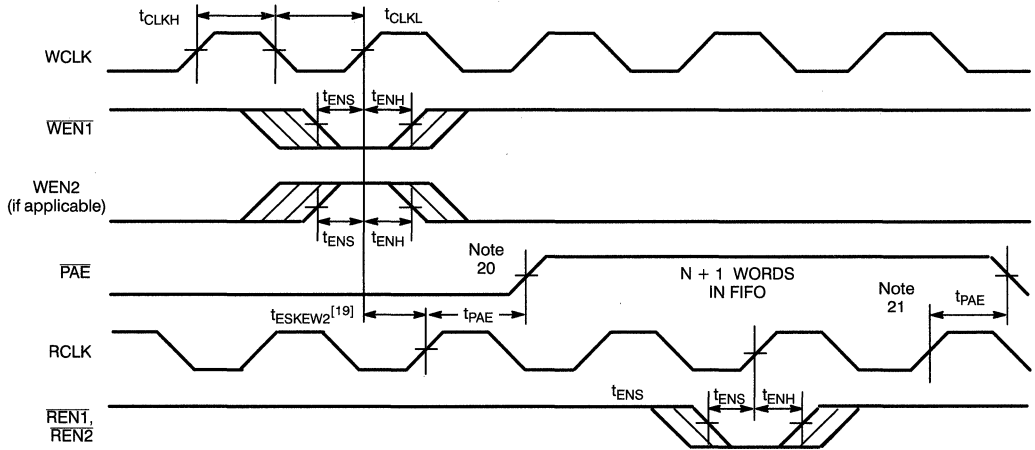
11. Values guaranteed by design, not currently tested.

Switching Waveforms (continued)
Reset Timing^[14]

Notes:

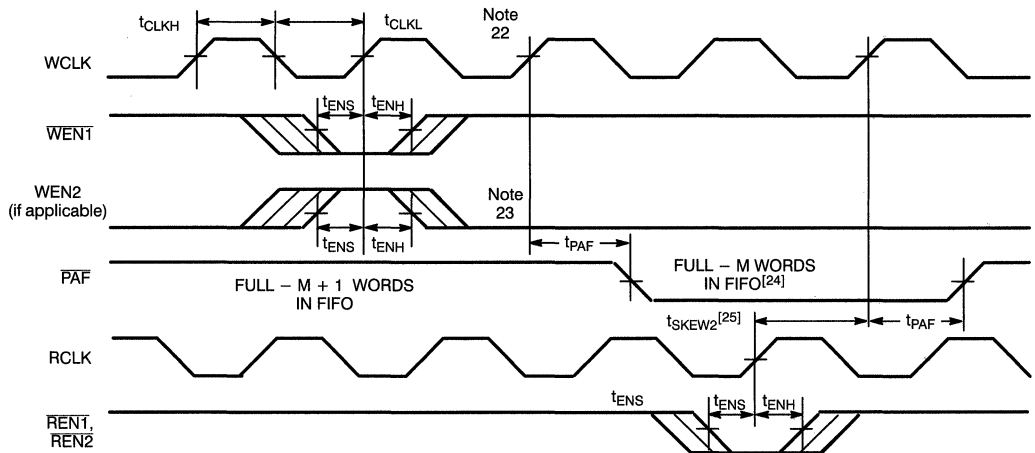
14. The clocks (RCLK, WCLK) can be free-running during reset.
15. After reset, the outputs will be LOW if $\overline{OE} = 0$ and three-state if $\overline{OE} = 1$.
16. Holding WEN2/LD HIGH during reset will make the pin act as a second enable pin. Holding WEN2/LD LOW during reset will make the pin act as a load enable for the programmable flag offset registers.

Switching Waveforms (continued)
Empty Flag Timing


42X1-10

Switching Waveforms (continued)
Programmable Almost Empty Flag Timing


42X1-12

Programmable Almost Full Flag Timing


42X1-13

Notes:

19. t_{SKEW2} is the minimum time between a rising WCLK and a rising RCLK edge for PAE to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW2} , then PAE may not change state until the next RCLK.
20. PAE offset = n.
21. If a read is performed on this rising edge of the read clock, there will be Empty + (n-1) words in the FIFO when PAE goes LOW.
22. If a write is performed on this rising edge of the write clock, there will be Full - (m-1) words of the FIFO when PAF goes LOW.
23. PAF offset = m.
24. 64-m words for CY7C4421, 256-m words in FIFO for CY7C4201, 512-m words for CY7C4211, 1024-m words for CY7C4221, 2048-m words for CY7C4231, 4096-m words for CY7C4241, 8192-m words for CY7C4251.
25. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for PAF to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2} , then PAF may not change state until the next WCLK rising.

is stored in the RAM array sequentially and independently of any on-going read operation.

Write Enable 2/Load (WEN2/LD) – This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows for depth expansion. If Write Enable 2/Load (WEN2/LD) is set active HIGH at Reset (RS=LOW), this pin operates as a second write enable pin.

If the FIFO is configured to have two write enables, when Write Enable (WEN1) is LOW and Write Enable 2/Load (WEN2/LD) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

Programming

When WEN2/LD is held LOW during Reset, this pin is the load (LD) enable for flag offset programming. In this configuration, WEN2/LD can be used to access the four 8-bit offset registers con-

tained in the CY7C42X1 for writing or reading data to these registers.

When the device is configured for programmable flags and both WEN2/LD and WEN1 are LOW, the first LOW-to-HIGH transition of WCLK writes data from the data inputs to the empty offset least significant bit (LSB) register. The second, third, and fourth LOW-to-HIGH transitions of WCLK store data in the empty offset most significant bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when WEN2/LD and WEN1 are LOW. The fifth LOW-to-HIGH transition of WCLK while WEN2/LD and WEN1 are LOW writes data to the empty LSB register again. *Figure 1* shows the registers sizes and default values for the various device types.

It is not necessary to write to all the offset registers at one time. A subset of the offset registers can be written; then by bringing the WEN2/LD input HIGH, the FIFO is returned to normal read and write operation. The next time WEN2/LD is brought LOW, a write operation stores data in the next offset register in sequence.

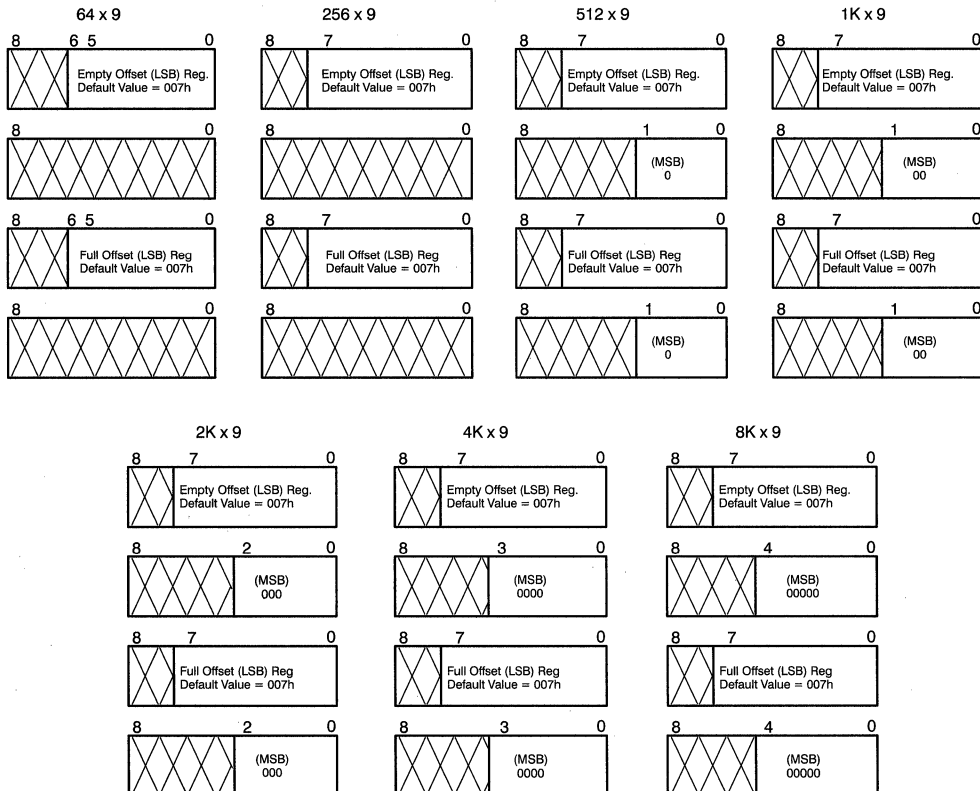


Figure 1. Offset Register Location and Default Values

Width Expansion Configuration

Word width may be increased simply by connecting the corresponding input controls signals of multiple devices. A composite flag should be created for each of the end-point status flags (\overline{EF} and \overline{FF}). The partial status flags (\overline{PAE} and \overline{PAF}) can be detected from any one device. *Figure 2* demonstrates a 18-bit word width by using two CY7C42X1s. Any word width can be attained by adding additional CY7C42X1s.

When the CY7C42X1 is in a Width Expansion Configuration, the Read Enable ($\overline{REN2}$) control input can be grounded (See *Figure 2*). In this configuration, the Write Enable 2/Load ($\overline{WEN2/LD}$) pin is set to LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

Flag Operation

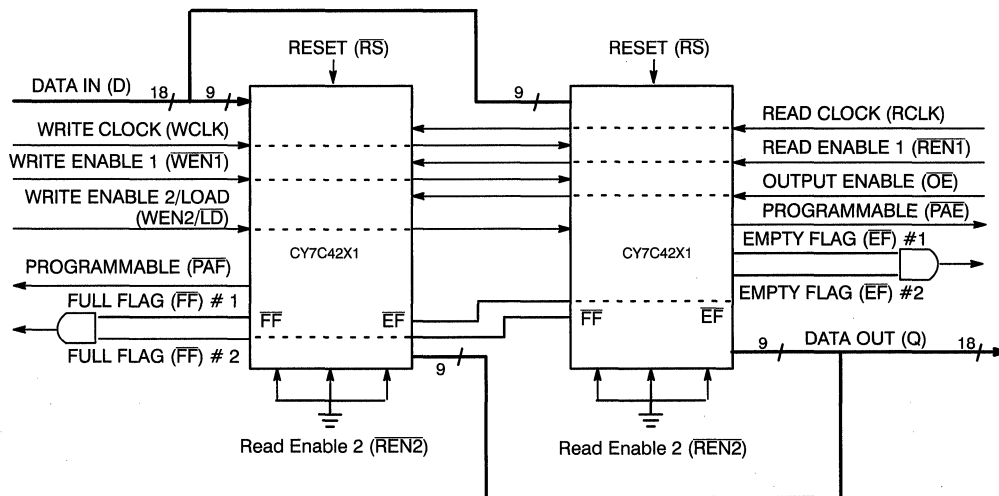
The CY7C42X5 devices provide five flag pins to indicate the condition of the FIFO contents. Empty, Full, PAE, and PAF are synchronous.

Full Flag

The Full Flag (\overline{FF}) will go LOW when device is full. Write operations are inhibited whenever \overline{FF} is LOW regardless of the state of $\overline{WEN1}$ and $\overline{WEN2/LD}$. \overline{FF} is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag (\overline{EF}) will go LOW when the device is empty. Read operations are inhibited whenever \overline{EF} is LOW, regardless of the state of $\overline{REN1}$ and $\overline{REN2}$. \overline{EF} is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.



42X1-16

Figure 2. Block Diagram of 64 x 18/256 x 18/512 x 18/1024 x 18/2048 x 18/4096 x 18/8192 x 18 Synchronous FIFO Memory Used in a Width Expansion Configuration



Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4211-10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4211-10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4211-10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4211-10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4211-15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4211-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4211-15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4211-15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4211-25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4211-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4211-25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4211-25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4211-35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4211-35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4211-35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4211-35JI	J65	32-Lead Plastic Leaded Chip Carrier	

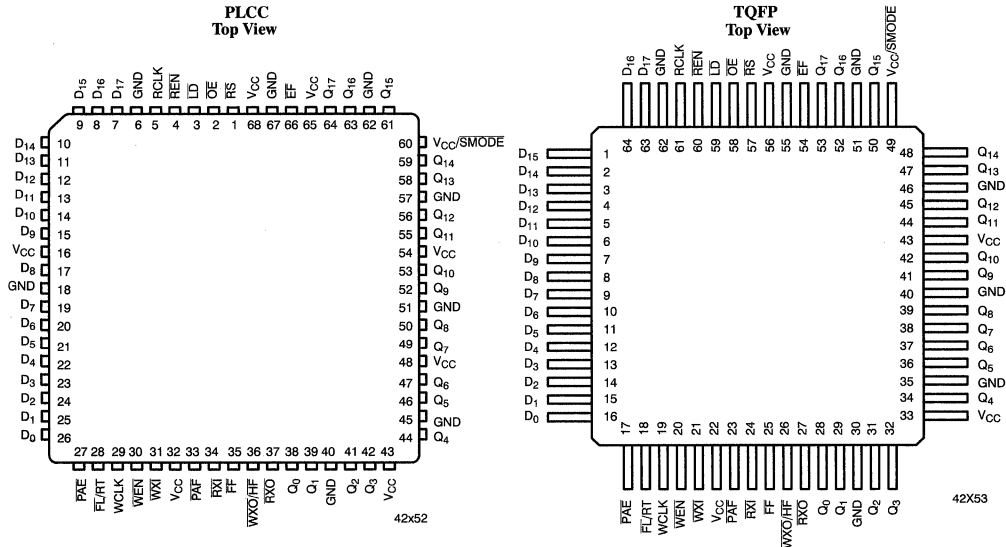
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4221-10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4221-10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4221-10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4221-10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4221-15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4221-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4221-15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4221-15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4221-25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4221-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4221-25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4221-25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4221-35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4221-35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4221-35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4221-35JI	J65	32-Lead Plastic Leaded Chip Carrier	



Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4251-10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4251-10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4251-10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4251-10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4251-15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4251-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4251-15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4251-15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4251-25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4251-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4251-25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4251-25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4251-35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4251-35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4251-35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4251-35JI	J65	32-Lead Plastic Leaded Chip Carrier	

Document #: 38-00419

Pin Configurations

Functional Description (continued)

The CY7C42X5 provides five status pins. These pins are decoded to determine one of five states: Empty, Almost Empty, Half Full, Almost Full, and Full (see *Table 2*). The Half Full flag shares the $WX\bar{O}$ pin. This flag is valid in the standalone and width-expansion configurations. In the depth expansion, this pin provides the expansion output (WXO) information that is used to signal the next FIFO when it will be activated.

The Empty and Full flags are synchronous, i.e., they change state relative to either the read clock (RCLK) or the write clock

(WCLK). When entering or exiting the Empty states, the flag is updated exclusively by the RCLK. The flag denoting Full states is updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags will remain valid from one clock cycle to the next. As mentioned previously, the Almost Empty/Almost Full flags become synchronous if the $V_{CC}/SMODE$ is tied to V_{SS} . All configurations are fabricated using an advanced 0.65μ N-Well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings.

Selection Guide

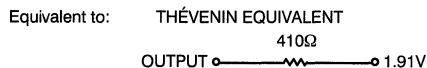
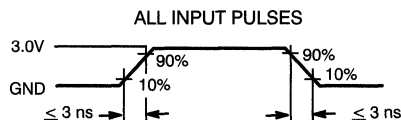
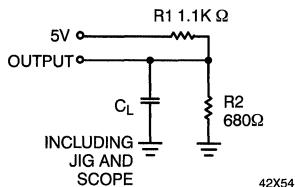
		7C42X5-10	7C42X5-15	7C42X5-25	7C42X5-35	
Maximum Frequency (MHz)		100	66.7	40	28.6	
Maximum Access Time (ns)		8	10	15	20	
Minimum Cycle Time (ns)		10	15	25	35	
Minimum Data or Enable Set-Up (ns)		3	4	6	7	
Minimum Data or Enable Hold (ns)		0.5	1	1	2	
Maximum Flag Delay (ns)		8	10	15	20	
Operating Current (I_{CC2}) (mA)	Commercial	100	100	100	100	
	Industrial	120	120	120	120	
	CY7C4425	CY7C4205	CY7C4215	CY7C4225	CY7C4235	CY7C4245
Density	64 x 18	256 x 18	512 x 18	1K x 18	2K x 18	4K x 18

Electrical Characteristics Over the Operating Range^[2]

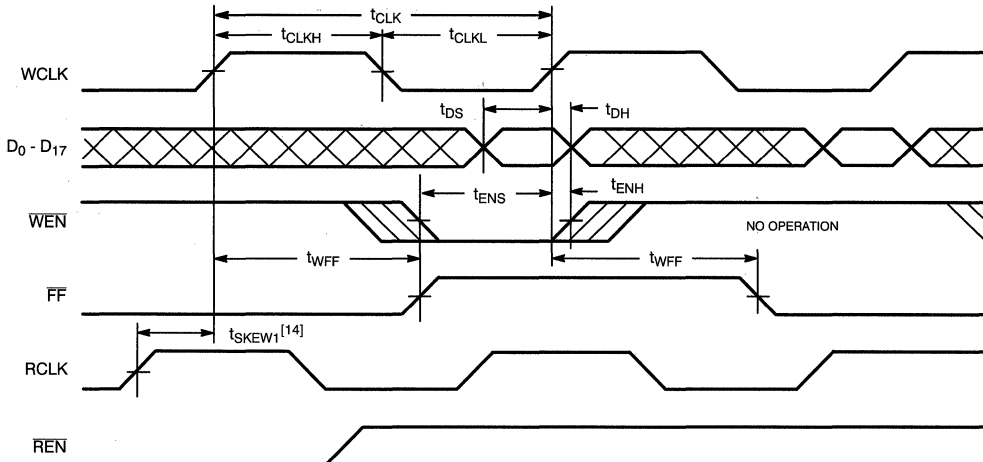
Parameter	Description	Test Conditions	7C42X5-10		7C42X5-15		7C42X5-25		7C42X5-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -2.0 mA	2.4		2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V _{IH} ^[3]	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL} ^[3]	Input LOW Voltage		-3.0	0.8	-3.0	0.8	-3.0	0.8	-3.0	0.8	V
I _{IX}	Input Leakage Current	V _{CC} = Max.	-10	+10	-10	+10	-10	+10	-10	+10	μA
I _{OS} ^[4]	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = GND	-90		-90		-90		-90		mA
I _{OZL} I _{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, V _{SS} < V _O < V _{CC}	-10	+10	-10	+10	-10	+10	-10	+10	μA
I _{CC1} ^[5]	Operating Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	230		200		115		90	mA
			Ind	250		220		135		110	mA
I _{CC2} ^[6]	Operating Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	100		100		100		100	mA
			Ind	120		120		120		120	mA
I _{SB} ^[7]	Standby Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	30		28		25		25	mA
			Ind	40		38		35		35	mA

Capacitance^[8]

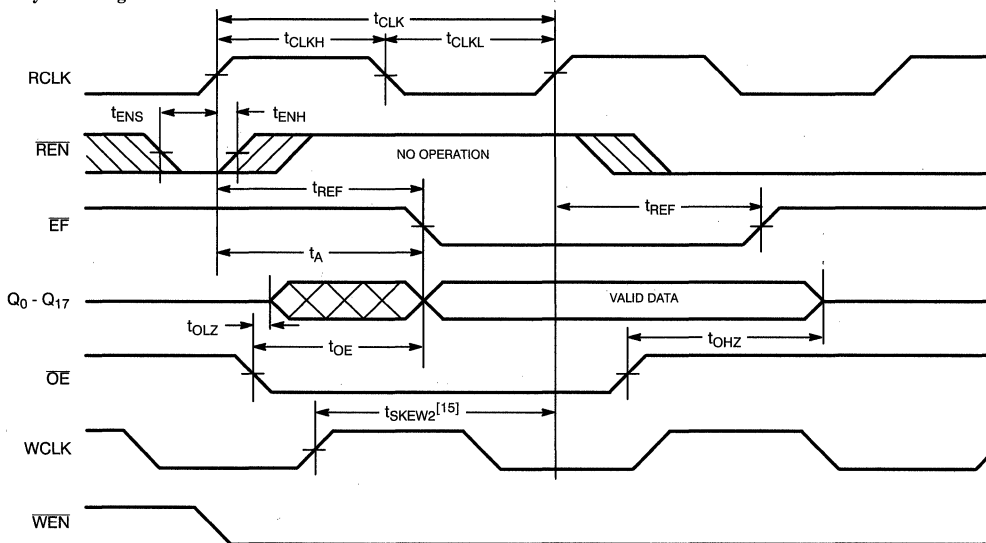
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	5	pF
C _{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms^[9, 10]

Notes:

- See the last page of this specification for Group A subgroup testing information.
- The V_{IH} and V_{IL} specifications apply for all inputs except \overline{WXI} , \overline{RXI} . The \overline{WXI} , \overline{RXI} pin is not a TTL input. It is connected to either \overline{RXO} , \overline{WXO} of the previous device or V_{SS}.
- Test no more than one output at a time for not more than one second.
- Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at f_{MAX}/2. Outputs are unloaded.
- Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
- All input signals are connected to V_{CC}. All outputs are unloaded.
- Tested initially and after any design or process changes that may affect these parameters.
- C_L = 30 pF for all AC parameters except for t_{OZH}.
- C_L = 5 pF for t_{OZL}.

Switching Waveforms
Write Cycle Timing


42X56

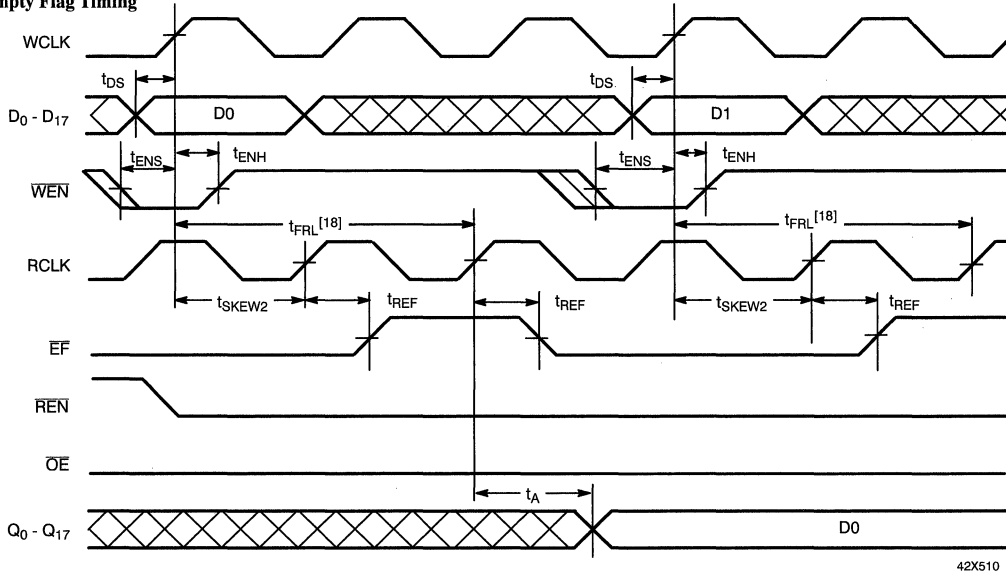
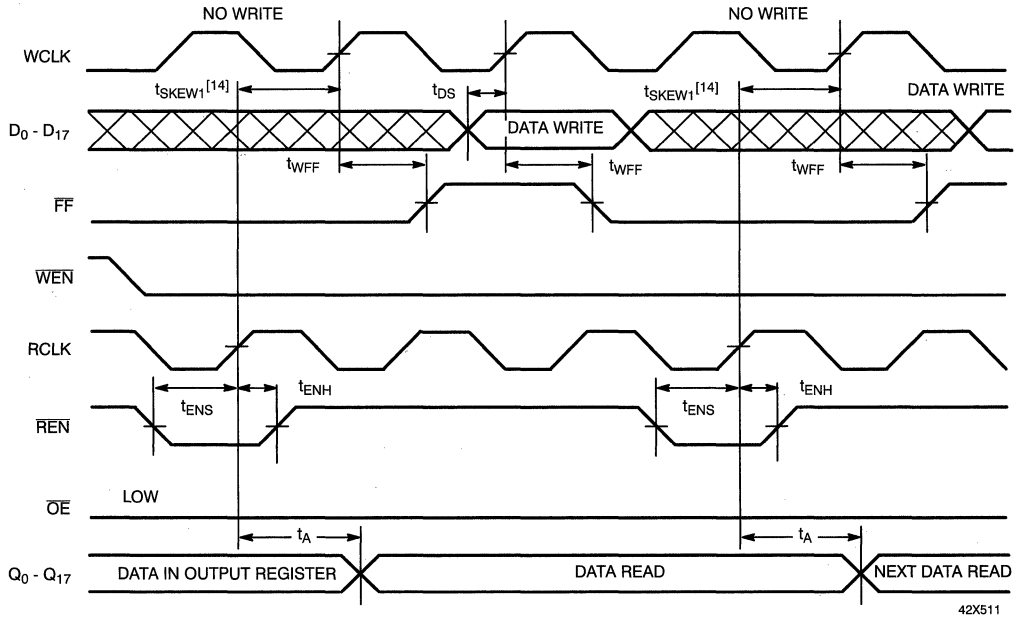
Read Cycle Timing


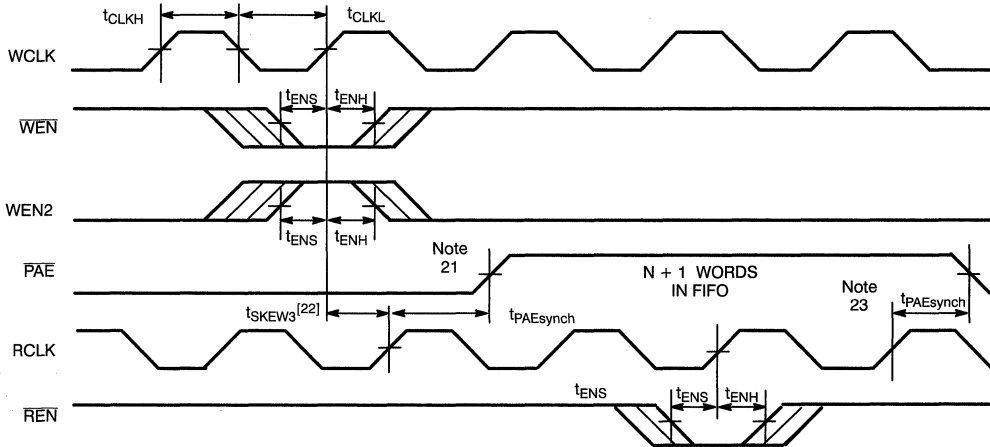
42X57

Notes:

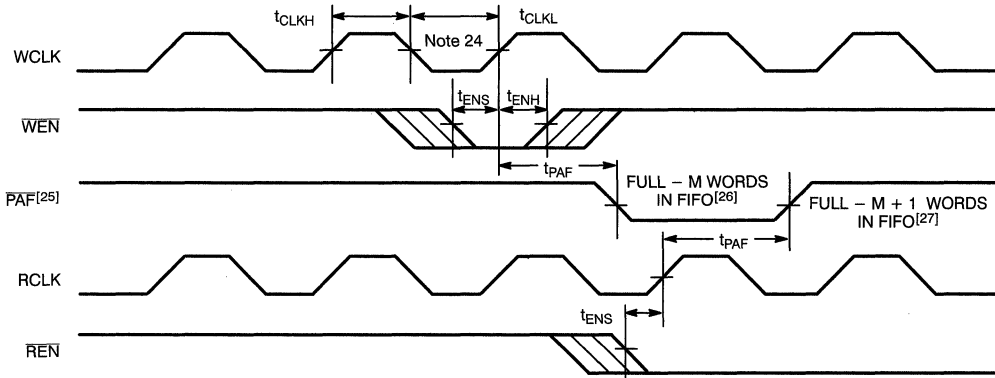
14. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that FF will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1} , then FF may not change state until the next WCLK edge.

15. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that EF will go HIGH during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2} , then EF may not change state until the next RCLK edge.

Switching Waveforms (continued)
Empty Flag Timing

Full Flag Timing


Switching Waveforms (continued)
Programmable Almost Empty Flag Timing (applies only in SMODE (SMODE is LOW))


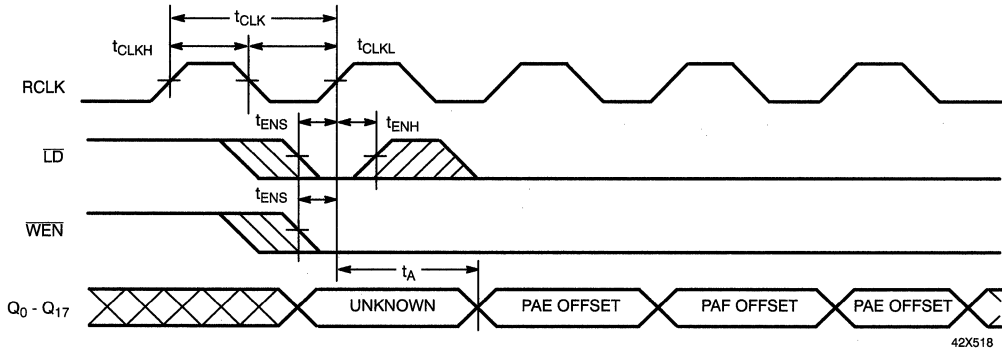
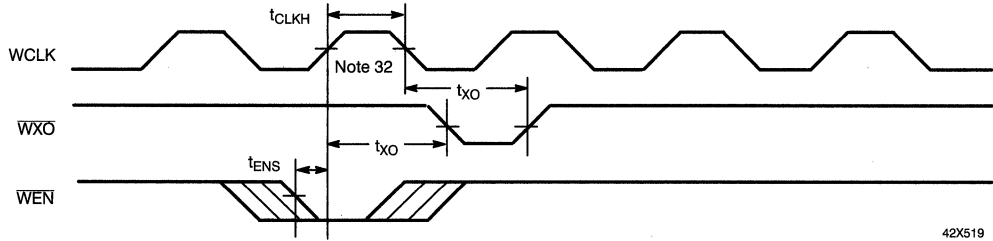
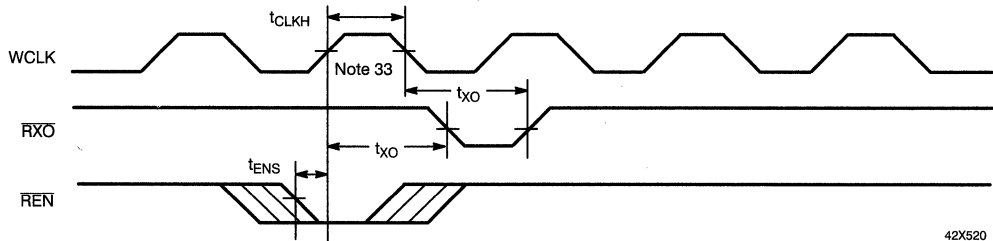
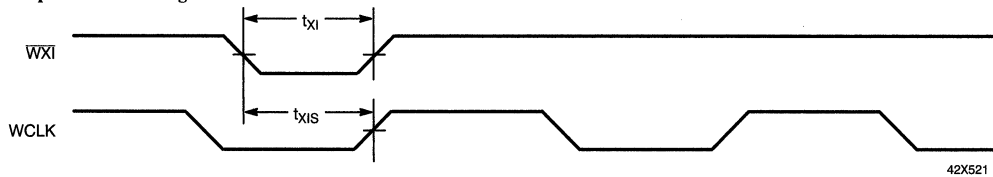
42X514

Programmable Almost Full Flag Timing


42X515

Notes:






21. PAE offset = n.
22. t_{SKEW3} is the minimum time between a rising WCLK and a rising RCLK edge for PAE to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW3} , then PAE may not change state until the next RCLK.
23. If a read is performed on this rising edge of the read clock, there will be Empty + (n-1) words in the FIFO when PAE goes LOW.
24. PAF offset = m. Number of data words written into FIFO already = 64 - m + 1 for the CY7C4425, 256 - m + 1 for the CY7C4205, 512 - m + 1 for the CY7C4215, 1024 - m + 1 for the CY7C4225, 2048 - m + 1 for the CY7C4235, and 4096 - m + 1 for the CY7C4245.
25. PAF is offset = m.
26. 64 - m words in CY7C4425, 256 - m words in CY7C4205, 512 - m words in CY7C4215, 1024 - m words in CY7C4225, 2048 - m words in CY7C4235, and 4096 - m words in CY7C4245.
27. 64 - m + 1 words in CY7C4425, 256 - m + 1 words in CY7C4205, 512 - m + 1 words in CY7C4215, 1024 - m + 1 words in CY7C4225, 2048 - m + 1 words in CY7C4235, and 4096 - m + 1 words in CY7C4245.

Switching Waveforms (continued)
Read Programmable Registers

Write Expansion Out Timing

Read Expansion Out Timing

Write Expansion In Timing

Notes:

32. Write to Last Physical Location.

33. Read from Last Physical Location.

Table 1. Write Offset Register

LD	WEN	WCLK ^[37]	Selection
0	0		Writing to offset registers: Empty Offset  Full Offset
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

Flag Operation

The CY7C42X5 devices provide five flag pins to indicate the condition of the FIFO contents. Empty and Full are synchronous. PAE and PAF are synchronous if V_{CC}/SMODE is tied to V_{SS}.

Full Flag

The Full Flag (\overline{FF}) will go LOW when device is Full. Write operations are inhibited whenever \overline{FF} is LOW regardless of the state of WEN. \overline{FF} is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag (\overline{EF}) will go LOW when the device is empty. Read operations are inhibited whenever \overline{EF} is LOW, regardless of the state of REN. \overline{EF} is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

Programmable Almost Empty/Almost Full Flag

The CY7C42X5 features programmable Almost Empty and Almost Full Flags. Each flag can be programmed (described in the Programming section) a specific distance from the corresponding boundary flags (Empty or Full). When the FIFO contains the number of words or fewer for which the flags have been programmed, the PAF or PAE will be asserted, signifying that the FIFO is either Almost Full or Almost Empty. See Table 2 for a description of programmable flags.

When the SMODE pin is tied LOW, the \overline{PAF} flag signal transition is caused by the rising edge of the write clock and the PAE flag transition is caused by the rising edge of the read clock.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit (RT) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred since the last \overline{RS} cycle. A HIGH pulse on RT resets the internal read pointer to the first physical location of the FIFO. WCLK and RCLK may be free running but must be disabled during and t_{RTR} after the retransmit pulse. With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of RT are transmitted also.

The full depth of the FIFO can be repeatedly retransmitted.

Table 2. Flag Truth Table

Number of Words in FIFO			\overline{FF}	\overline{PAF}	\overline{HF}	\overline{PAE}	\overline{EF}
7C4425 – 64 x 18	7C4205 – 256 x 18	7C4215 – 512 x 18					
0	0	0	H	H	H	L	L
1 to $n^{[38]}$	1 to $n^{[38]}$	1 to $n^{[38]}$	H	H	H	L	H
$(n+1)$ to 32	$(n+1)$ to 128	$(n+1)$ to 256	H	H	H	H	H
33 to $(64 - (m+1))$	129 to $(256 - (m+1))$	257 to $(512 - (m+1))$	H	H	L	H	H
$(64 - m)^{[39]}$ to 63	$(256 - m)^{[39]}$ to 255	$(512 - m)^{[39]}$ to 511	H	L	L	H	H
64	256	512	L	L	L	H	H

Number of Words in FIFO			\overline{FF}	\overline{PAF}	\overline{HF}	\overline{PAE}	\overline{EF}
7C4225 – 1K x 18	7C4235 – 2K x 18	7C4245 – 4K x 18					
0	0	0	H	H	H	L	L
1 to $n^{[38]}$	1 to $n^{[38]}$	1 to $n^{[38]}$	H	H	H	L	H
$(n+1)$ to 512	$(n+1)$ to 1024	$(n+1)$ to 2048	H	H	H	H	H
513 to $(1024 - (m+1))$	1025 to $(2048 - (m+1))$	2049 to $(4096 - (m+1))$	H	H	L	H	H
$(1024 - m)^{[39]}$ to 1023	$(2048 - m)^{[39]}$ to 2047	$(4096 - m)^{[39]}$ to 4095	H	L	L	H	H
1024	2048	4096	L	L	L	H	H

Notes:

37. The same selection sequence applies to reading from the registers. REN is enabled and read is performed on the LOW-to-HIGH transition of RCLK.
38. n = Empty Offset (Default Values: CY7C4425 n = 7, CY7C4205 n = 31, CY7C4215 n = 63, CY7C4225/7C4235/7C4245 n = 127).
39. m = Full Offset (Default Values: CY7C4425 n = 7, CY7C4205 n = 31, CY7C4215 n = 63, CY7C4225/7C4235/7C4245 n = 127).

**Depth Expansion Configuration
(with Programmable Flags)**

The CY7C42X5 can easily be adapted to applications requiring more than 64/256/512/1024/2048/4096 words of buffering. Figure 2 shows Depth Expansion using three CY7C42X5s. Maximum depth is limited only by signal loading. Follow these steps:

1. The first device must be designated by grounding the First Load (FL) control input.
2. All other devices must have FL in the HIGH state.
3. The Write Expansion Out (WXO) pin of each device must be tied to the Write Expansion In (WXI) pin of the next device.
4. The Read Expansion Out (RXO) pin of each device must be tied to the Read Expansion In (RXI) pin of the next device.
5. All Load (LD) pins are tied together.
6. The Half-Full Flag (HF) is not available in the Depth Expansion Configuration.
7. EF, FF, PAE, and PAF are created with composite flags by ORing together these respective flags for monitoring. The composite PAE and PAF flags are not precise.

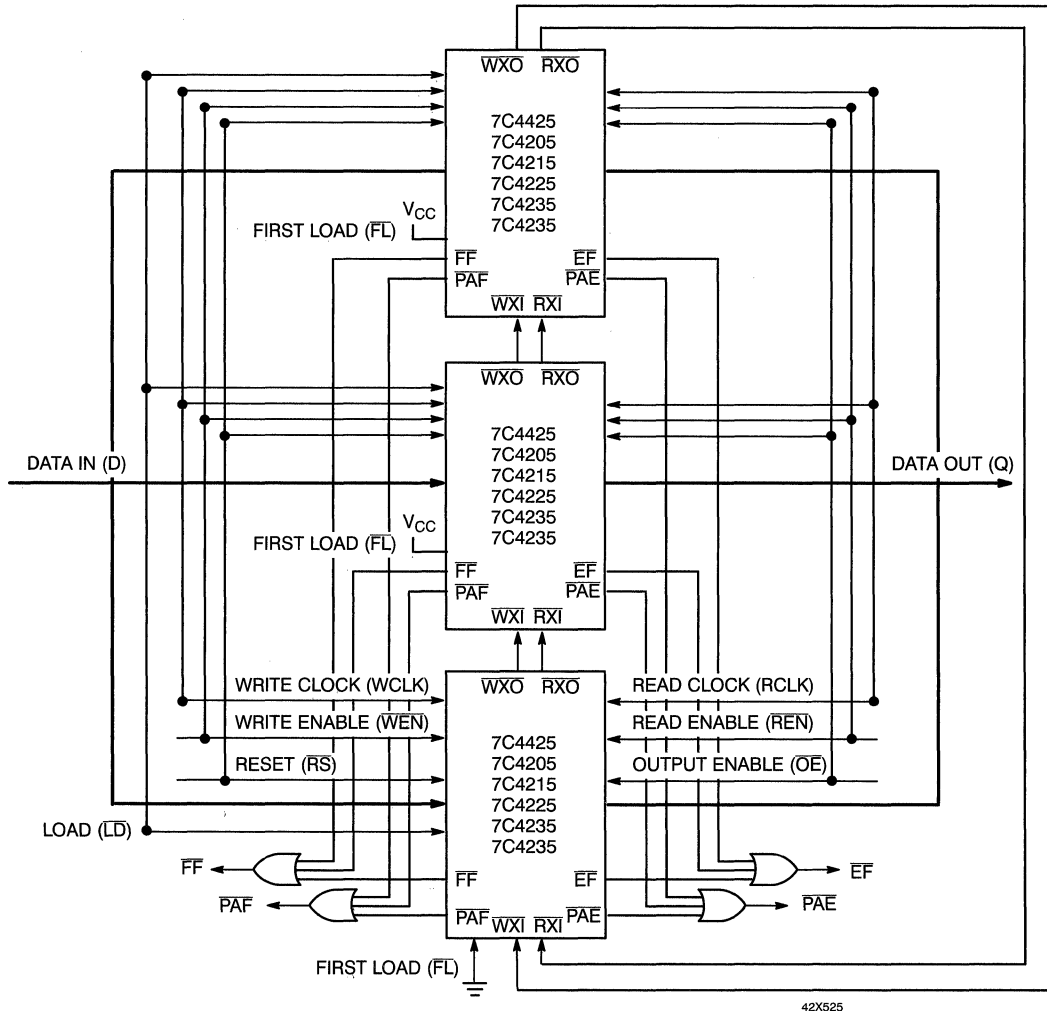


Figure 2. Block Diagram of 192 x 18/768 x 18/1536 x 18/3072 x 18/12288 x 18 Synchronous FIFO Memory with Programmable Flags used in Depth Expansion Configuration



Ordering Information (continued)

512 x 18

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4215-10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4215-10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4215-10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4215-10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4215-15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4215-15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4215-15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4215-15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4215-25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4215-25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4215-25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4215-25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4215-35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4215-35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4215-35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4215-35JI	J81	68-Lead Plastic Leaded Chip Carrier	

1K x 18

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4225-10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4225-10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4225-10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4225-10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4225-15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4225-15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4225-15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4225-15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4225-25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4225-25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4225-25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4225-25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4225-35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4225-35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4225-35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4225-35JI	J81	68-Lead Plastic Leaded Chip Carrier	



Bidirectional 2K x 9 FIFO

Features

- 2048 x 9 FIFO buffer memory
- Bidirectional operation
- High-speed 28.5-MHz asynchronous reads and writes
- Simple control interface
- Registered and transparent bypass modes
- Flags indicate Empty, Full, and Half Full conditions
- 5V ± 10% supply
- Available in 300-mil DIP, PLCC, LCC, and SOJ packages
- TTL compatible

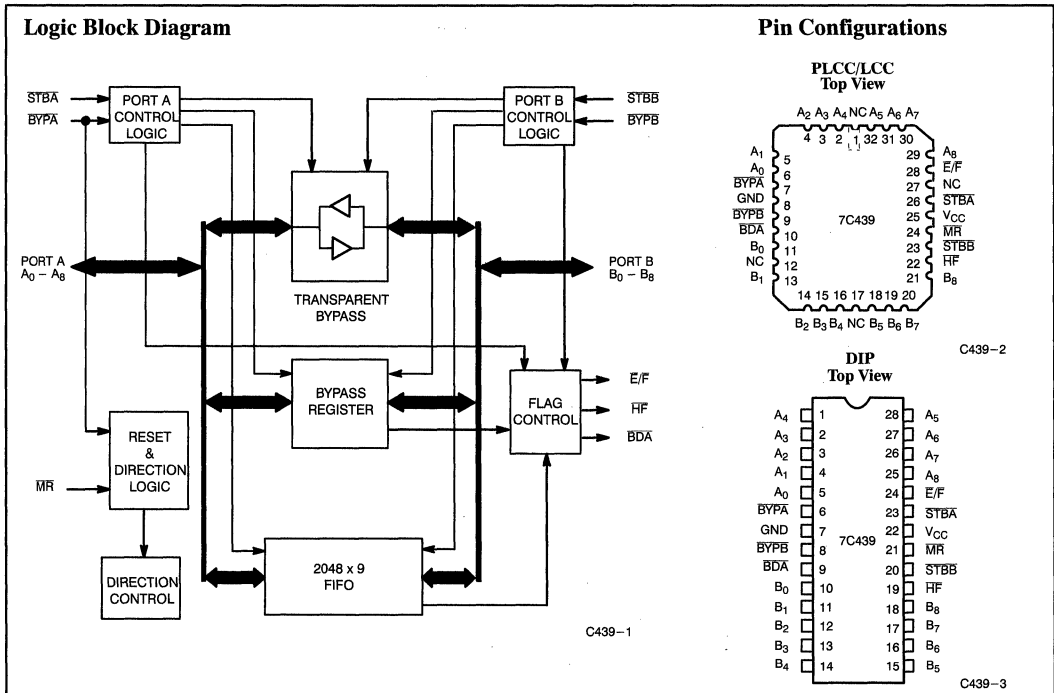
Functional Description

The CY7C439 is a 2048 x 9 FIFO memory capable of bidirectional operation. As the term first-in first-out (FIFO) implies, data becomes available to the output port in the same order that it was presented to the input port. There are two pins that indicate the amount of data contained within the FIFO block— $\overline{E}/\overline{F}$ (Empty/Full) and $\overline{H}/\overline{F}$ (Half Full). These pins can be decoded to determine one of four states. Two 9-bit data ports are provided. The direction selected for the FIFO determines the input and output ports. The FIFO direction can be programmed by the user at any time through the use of the reset pin (\overline{MR}) and the bypass/direction pin (\overline{BYPA}). There are no control or status registers on the CY7C439, making the part simple to use

while meeting the needs of the majority of bidirectional FIFO applications.

FIFO read and write operations may occur simultaneously, and each can occur at up to 28.5 MHz. The port designated as the write port drives its strobe pin (\overline{STBX} , X = A or B) LOW to initiate the write operation. The port designated as the read port drives its strobe pin LOW to initiate the read operation. Output port pins go to a high-impedance state when the associated strobe pin is HIGH. All normal FIFO operations require the bypass control pin (\overline{BYPX} , X = A or B) to remain HIGH.

In addition to the FIFO, two other data paths are provided: registered bypass and transparent bypass. Registered bypass can be considered as a single-word FIFO in the reverse direction to the main FIFO. The



Selection Guide

	7C439-25	7C439-30	7C439-40	7C439-65
Frequency (MHz)	28.5	25	20	12.5
Maximum Access Time (ns)	25	30	40	65
Maximum Operating Current (mA)	Commercial	147	130	115
	Military	170	160	145

Electrical Characteristics Over the Operating Range^[2]

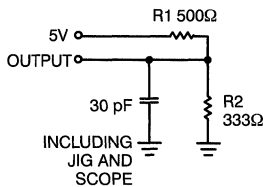
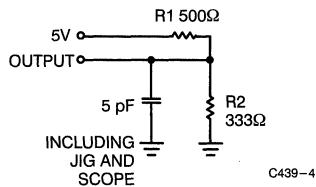
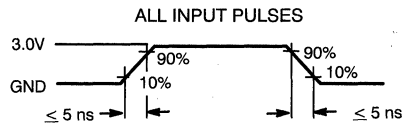
Parameter	Description	Test Conditions	7C439-25		7C439-30		7C439-40		7C439-65		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -2.0 mA	2.4		2.4		2.4		2.4		V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V	
V _{IH}	Input HIGH Voltage		Com ¹	2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
			Mil			2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage		-3.0	0.8	-3.0	0.8	-3.0	0.8	-3.0	0.8	V	
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	-10	+10	-10	+10	μA	
I _{OZ}	Output Leakage Current	STB \bar{X} ≥ V _{IH} , GND ≤ V _O ≤ V _{CC}	-10	+10	-10	+10	-10	+10	-10	+10	μA	
I _{CC}	Operating Current	V _{CC} = Max., I _{OUT} = 0 mA	Com ¹ ^[3]	147		140		130		115	mA	
			Mil ^[4]			170		160		145		
I _{SB1}	Standby Current	All Inputs = V _{IH} Min.	Com ¹	40		40		40		40	mA	
			Mil			45		45		45		
I _{SB2}	Power-Down Current	All Inputs V _{CC} - 0.2V	Com ¹	20		20		20		20	mA	
			Mil			25		25		25		
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND		-90		-90		-90		-90	mA	

Capacitance^[6]

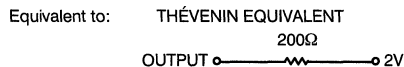
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 4.5V	8	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

- See the last page of this specification for Group A subgroup testing information.
- I_{CC} (commercial) = 115 mA + [(f̄ - 12.5) · 2 mA/MHz] for f̄ ≥ 12.5 MHz
where f̄ = the larger of the write or read operating frequency.
- I_{CC} (military) = 145 mA + [(f̄ - 12.5) · 2 mA/MHz] for f̄ ≥ 12.5 MHz
where f̄ = the larger of the write or read operating frequency.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveform

(a) Normal Load

(b) High-Z Load


C439-5

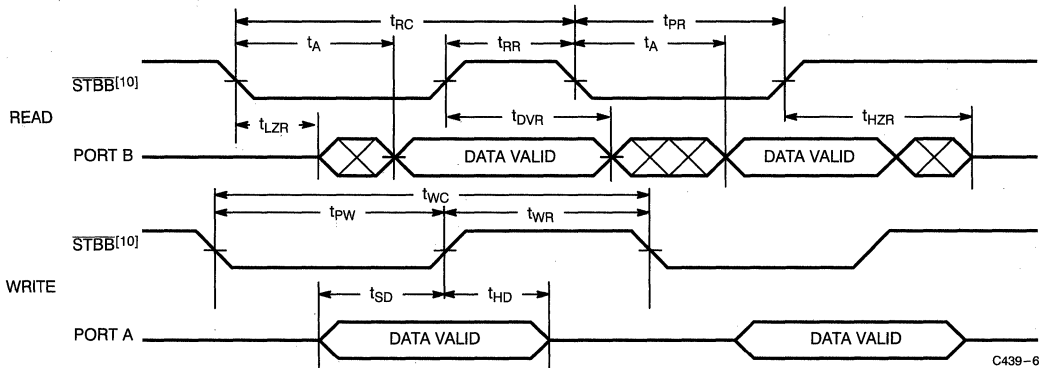


Switching Characteristics Over the Operating Range^[2, 7] (continued)

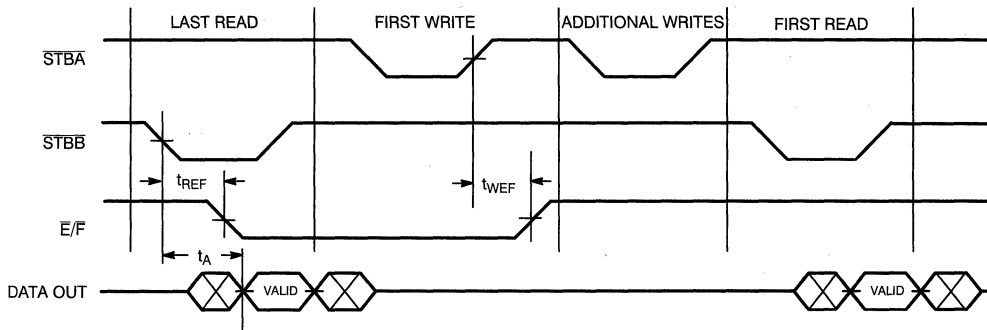
Parameter	Description	7C439-25		7C439-30		7C439-40		7C439-65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{TPD}^{[8, 9]}$	STBX LOW to Data Valid		20		20		30		55	ns
t_{DL}	Transparent Propagation Delay		20		20		25		30	ns
$t_{ESD}^{[8, 9]}$	STBX LOW to High Z		18		20		25		30	ns
$t_{EBD}^{[8, 9]}$	BYPX LOW to High Z		18		20		25		30	ns
t_{EDS}	STBX HIGH to Low Z		18		20		25		30	ns
t_{EDB}	BYPX HIGH to Low Z		18		20		25		30	ns
t_{BPW}	BYPX Pulse Width (Trans.)	25		30		40		65		ns
t_{TSP}	STBX Pulse Width (Trans.)	20		20		30		55		ns
$t_{BLZ}^{[8, 9]}$	BYPX LOW to Low Z (Read)	10		10		10		10		ns
t_{BDV}	BYPX HIGH to Data Invalid (Read)	3		3		3		3		ns
t_{WHF}	STBX LOW to HF LOW (Write)		35		40		50		80	ns
t_{RHF}	STBX HIGH to HF HIGH (Read)		35		40		50		80	ns
t_{RAE}	Effective Read from Write HIGH		25		30		35		60	ns
t_{RPE}	Effective Read Pulse Width after E/F HIGH	25		30		40		65		ns
t_{WAF}	Effective Write from Read HIGH		25		30		35		60	ns
t_{WPF}	Effective Write Pulse Width after E/F HIGH	25		30		40		65		ns
t_{BSU}	Bypass Data Set-Up Time	15		18		20		30		ns
t_{BHL}	Bypass Data Hold Time	0		0		0		10		ns

Notes:

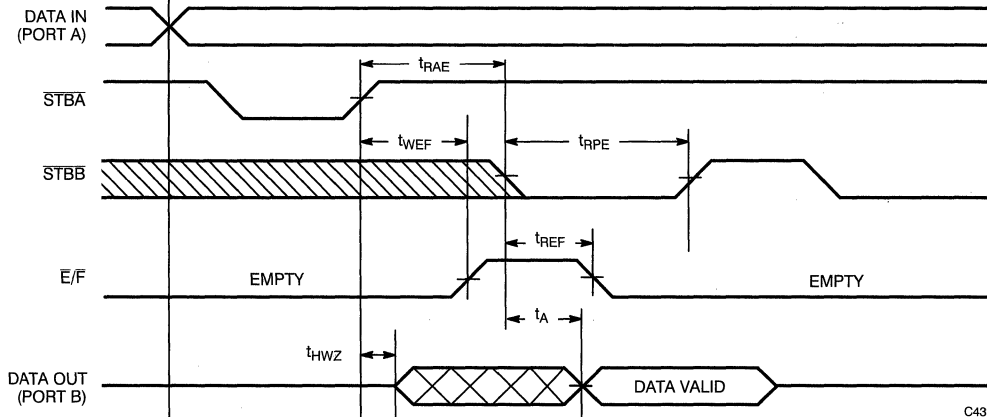
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance as in part (a) of AC Test Loads, unless otherwise specified.
- t_{DVR} , t_{BDV} , t_{HZR} , t_{TBD} , t_{BHZ} , t_{EBD} , t_{ESD} , t_{TSD} , t_{LZR} , t_{HWZ} , and t_{BLZ} use capacitance loading as in part (b) of AC Test Loads.
- t_{HZR} , t_{TBD} , t_{BHZ} , t_{EBD} , t_{ESD} , and t_{TSD} transition is measured at +500 mV from V_{OL} and -500 mV from V_{OH} . t_{DVR} and t_{BDV} transition is measured at the 1.5V level. t_{LZR} , t_{HWZ} , and t_{BLZ} transition is measured at ± 100 mV from the steady state.

Switching Waveforms
Asynchronous Read and Write Timing Diagram


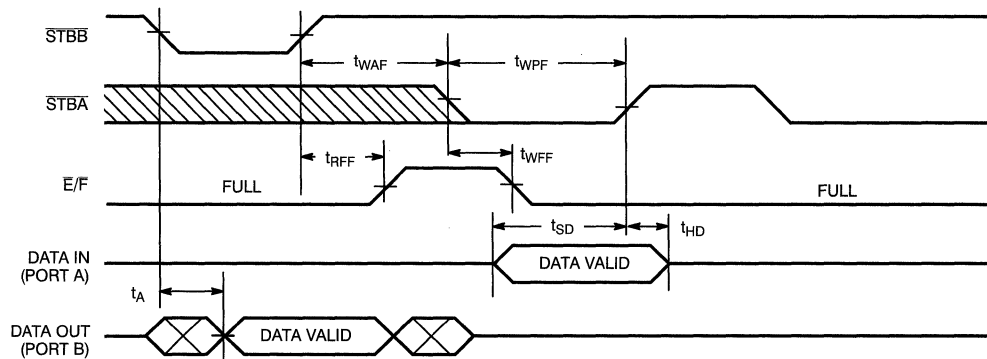
C439-6

Switching Waveforms (continued)
Last Read to First Write Empty/Full Flag Timing Diagram^[11]


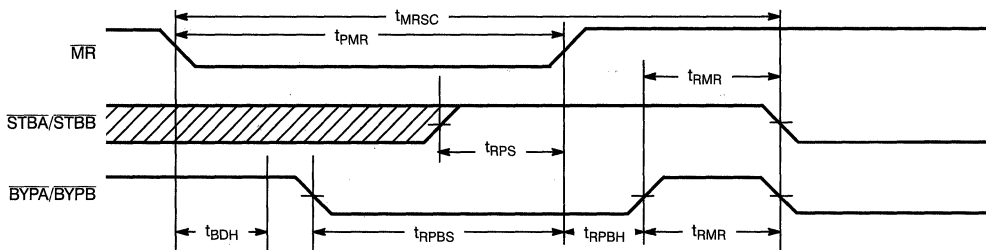
C439-10

Empty/Full Flag and Read Bubble-Through Mode Timing Diagram^[11]


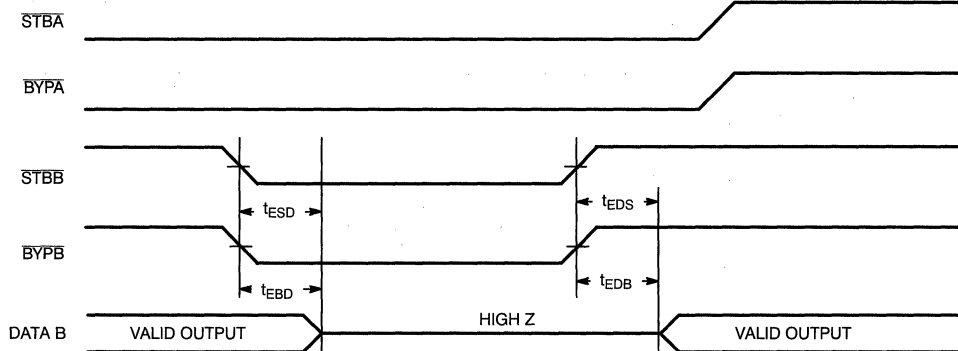
C439-11

Empty/Full Flag and Write Bubble-Through Mode Timing Diagram^[11]


C439-12

Switching Waveforms (continued)
Test Mode Timing Diagram


C439-16

Exception Condition Timing Diagram^[14]


C439-17

Architecture

The CY7C439 consists of a 2048 by 9-bit dual-ported RAM array, a read pointer, a write pointer, data switching circuitry, buffers, a bypass register, control signals (STBA, STBB, BYPA, BYPB, MR), and flags (E/F, HF, BDA).

Operation at Power-On

Upon power-up, the FIFO must be reset with a Master Reset (MR) cycle. During an MR cycle, the user can initialize the device by choosing the direction of FIFO operation (see Table 1). There is a minimum LOW period for MR, but no maximum time. The state of BYPA is latched internally by the rising edge of MR and used to determine the direction of subsequent data operations.

Resetting the FIFO

During the reset condition (see Table 1), the FIFO three-states the data ports, sets BDA and HF HIGH, E/F LOW, and ignores the state of BYPA/B and STBA/B. The bypass registers are initialized to zero. During this time the user is expected to set the direction of the FIFO by driving BYPA HIGH or LOW, and BYPB, STBA, and STBB HIGH. If BYPA is LOW (selecting direction B>A), the FIFO will then remain in a reset condition until the user terminates the reset operation by driving BYPA HIGH. If BYPA is HIGH (selecting direction A>B), the reset condition ter-

minates after the rising edge of MR. The entire reset phase can be accomplished in one cycle time of t_{RC}.

FIFO Operation

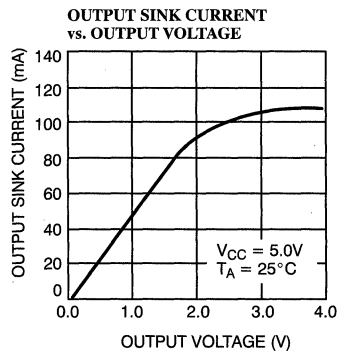
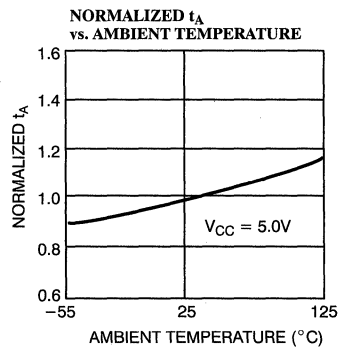
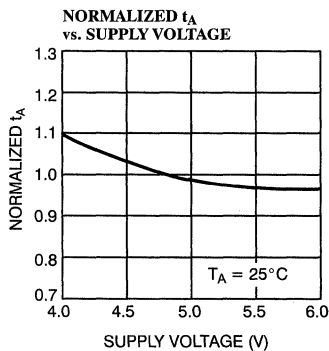
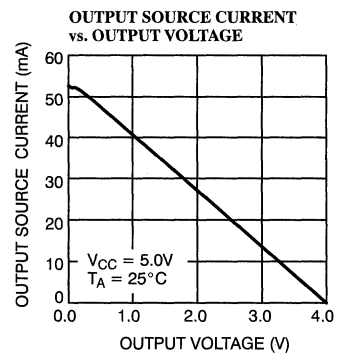
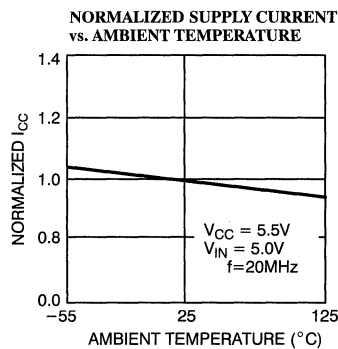
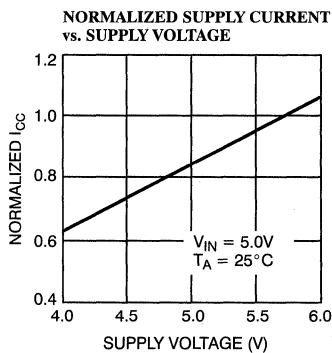
The operation of the FIFO requires only one control pin per port (STBX). The user determines the direction of the FIFO data flow by initiating an MR cycle (see Table 1), which clears the FIFO and bypass register and sets the data path and control signal multiplexers. The bypass register is configured in the opposite direction to the FIFO data flow. The FIFO direction can be reversed at any time by initiating another MR cycle. Data is written into the FIFO on the rising edge of the input, STBX, and read from the FIFO by a low level at the output, STBX. The two ports are asynchronous and independent. If the user attempts to read the FIFO when it is empty, no action takes place (the read pointer is not incremented) until the other port writes to the FIFO. Then a bubble-through read takes place, in which the read strobe is generated internally and the data becomes available at the read port shortly thereafter if the read strobe (STBX) is still LOW. Similarly, for an attempted write operation when the FIFO is full, no internal operation takes place until the other port performs a read operation, at which time the bubble-through write is performed if the write strobe (STBX) is still LOW.

Table 3. Exception Conditions: Operation Not Defined

Direction	STBA	BYPA	STBB	BYBP	Action
X	0	1	0	0	Data Buses High Impedance
X	1	0	0	0	Data Buses High Impedance
X	0	0	0	0	Data Buses High Impedance
X	0	0	1	0	Data Buses High Impedance
X	0	0	0	1	Data Buses High Impedance

Table 4. Flag Truth Table

$\overline{E}/\overline{F}$	\overline{HF}	State
0	1	Empty
1	1	1–1024 Locations Full
1	0	1025–2047 Locations Full
0	0	Full

Typical DC and AC Characteristics


**MILITARY SPECIFICATIONS
Group A Subgroup Testing**
DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{IX}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3
I _{OS}	1, 2, 3
I _{OZ}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t _{RC}	9, 10, 11
t _A	9, 10, 11
t _{RR}	9, 10, 11
t _{PR}	9, 10, 11
t _{LZR}	9, 10, 11
t _{DVR}	9, 10, 11
t _{HZR}	9, 10, 11
t _{WC}	9, 10, 11
t _{PW}	9, 10, 11
t _{HWZ}	9, 10, 11
t _{WR}	9, 10, 11
t _{SD}	9, 10, 11
t _{HD}	9, 10, 11
t _{MRSC}	9, 10, 11
t _{PMR}	9, 10, 11
t _{RMR}	9, 10, 11
t _{RFS}	9, 10, 11
t _{RPBS}	9, 10, 11
t _{RFBH}	9, 10, 11
t _{BDH}	9, 10, 11
t _{BSR}	9, 10, 11
t _{EFL}	9, 10, 11
t _{HFH}	9, 10, 11
t _{BRS}	9, 10, 11
t _{REF}	9, 10, 11
t _{RFF}	9, 10, 11
t _{WEF}	9, 10, 11
t _{WFF}	9, 10, 11
t _{WHF}	9, 10, 11
t _{RHF}	9, 10, 11
t _{RAE}	9, 10, 11
t _{RPE}	9, 10, 11

Parameters	Subgroups
t _{WAF}	9, 10, 11
t _{WPF}	9, 10, 11
t _{BSU}	9, 10, 11
t _{BHL}	9, 10, 11
t _{BDA}	9, 10, 11
t _{BDB}	9, 10, 11
t _{BA}	9, 10, 11
t _{BHZ}	9, 10, 11
t _{TSB}	9, 10, 11
t _{TBS}	9, 10, 11
t _{TSN}	9, 10, 11
t _{TSD}	9, 10, 11
t _{TBN}	9, 10, 11
t _{TBD}	9, 10, 11
t _{TPD}	9, 10, 11
t _{DL}	9, 10, 11
t _{ESD}	9, 10, 11
t _{EBD}	9, 10, 11
t _{EDS}	9, 10, 11
t _{EDB}	9, 10, 11
t _{BPW}	9, 10, 11
t _{TSP}	9, 10, 11
t _{BLZ}	9, 10, 11
t _{BDV}	9, 10, 11

Document #: 38-00126-D

Selection Guide

		7C441-14 7C443-14	7C441-20 7C443-20	7C441-30 7C443-30
Maximum Frequency (MHz)		71.4	50	33.3
Maximum Access Time (ns)		10	15	20
Minimum Cycle Time (ns)		14	20	30
Minimum Clock HIGH Time (ns)		6.5	9	12
Minimum Clock LOW Time (ns)		6.5	9	12
Minimum Data or Enable Set-Up (ns)		7	9	12
Minimum Data or Enable Hold (ns)		0	0	0
Maximum Flag Delay (ns)		10	15	20
Maximum Current (mA)	Commercial	140	120	100
	Military/Industrial	150	130	110

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature - 65°C to +150°C
 Ambient Temperature with
 Power Applied - 55°C to +125°C
 Supply Voltage to Ground Potential - 0.5V to +7.0V
 DC Input Voltage - 3.0V to + 7.0V
 Output Current into Outputs (LOW) 20 mA
 Static Discharge Voltage > 2001V
 (per MIL-STD-883, Method 3015)

Latch-Up Current > 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	- 40°C to +85°C	5V ± 10%
Military ^[1]	- 55°C to +125°C	5V ± 10%

Pin Definitions

Signal Name	I/O	Description
D ₀₋₈	I	Data Inputs: when the FIFO is not full and $\overline{\text{ENW}}$ is active, CKW (rising edge) writes data (D ₀ – D ₈) into the FIFO's memory
Q ₀₋₈	O	Data Outputs: when the FIFO is not empty and $\overline{\text{ENR}}$ is active, CKR (rising edge) reads data (Q ₀ – Q ₈) out of the FIFO's memory
$\overline{\text{ENW}}$	I	Enable Write: enables the CKW input
$\overline{\text{ENR}}$	I	Enable Read: enables the CKR input
CKW	I	Write Clock: the rising edge clocks data into the FIFO when $\overline{\text{ENW}}$ is LOW and updates the Almost Full flag state
CKR	I	Read Clock: the rising edge clocks data out of the FIFO when $\overline{\text{ENR}}$ is LOW and updates the Almost Empty and Empty flag states
F1	O	Flag 1: is used in conjunction with Flag 2 to decode which state the FIFO is in (see <i>Table 1</i>)
F2	O	Flag 2: is used in conjunction with Flag 1 to decode which state the FIFO is in (see <i>Table 1</i>)
$\overline{\text{MR}}$	I	Master Reset: resets the device to an empty condition

Note:

1. T_A is the "instant on" case temperature.

Switching Characteristics Over the Operating Range^[2,10]

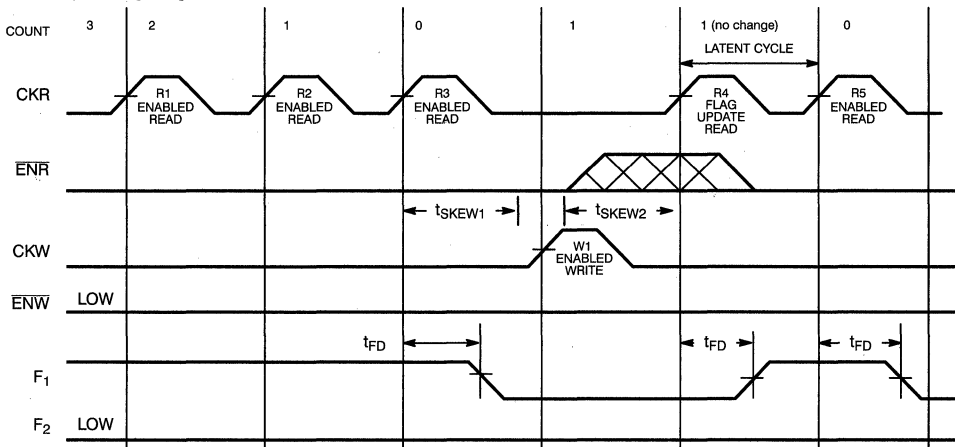
Parameter	Description	7C441-14 7C443-14		7C441-20 7C443-20		7C441-30 7C443-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CKW}	Write Clock Cycle	14		20		30		ns
t _{CKR}	Read Clock Cycle	14		20		30		ns
t _{CKH}	Clock HIGH	6.5		9		12		ns
t _{CKL}	Clock LOW	6.5		9		12		ns
t _A ^[11]	Data Access Time		10		15		20	ns
t _{OH}	Previous Output Data Hold After Read HIGH	0		0		0		ns
t _{FH}	Previous Flag Hold After Read/Write HIGH	0		0		0		ns
t _{SD}	Data Set-Up	7		9		12		ns
t _{HD}	Data Hold	0		0		0		ns
t _{SEN}	Enable Set-Up	7		9		12		ns
t _{HEN}	Enable Hold	0		0		0		ns
t _{FD}	Flag Delay		10		15		20	ns
t _{SKEW1} ^[12]	Opposite Clock After Clock	0		0		0		ns
t _{SKEW2} ^[13]	Opposite Clock Before Clock	14		20		30		ns
t _{PMR}	Master Reset Pulse Width (\overline{MR} LOW)	14		20		30		ns
t _{SCMR}	Last Valid Clock LOW Set-Up to \overline{MR} LOW	0		0		0		ns
t _{OHMR}	Data Hold From \overline{MR} LOW	0		0		0		ns
t _{MRR}	Master Reset Recovery (\overline{MR} HIGH Set-Up to First Enabled Write/Read)	14		20		30		ns
t _{MRF}	\overline{MR} HIGH to Flags Valid		14		20		30	ns
t _{AMR}	\overline{MR} HIGH to Data Outputs LOW		14		20		30	ns

Notes:

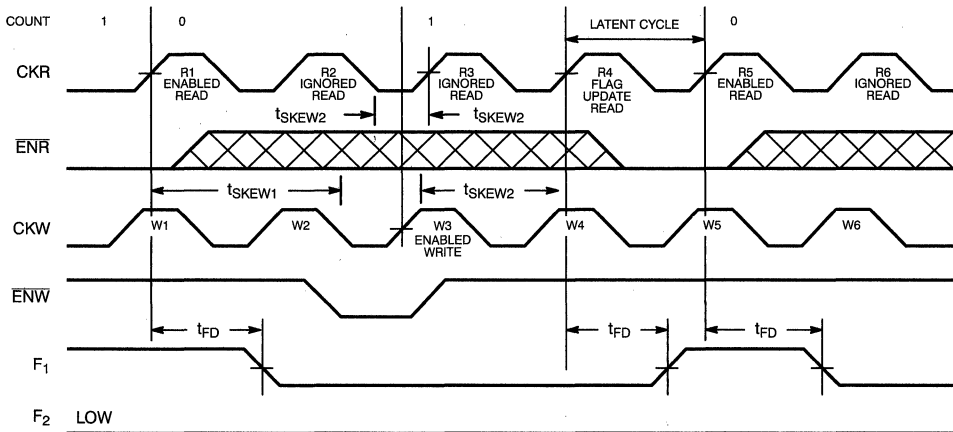
8. C_L = 30 pF for all AC parameters.
9. All AC measurements are referenced to 1.5V.
10. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and output loading as shown in the AC Test Loads and Waveforms and capacitance as in note NO TAG, unless otherwise specified.
11. Access time includes all data outputs switching simultaneously.
12. t_{SKEW1} is the minimum time an opposite clock can occur after a clock and still be guaranteed not to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW1} after the clock, the decision of whether or not to include the opposite

clock in the current clock cycle is arbitrary. *Note:* The opposite clock is the signal to which a flag is not synchronized; i.e., CKW is the opposite clock for Empty and Almost Empty flags, CKR is the the opposite clock for the Almost Full flag. The clock is the signal to which a flag is synchronized; i.e., CKW is the clock for the Almost Full flag, CKR is the clock for Empty and Almost Empty flags.

13. t_{SKEW2} is the minimum time an opposite clock can occur before a clock and still be guaranteed to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW2} before the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. See Note NO TAG for definition of clock and opposite clock.

Switching Waveforms (continued)
Read to Empty Timing Diagram^[18,19,20]


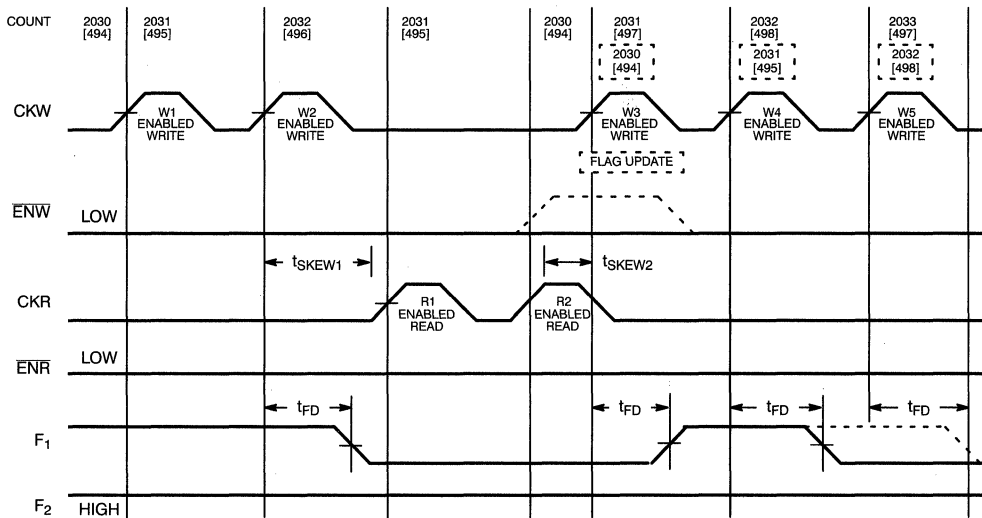
C441-9

Read to Empty Timing Diagram with Free-Running Clocks^[18,19,21]


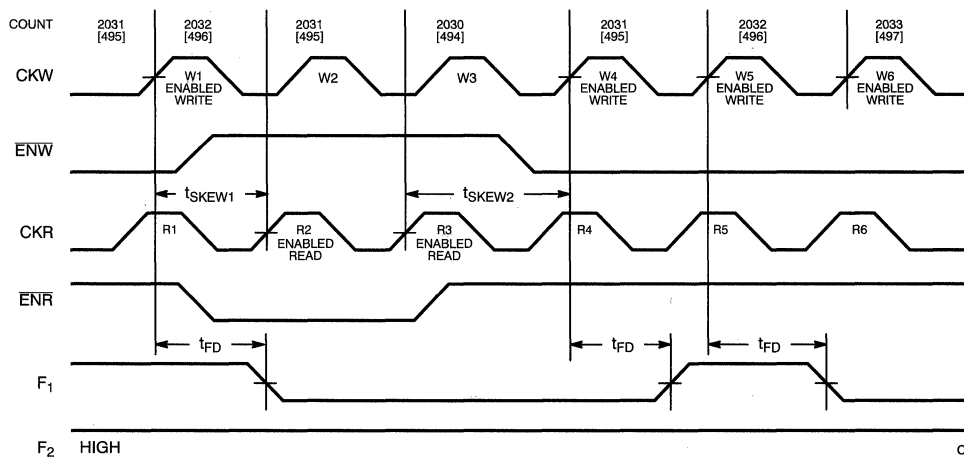
C441-10

Notes:

14. \overline{ENW} or CKW must be inactive while \overline{MR} is LOW.
15. ENR or CKR must be inactive while \overline{MR} is LOW.
16. All data outputs ($Q_0 - 8$) go LOW as a result of the rising edge of \overline{MR} .
17. In this example, $Q_0 - 8$ will remain valid until t_{OHMR} if the first read shown did not occur or if the read occurred soon enough such that the valid data was caused by it.
18. "Count" is the number of words in the FIFO.
19. CKR is clock and CKW is opposite clock.
20. R3 updates the flags to the Empty state by bringing F1 LOW. Because W1 occurs greater than t_{SKW1} after R3, R3 does not recognize W1 when updating flag status. But because W1 occurs greater than t_{SKW2} before R4, R4 includes W1 in the flag update and therefore updates the FIFO to the Almost Empty state. It is important to note that R4 is a latent cycle; i.e., it only updates the flag status, regardless of the state of ENR. It does not change the count or the FIFO's data outputs.
21. R2 is ignored because the FIFO is empty (count = 0). It is important to note that R3 is also ignored because W3, the first enabled write after empty, occurs less than t_{SKW2} before R3. Therefore, the FIFO still appears empty when R3 occurs. Because W3 occurs greater than t_{SKW2} before R4, R4 includes W3 in the flag update.

Switching Waveforms (continued)
Write to Almost Full Timing Diagram [18,24,25,26,27]


C441-13

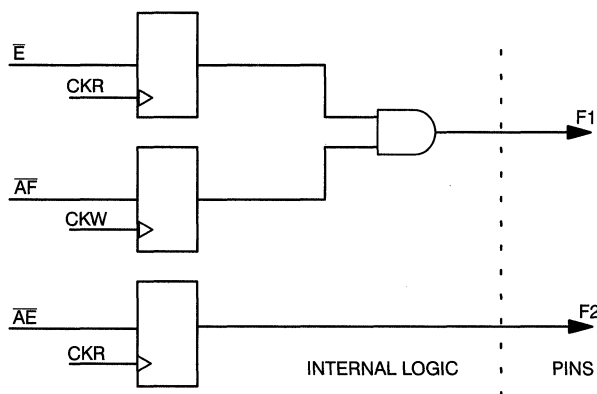
Write to Almost Full Timing Diagram with Free-Running Clocks [18,24,25]


C441-14

Notes:

24. CKW is clock and CKR is opposite clock.
 25. Count = 2032 indicates Almost Full for CY7C443 and count = 496 indicates Almost Full for CY7C441. Values for the CY7C441 count are shown in brackets.
 26. The dashed lines show W3 as flag update write rather than an enabled write because ENW is deasserted.

27. W2 updates the flags to the Almost Full state by bringing F₁ LOW. Because R1 occurs greater than t_{SKEW1} after W2, W2 does not recognize R1 when updating the flag status. W3 includes R2 in the flag update because R2 occurs greater than t_{SKEW2} before W3. Note that W3 does not have to be enabled to update flags.
 28. When making the transition from Almost Full to Intermediate, the count must decrease by two (2032 \rightarrow 2030; two enabled reads: R2, R3) before a write (W4) can update flags to Intermediate state.



C441-16

Figure 1. Flag Logic Diagram
Flag Operation (continued)

Until the flag update cycle is executed, the synchronous flags do not show the true state of the FIFO. For example, if 2,040 writes are performed to an empty CY7C443 without a single read, F1 and F2 will still exhibit an Empty flag. This is because F2 is exclusively updated by the CKR, therefore, a single read (flag update cycle) is necessary to update flags to Almost Full state. It should be noted that this flag update read does not require ENR = LOW, so a free-running read clock will initiate the flag update cycle.

When updating the flags, the CY7C441/443 decide whether or not the opposite clock was recognized when a clock updates the flag. For example, if a write occurs at least t_{SKEW1} after a read when updating the Empty flag, the write is guaranteed not to be included when CKR updates the flag. If a write occurs at least t_{SKEW2} before a read, the write is guaranteed to be included when CKR updates the flag. If a write occurs within $t_{\text{SKEW1}}/t_{\text{SKEW2}}$ after or before CKR, then the decision of whether or not to include the write when the flag is updated by CKR is arbitrary.

The update cycle for non-boundary flags (Almost Empty, Almost Full) is different from that used to update the boundary flag (Empty). Both operations are described below.

Boundary Flag (Empty)

The Empty flag is synchronized to the CKR signal. The Empty flag can only be updated by a clock pulse on the CKR pin. An empty FIFO that is written to will be described with an Empty flag state until a clock pulse is presented on the CKR pin. When making the transition from Empty to Almost Empty (or Empty to Intermediate or Empty to Almost Full), a clock cycle on the CKR is necessary to update the flags to the current state. Such a state (flags displaying empty even though data has been written to the FIFO) would require two read cycles to read data out of FIFO. The first read serves only to update the flags to the Almost Empty, Intermediate, or Almost Full state, and the second read outputs the data. This first read cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in FIFO). It simply deasserts the Empty flag. The flags are updated regardless of the ENR state. Therefore the update occurs even when ENR is deasserted (HIGH) so that a valid read is not necessary to update the flags to correctly describe the FIFO. With a free-running clock connected to CKR, the flag

updates with each cycle. *Table 2* shows sample operations that update the Empty flag.

Although a Full flag is not supplied externally on the CY7C441/CY7C443, a Full flag exists internally. The operation of the FIFO at the Full boundary is analogous to its operation at the Empty boundary. See the text section “Boundary Flags (Full)” in the CY7C451/CY7C453 datasheet.

Non-Boundary Flags (Almost Empty, Almost Full)

The flag status pins, F1 and F2, exhibit the Almost Empty status when both the CY7C441 and the CY7C443 contain 16 words or less. The Almost Full Flag becomes active when the FIFO contains 16 or less empty locations. The CY7C441 becomes Almost Full when it contains 496 words. The CY7C443 becomes Almost Full when it contains 2032 words. The Almost Empty flag (like the Empty flag) is synchronous to the CKR signal, whereas the Almost Full flag is synchronous to the CKW signal. Non-boundary flags employ flag update cycles similar to the boundary flag latent cycles in order to update the FIFO state. For example, if the FIFO just reaches the Almost Empty state (16 words) and then two words are written, a read clock (CKR) will be required to update the flags to the Intermediate state. However, unlike the boundary (Empty) flag’s update cycle, the state of the enable pin (ENR in this case) affects the operation. Therefore, ENR set-up (t_{SEN}) and hold (t_{HEN}) times must be met. If ENR is asserted (ENR = LOW) during the latent cycle, the count and data update in addition to F1 and F2. If ENR is not active (ENR = 1) during the flag update cycle, only the flag is updated.

The same principles apply for updating the flags when a transition from the Almost Full to the Intermediate state occurs. If the CY7C443 just reaches the Almost Full state (2032 words) and then two words are read, a write clock (CKW) will be required to update the flag to the Intermediate state. If ENW is LOW during the flag update cycle, the count and data update in addition to the flags. If ENW is HIGH, only the flag is updated. Therefore, ENW set-up (t_{SEN}) and hold (t_{HEN}) times must be met. *Tables 3* and *4* show examples for a sequence of operations that affect the Almost Empty and Almost Full flags, respectively.

Width Expansion

The CY7C441/3 can be expanded in width to provide word width greater than 9 in increments of 9. During width expansion mode, all control inputs are common. When the FIFO is being read near

Table 4. Almost Full Flag Operation Example^[30,31]

Status Before Operation					Operation	Next State of FIFO	Status After Operation				
Current State of FIFO	F1	F2	Number of Words in FIFO CY7C441	Number of Words in FIFO CY7C443			F1	F2	Number of Words in FIFO CY7C441	Number of Words in FIFO CY7C443	Comments
AF	0	1	496	2032	Read (ENR=LOW)	AF	0	1	495	2031	Read
AF	0	1	495	2031	Read (ENR=LOW)	AF	0	1	494	2030	Read
AF	0	1	494	2030	Write (ENW=HIGH)	Intermediate	1	1	494	2030	Flag Update
Intermediate	1	1	494	2030	Write (ENW=LOW)	Intermediate	1	1	495	2031	Write
Intermediate	1	1	495	2031	Write (ENW=LOW)	AF	0	1	496	2032	Write (Transition from Intermediate to Almost Full)

Notes:

29. Applies to both the CY7C441 and CY7C443 operations.

30. The CY7C441 Almost Full state is represented by 496 or more words.

31. The CY7C443 Almost Full state is represented by 2032 or more words.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C441-14PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C441-14JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441-14VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C441-14PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C441-14JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441-14DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C441-14LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C441-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C441-20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441-20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C441-20PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C441-20JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C441-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C441-30PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C441-30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441-30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C441-30PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C441-30JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441-30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C441-30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{CC1}	1, 2, 3
I _{CC2}	1, 2, 3
I _{SB}	1, 2, 3
I _{OS}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{CKR}	9, 10, 11
t _{CKW}	9, 10, 11
t _{CKH}	9, 10, 11
t _{CKL}	9, 10, 11
t _A	9, 10, 11
t _{OH}	9, 10, 11
t _{FH}	9, 10, 11
t _{SD}	9, 10, 11
t _{HD}	9, 10, 11
t _{SEN}	9, 10, 11
t _{HEN}	9, 10, 11
t _{HENR}	9, 10, 11
t _{FD}	9, 10, 11
t _{SKEW1}	9, 10, 11
t _{SKEW2}	9, 10, 11
t _{PMR}	9, 10, 11
t _{SCMR}	9, 10, 11
t _{OHMR}	9, 10, 11
t _{MRR}	9, 10, 11
t _{MRF}	9, 10, 11
t _{AMR}	9, 10, 11

Document #: 38-00124-F

Functional Description (continued)

valid in the standalone and width expansion configurations. In the depth expansion, this pin provides the expansion out (\overline{XO}) information that is used to signal the next FIFO when it will be activated.

The flags are synchronous, i.e., they change state relative to either the read clock (CKR) or the write clock (CKW). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the CKR. The flags denoting Half Full, Almost Full,

and Full states are updated exclusively by CKW. The synchronous flag architecture guarantees that the flags maintain their status for some minimum time.

The CY7C451 and the CY7C453 use center power and ground for reduced noise. Both configurations are fabricated using an advanced 0.8μ N-well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of reliable layout techniques, guard rings, and a substrate bias generator.

Selection Guide

		7C451-14 7C453-14	7C451-20 7C453-20	7C451-30 7C453-30
Maximum Frequency (MHz)		71.4 ^[1]	50	33.3
Maximum Cascadable Frequency		N/A ^[2]	50	33.3
Maximum Access Time (ns)		10	15	20
Minimum Cycle Time (ns)		14	20	30
Minimum Clock HIGH Time (ns)		6.5	9	12
Minimum Clock LOW Time (ns)		6.5	9	12
Minimum Data or Enable Set-Up (ns)		7	9	12
Minimum Data or Enable Hold (ns)		0	0	0
Maximum Flag Delay (ns)		10	15	20
Maximum Current (mA)	Commercial	140	120	100
	Military/Industrial	150	130	110

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-3.0V to +7.0V
Output Current into Outputs (LOW)	20 mA

Notes:

- 71.4-MHz operation is available only in the standalone configuration.
- The -14 device cannot be cascaded.

Static Discharge Voltage > 2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current > 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Military ^[3]	-55°C to +125°C	5V ± 10%

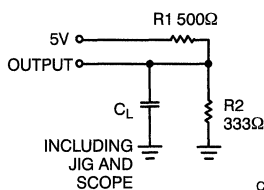
- T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range^[4]

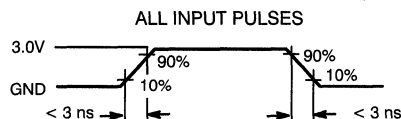
Parameter	Description	Test Conditions	7C451-14 7C453-14		7C451-20 7C453-20		7C451-30 7C453-30		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 2.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH} ^[5]	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL} ^[5]	Input LOW Voltage		-3.0	0.8	-3.0	0.8	-3.0	0.8	V
I _{IX}	Input Leakage Current	V _{CC} = Max.	-10	+10	-10	+10	-10	+10	μA
I _{OS} ^[6]	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = GND	-90		-90		-90		mA
I _{OZL} I _{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, V _{SS} < V _O < V _{CC}	-10	+10	-10	+10	-10	+10	μA
I _{CC1} ^[7]	Operating Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	140		120		100	mA
			Mil/Ind	150		130		110	mA
I _{CC2} ^[8]	Operating Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	70		70		70	mA
			Mil/Ind	80		80		80	mA
I _{SB} ^[9]	Standby Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	30		30		30	mA
			Mil/Ind	30		30		30	mA

Capacitance^[10]

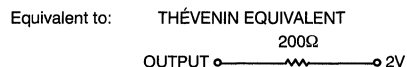
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		12	pF

AC Test Loads and Waveforms^[11, 12, 13, 14, 15]


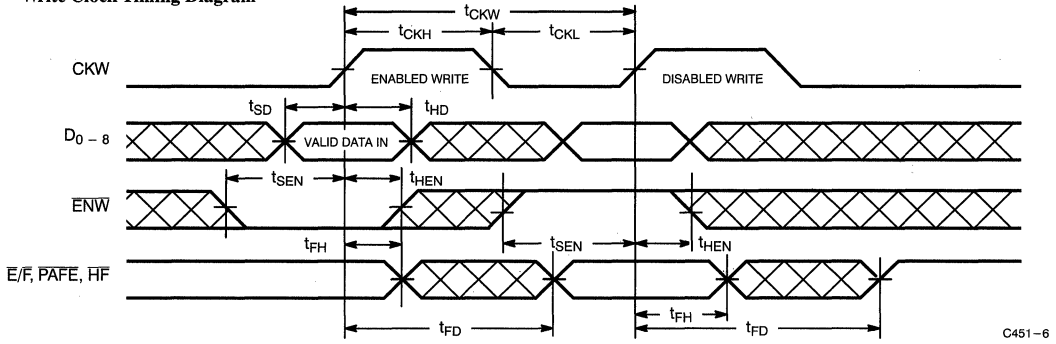
C451-4



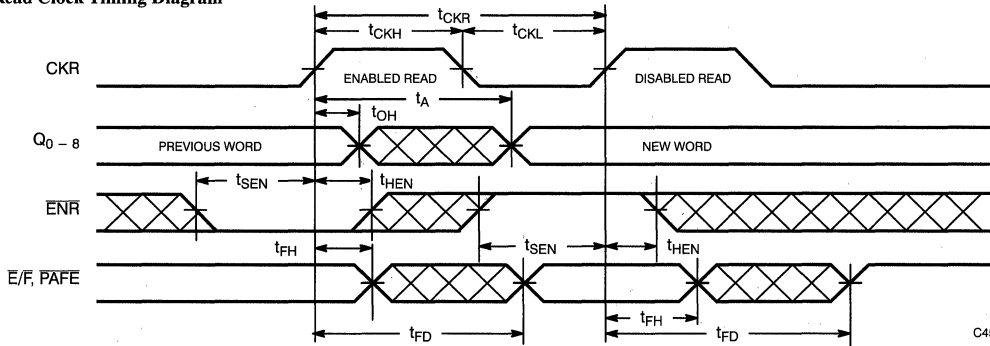
C451-5


Notes:

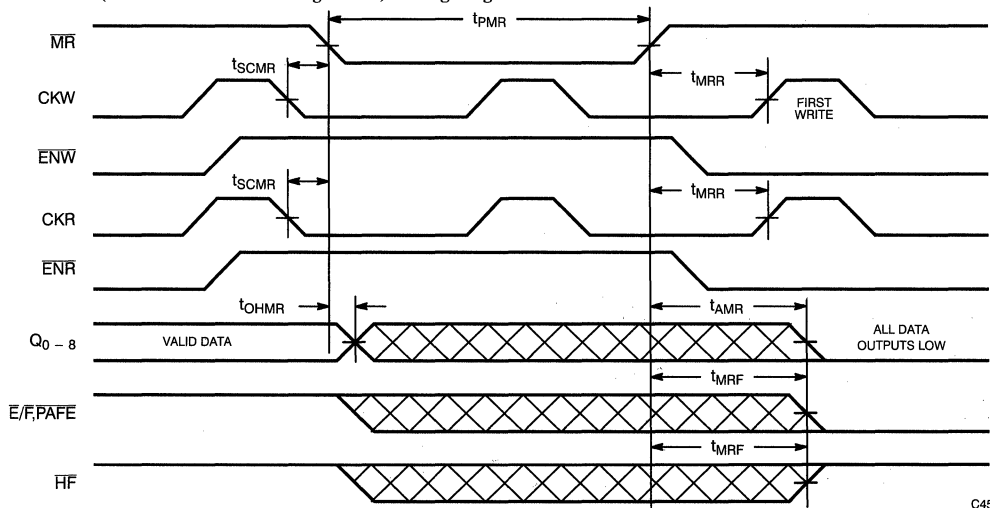
- See the last page of this specification for Group A subgroup testing information.
- The V_{IH} and V_{IL} specifications apply for all inputs except \overline{XI} and \overline{FL} . The \overline{XI} pin is not a TTL input. It is connected to either \overline{XO} of the previous device or V_{SS}. \overline{FL} must be connected to either V_{SS} or V_{CC}.
- Test no more than one output at a time for not more than one second.
- Input signals switch from 0V to 3V with a rise/fall time of 3 ns or less, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at f_{MAX}/2. Outputs are unloaded.
- Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
- All inputs signals are connected to V_{CC}. All outputs are unloaded. Read and write clocks switch at maximum frequency (f_{MAX}).
- Tested initially and after any design or process changes that may affect these parameters.
- C_L = 30 pF for all AC parameters except for t_{OHZ}.
- C_L = 5 pF for t_{OHZ}.
- All AC measurements are referenced to 1.5V except t_{OE}, t_{OLZ}, and t_{OHZ}.
- t_{OE} and t_{OLZ} are measured at ± 100 mV from the steady state.
- t_{OHZ} is measured at +500 mV from V_{OL} and - 500 mV from V_{OH}.

Switching Waveforms
Write Clock Timing Diagram


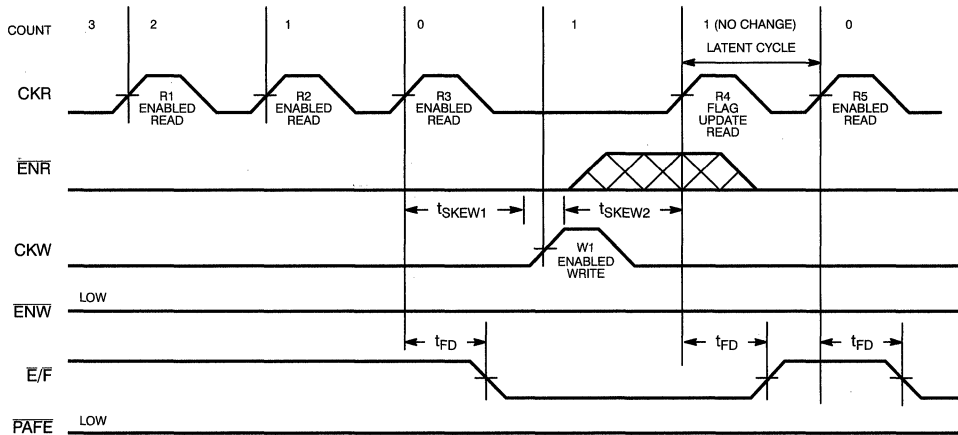
C451-6

Read Clock Timing Diagram


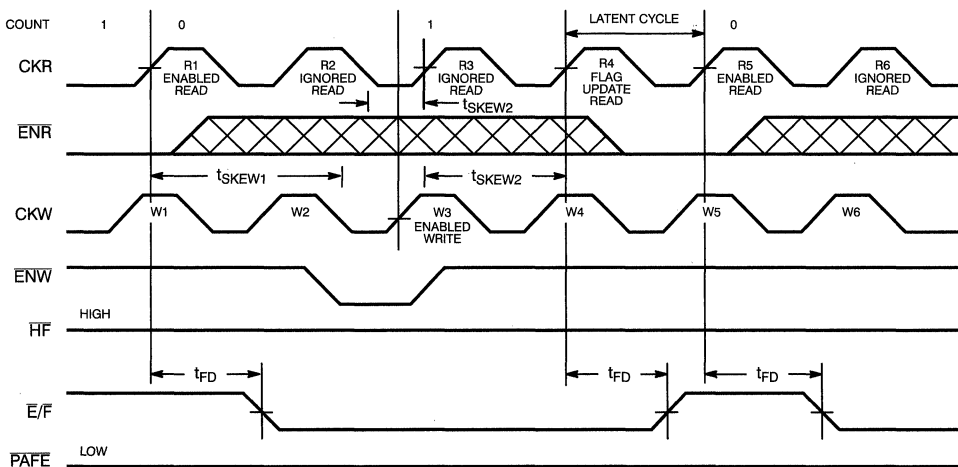
C451-7

Master Reset (Default with Free-Running Clocks) Timing Diagram [21, 22, 23, 24]


C451-8

Switching Waveforms (continued)
Read to Empty Timing Diagram^[25, 28, 29]


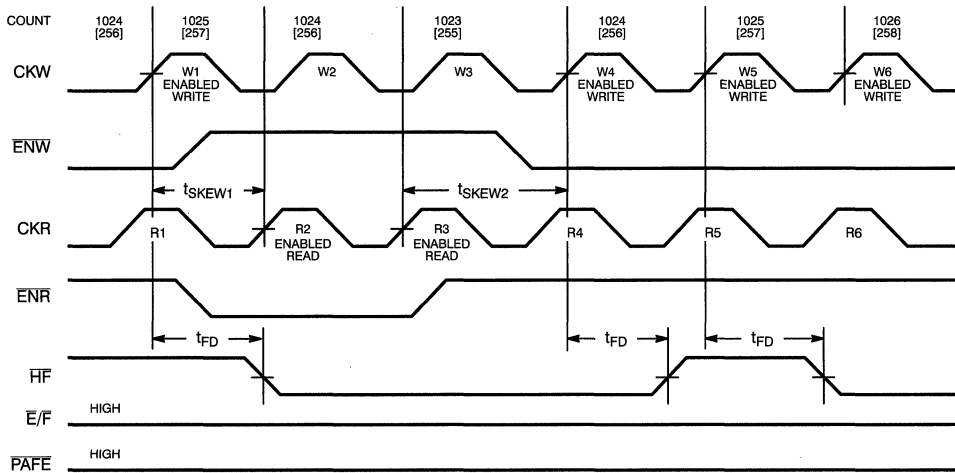
C451-11

Read to Empty Timing Diagram with Free-Running Clocks^[25, 26, 27, 28]


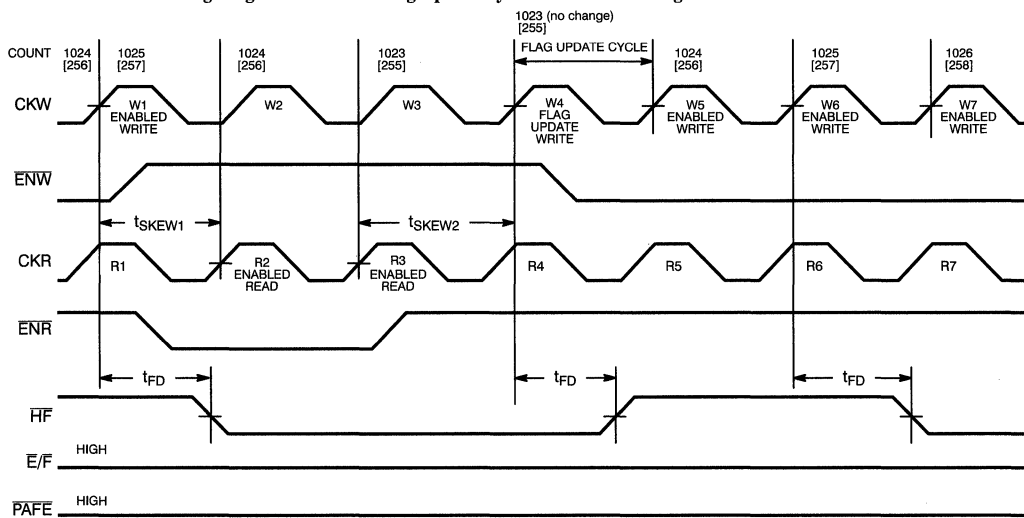
C451-12

Notes:

25. "Count" is the number of words in the FIFO.
26. The FIFO is assumed to be programmed with $P > 0$ (i.e., \overline{PAFE} does not transition at Empty or Full).
27. R2 is ignored because the FIFO is empty (count = 0). It is important to note that R3 is also ignored because W3, the first enabled write after empty, occurs less than t_{SKWEW2} before R3. Therefore, the FIFO still appears empty when R3 occurs. Because W3 occurs greater than t_{SKWEW2} before R4, R4 includes W3 in the flag update.
28. CKR is clock; CKW is opposite clock.
29. R3 updates the flag to the Empty state by asserting $\overline{E/F}$. Because W1 occurs greater than t_{SKWEW1} after R3, R3 does not recognize W1 when updating flag status. But because W1 occurs greater than t_{SKWEW2} before R4, R4 includes W1 in the flag update and, therefore, updates FIFO to Almost Empty state. It is important to note that R4 is a latent cycle; i.e., it only updates the flag status regardless of the state of ENR. It does not change the count or the FIFO's data outputs.

Switching Waveforms (continued)
Write to Half Full Timing Diagram with Free-Running Clocks^[25, 33, 34, 35]


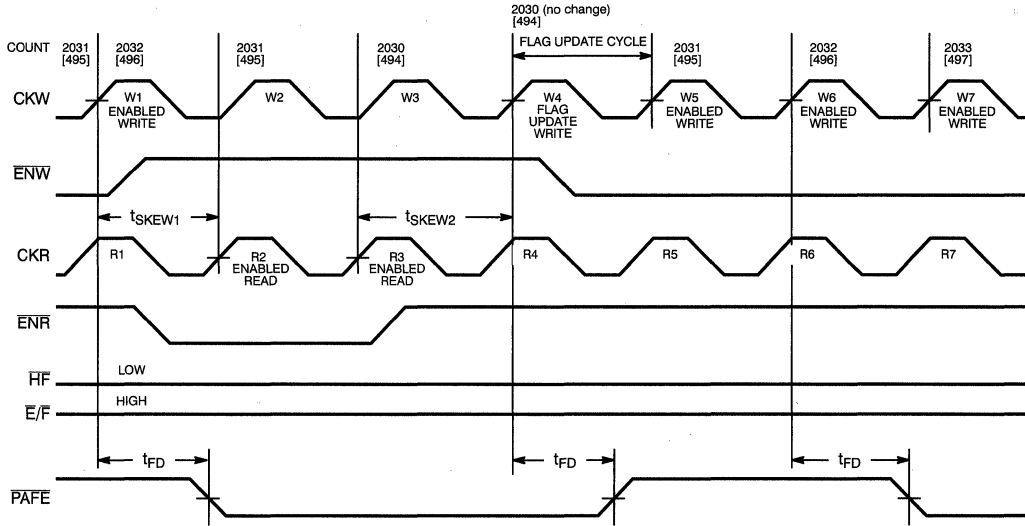
C451-15

Write to Half Full Timing Diagram with Write Flag Update Cycle with Free-Running Clocks^[25, 33, 34, 35, 36, 37]


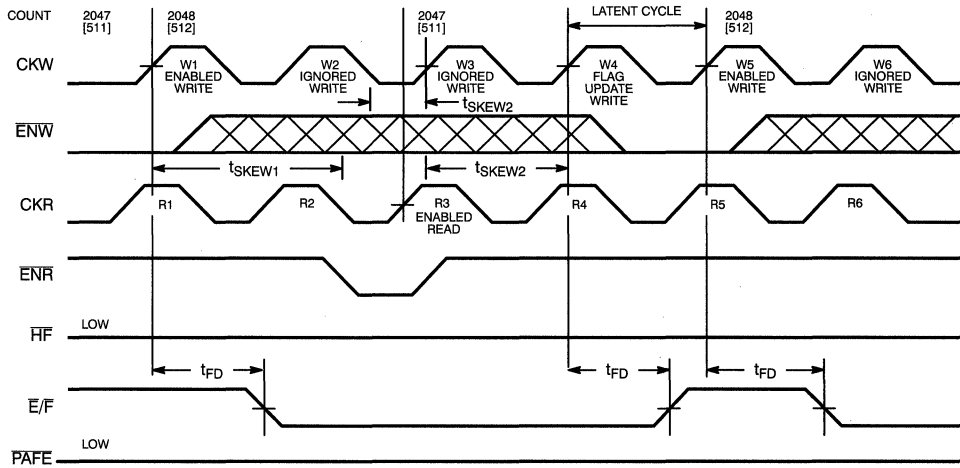
C451-16

Notes:

33. CKW is clock and CKR is opposite clock.
34. Count = 1,025 indicates Half Full for the CY7C453 and count = 257 indicates Half Full for the CY7C451. Values for CY7C451 count are shown in brackets.
35. When the FIFO contains 1,024 [256] words, the rising edge of the next enabled write causes the HF to be true (LOW).
36. The HF write flag update cycle does not affect the count because ENW is HIGH. It only updates HF to HIGH.
37. When making the transition from Half Full to Less Than Half Full, the count must decrease by two (1,025 \rightarrow 1,023; two enabled reads: R2 and R3) before a write (W4) can update flags to less than Half Full.

Switching Waveforms (continued)
Write to Almost Full Timing Diagram with Write Flag Update Cycle and Free-Running Clocks^[25, 30, 33]


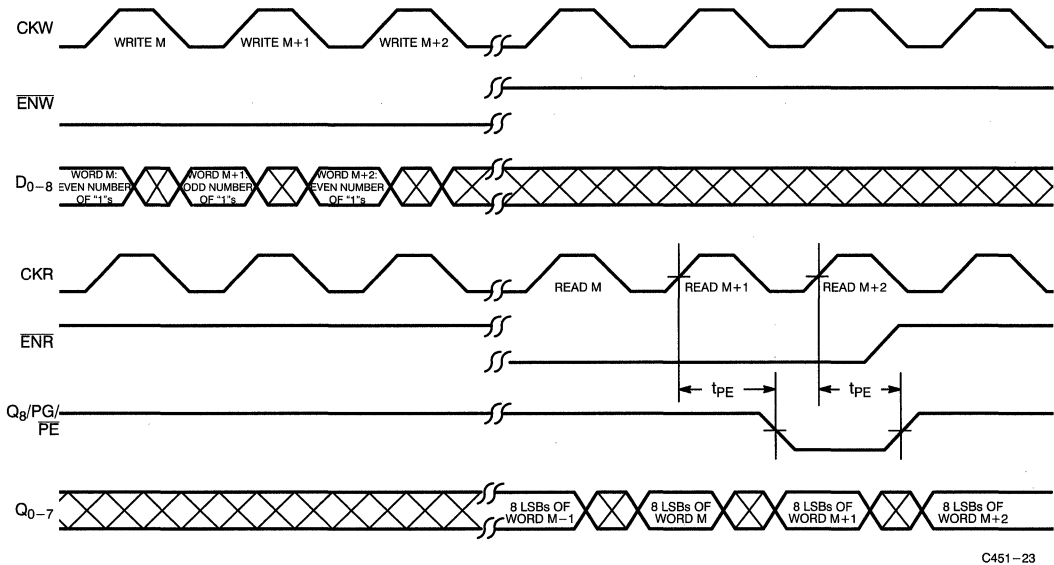
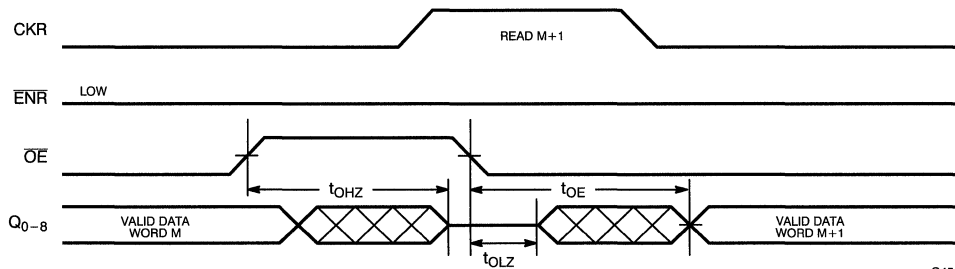
C451-19

Write to Full Flag Timing Diagram with Free-Running Clocks^[25, 26, 33, 40]


C451-20

Note:

40. W2 is ignored because the FIFO is full (count = 2,048 [512]). It is important to note that W3 is also ignored because R3, the first enabled read after full, occurs less than t_{SKEW2} before W3. Therefore, the FIFO still appears full when W3 occurs. Because R3 occurs greater than t_{SKEW2} before W4, W4 includes R3 in the flag update.

Switching Waveforms (continued)
Even Parity Checking^[44]

Output Enable Timing^[45, 46]

Notes:

44. In this example, the FIFO is assumed to be programmed to check for even parity.
45. This example assumes that the time from the CKR rising edge to valid word M+1 $\geq t_A$.
46. If ENR was HIGH around the rising edge of CKR (i.e., read disabled), the valid data at the far right would once again be word M instead of word M+1.

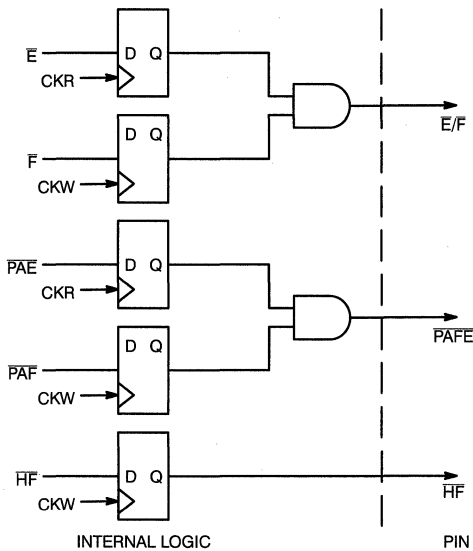


Figure 1. Flag Logic Diagram

Flag Operation (continued)

Since the flags denoting emptiness (Empty, Almost Empty) are only updated by CKR and the flags signifying fullness (Half Full, Almost Full, Full) are exclusively updated by CKW, careful attention must be given to the flag operation. The user must be aware that if a boundary (Empty, Almost Empty, Half Full, Almost Full, or Full) is crossed due to an operation from a clock that the flag is not synchronized to (i.e., CKW does not affect Empty or Almost Empty), a flag update cycle is necessary to represent the FIFO's new state. The signal to which a flag is not synchronized will be referred to as the opposite clock (CKW is opposite clock for Empty and Almost Empty flags; CKR is the opposite clock for Half Full, Almost Full, and Full flags). Until a proper flag update cycle is executed, the synchronous flags will not show the new state of the FIFO.

When updating flags, the CY7C451/453 must make a decision as to whether or not the opposite clock was recognized when a clock updates the flag. For example (when updating the Empty flag), if a write occurs at least t_{SKEW1} after a read, the write is guaranteed not to be included when CKR updates the flag. If a write occurs at least t_{SKEW2} before a read, the write is guaranteed to be included when CKR updates flag. If a write occurs within t_{SKEW1}/t_{SKEW2} after or before CKR, then the decision of whether or not to include the write when the flag is updated by CKR is arbitrary.

The update cycle for non-boundary flags (Almost Empty, Half Full, Almost Full) is different from that used to update the boundary flags (Empty, Full). Both operations are described below.

Boundary and Non-Boundary Flags

Boundary Flags (Empty)

The Empty flag is synchronized to the CKR signal (i.e., the Empty flag can only be updated by a clock pulse on the CKR pin). An empty FIFO that is written to will be described with an Empty flag state until a rising edge is presented to the CKR pin. When making the transition from Empty to Almost Empty (or Empty to Less than or Equal to Half Full), a clock cycle on the CKR is necessary to update the flags to the current state. In such a state (flags showing Empty even though data has been written to the FIFO), two read cycles are required to read data out of FIFO. The first read serves only to update the flags to the Almost Empty or Less than or Equal to Half Full state, while the second read outputs the data. This first read cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in FIFO). It simply deasserts the Empty flag. The flag is updated regardless of the \overline{ENR} state. Therefore, the update occurs even when \overline{ENR} is unasserted (HIGH), so that a valid read is not necessary to update the flags to correctly describe the FIFO. In this example, the write must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the write will be included in the count when CKR updates the flags. When a free-running clock is connected to CKR, the flag is updated each cycle. *Table 2* shows an example of a sequence of operations that update the Empty flag.

Boundary Flags (Full)

The Full flag is synchronized to the CKW signal (i.e., the Full flag can only be updated by a clock pulse on the CKW pin). A full FIFO that is read will be described with a Full flag until a rising edge is presented to the CKW pin. When making the transition from Full to Almost Full (or Full to Greater Than Half Full), a clock cycle on the CKW is necessary to update the flags to the current state. In such a state (flags showing Full even though data has been read from the FIFO), two write cycles are required to write data into the FIFO. The first write serves only to update the flags to the Almost Full or Greater Than Half Full state, while the second write inputs the data. This first write cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in the FIFO). It simply deasserts the Full flag. The flag is updated regardless of the \overline{ENW} state. Therefore, the update occurs even when \overline{ENW} is deasserted (HIGH), so that a valid write is not necessary to update the flags to correctly describe the FIFO. In this example, the read must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the read will be included in the count when CKW updates the flags. When a free-running clock is connected to CKW, the flag updates each cycle. Full flag operation is similar to the Empty flag operation described in *Table 2*.

Non-Boundary Flags (Almost Empty, Half Full, Almost Full)

The CY7C451/453 feature programmable Almost Empty and Almost Full flags. Each flag can be programmed a specific distance from the corresponding boundary flags (Empty or Full). The flags can be programmed to be activated at the Empty or Full boundary, or at a distance of up to 1008 words/locations for the CY7C453 (240 words/locations for the CY7C451) from the Empty/Full boundary. The programming resolution is 16 words/locations. When the FIFO contains the number of words or fewer for which the flags have been programmed, the \overline{PAFE} flag will be asserted signifying that the FIFO is Almost Empty. When the FIFO is within that same number of empty locations from being Full, the \overline{PAFE} will also be asserted signifying that the FIFO is Almost Full. The \overline{HF} flag is decoded to distinguish the states.

\overline{XO} of the last device connected to \overline{XI} of the first device. The first device has its first load pin (\overline{FL}) tied to V_{SS} while all other devices must have this pin tied to V_{CC} . The first device will be the first to be write and read enabled after a master reset.

Proper operation also requires that all cascaded devices have common CKW, CKR, ENW, ENR, D_0-8 , Q_0-8 , and MR pins. When cascaded, one device at a time will be read enabled so as to avoid bus contention. By asserting \overline{XO} when appropriate, the currently enabled FIFO alerts the next FIFO that it should be enabled. The next rising edge on CKR puts Q_0-8 outputs of the first device into a high-impedance state. This occurs regardless of the state of ENR or the next FIFO's Empty flag. Therefore, if the next FIFO is empty or undergoing a latent cycle, the Q_0-8 bus will be in a high-

impedance state until the next device receives its first read, which brings its data to the Q_0-8 bus.

Program Write/Read of Cascaded Devices

Programming of cascaded FIFOs is the same as for a single device. Because the controls of the FIFOs are in parallel when cascaded, they all get programmed the same. During program mode, only parity is programmed since Almost Full and Almost Empty flags are not available when CY7C451/453 are cascaded. Only the "first device" (FIFO with $\overline{FL}=\text{LOW}$) will output its program register contents on Q_0-8 during a program read. Q_0-8 of all other devices will remain in a high-impedance state to avoid bus contention.

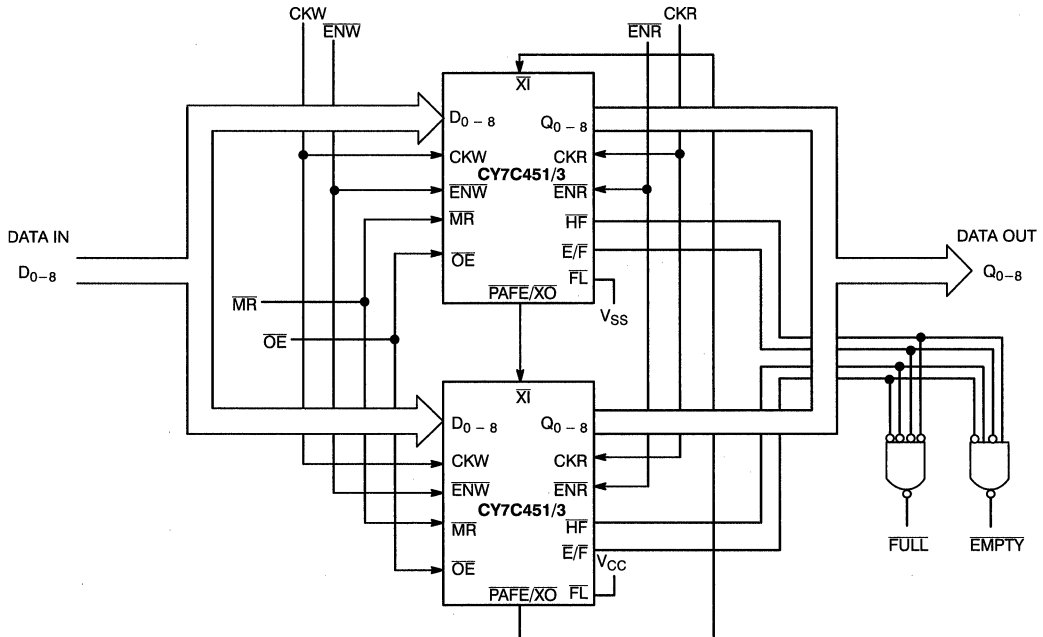


Figure 2. Depth Expansion with CY7C451/3

Table 5. Programmable Almost Full/Almost Empty Options – CY7C451/CY7C453^[50]

D5	D4	D3	D2	D1	D0	PAFE Active when CY7C451/453 is:	p ^[51]
0	0	0	0	0	0	Completely Full and Empty.	0
0	0	0	0	0	1	16 or less locations from Empty/Full (default)	1
0	0	0	0	1	0	32 or less locations from Empty/Full	2
0	0	0	0	1	1	48 or less locations from Empty/Full	3
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	0	1	1	1	0	224 or less locations from Empty/Full	14
0	0	1	1	1	1	240 or less locations from Empty/Full	15
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	0	992 or less locations from Empty/Full	62
1	1	1	1	1	1	1008 or less locations from Empty/Full	63

Table 6. Programmable Parity Options

D8	D7	D6	Condition
0	X	X	Parity disabled.
1	0	0	Generate even parity on PG output pin.
1	0	1	Generate odd parity on PG output pin.
1	1	0	Check for even parity. Indicate error on \overline{PE} output pin.
1	1	1	Check for odd parity. Indicate error on \overline{PE} output pin.

Notes:

50. D4 and D5 are don't care for CY7C451.

51. Referenced in *Table 1*.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C451-14DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C451-14JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C451-14JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C451-14DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C451-14LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C451-20DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C451-20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C451-20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C451-20DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C451-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C451-30DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C451-30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C451-30JI	D32	32-Lead (300-Mil) CerDIP	Industrial
	CY7C451-30DMB	D32	32-Lead (300-Mil) CerDIP	Military
CY7C451-30LMB	L55	32-Pin Rectangular Leadless Chip Carrier		

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C453-14DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C453-14JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C453-14JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C453-14DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C453-14LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C453-20DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C453-20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C453-20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C453-20DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C453-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C453-30DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C453-30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C453-30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C453-30DMB	D32	32-Lead (300-Mil) CerDIP	Military
CY7C453-30LMB	L55	32-Pin Rectangular Leadless Chip Carrier		



CY7C455
CY7C456
CY7C457

512 x 18, 1K x 18, and 2K x 18 Cascadable Clocked FIFOs with Programmable Flags

Features

- 512 x 18 (CY7C455), 1,024 x 18 (CY7C456), 2,048 x 18 (CY7C457) FIFO buffer memory
- Expandable in width
- Expandable in depth
- High-speed 70-MHz standalone; 50-MHz cascaded
- Supports free-running 50% duty cycle clock inputs
- Empty, Full, Half Full, and programmable Almost Empty and Almost Full status flags
- Parity generation/checking
- Fully asynchronous and simultaneous read and write operation
- Output Enable (\overline{OE}) pin
- Independent read and write enable pins
- Center power and ground pins for reduced noise
- 52-pin PLCC and 52-pin PQFP
- Proprietary 0.8 μ CMOS technology
- TTL compatible

Functional Description

The CY7C455, CY7C456, and CY7C457 are high-speed, low-power, first-in-first-out (FIFO) memories with clocked read and write interfaces. All are 18 bits wide. The CY7C455 has a 512-word memory array, the CY7C456 has a 1,024-word memory array, and the CY7C457 has a 2,048-word memory array. The CY7C455, CY7C456, and CY7C457 can be cascaded to increase FIFO depth. Programmable features include Almost Full/Empty flags and generation/checking of parity. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

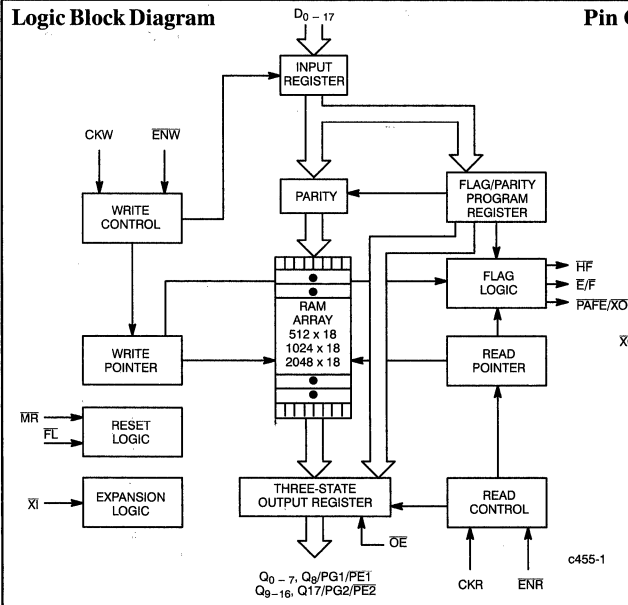
These FIFOs have 18-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (CKW) and a write enable pin (ENW). The output port is controlled by a read clock (CKR) and a read enable pin (ENR).

When ENW is asserted, data is written into the FIFO on the rising edge of the

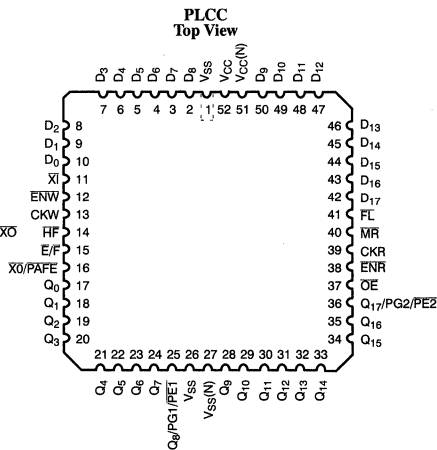
CKW signal. While \overline{ENW} is held active, data is continually written into the FIFO on each CKW cycle. The output port is controlled in a similar manner by a free-running read clock (CKR) and a read enable pin (\overline{ENR}). In addition, the CY7C455, CY7C456, and CY7C457 have an output enable pin (\overline{OE}). The read (CKR) and write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 71.4 MHz are achievable in the standalone configuration, and up to 50 MHz is achievable when FIFOs are cascaded for depth expansion.

Depth expansion is possible using the cascade input (\overline{XI}), cascade output (\overline{XO}), and First Load (\overline{FL}) pins. The \overline{XO} pin is connected to the \overline{XI} pin of the next device, and the \overline{XO} pin of the last device should be connected to the \overline{XI} pin of the first device. The \overline{FL} pin of the first device is tied to V_{SS} .

Logic Block Diagram



Pin Configuration





Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-3.0V to +7.0V
Output Current into Outputs (LOW)	20 mA

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial ^[2]	-40°C to +85°C	5V ± 10%

Pin Definitions

Signal Name	I/O	Description
D ₀₋₁₇	I	Data Inputs: When the FIFO is not full and \overline{ENW} is active, CKW (rising edge) writes data (D ₀₋₁₇) into the FIFO's memory. If MR is asserted at the rising edge of CKW, data is written into the FIFO's programming register. D _{8,17} are ignored if the device is configured for parity generation.
Q ₀₋₇ Q ₉₋₁₆	O	Data Outputs: When the FIFO is not empty and \overline{ENR} is active, CKR (rising edge) reads data (Q ₀₋₇ , Q ₉₋₁₆) out of the FIFO's memory. If MR is active at the rising edge of CKR, data is read from the programming register.
Q ₈ /PG1/PE1 Q ₁₇ /PG2/PE2	O	Function varies according to mode: Parity disabled – same function as Q ₀₋₇ and Q ₉₋₁₆ Parity enabled, generation – parity generation bit (PG _x) Parity enabled, check – Parity Error Flag (PE _x)
\overline{ENW}	I	Enable Write: Enables the CKW input (for both non-program and program modes).
\overline{ENR}	I	Enable Read: Enables the CKR input (for both non-program and program modes).
CKW	I	Write Clock: The rising edge clocks data into the FIFO when \overline{ENW} is LOW; updates Half Full, Almost Full, and Full flag states. When MR is asserted, CKW writes data into the program register.
CKR	I	Read Clock: The rising edge clocks data out of the FIFO when \overline{ENR} is LOW; updates the Empty and Almost Empty flag states. When MR is asserted, CKR reads data out of the program register.
HF	O	Half Full Flag: Synchronized to CKW.
E/F	O	Empty or Full Flag: \overline{E} is synchronized to CKR; \overline{F} is synchronized to CKW.
$\overline{PAFE}/\overline{XO}$	O	Dual-Mode Pin: Not Cascaded – programmable Almost Full is synchronized to CKW; Programmable Almost Empty is synchronized to CKR. Cascaded – expansion out signal, connected to \overline{XI} of next device.
\overline{XI}	I	Expansion-In Pin: Not Cascaded – \overline{XI} is tied to V _{SS} . Cascaded – expansion Input, connected to \overline{XO} of previous device.
\overline{FL}	I	First Load Pin: Cascaded – the first device in the daisy chain will have \overline{FL} tied to V _{SS} ; all other devices will have \overline{FL} tied to V _{CC} (Figure 1). Not Cascaded – tied to V _{CC} .
MR	I	Master Reset: Resets device to empty condition. Non-Programming Mode: Program register is reset to default condition of no parity and \overline{PAFE} active at 16 or less locations from Full/Empty. Programming Mode: Data present on D ₀₋₈ is written into the programmable register on the rising edge of CKW. Program register contents appear on Q ₀₋₈ after the rising edge of CKR.
\overline{OE}	I	Output Enable for Q ₀₋₇ , Q ₉₋₁₆ , Q ₈ /PG1/PE1 and Q ₁₇ /PG2/PE2 pins.

Note:

2. T_A is the "instant on" case temperature.



Switching Characteristics Over the Operating Range^[3, 15]

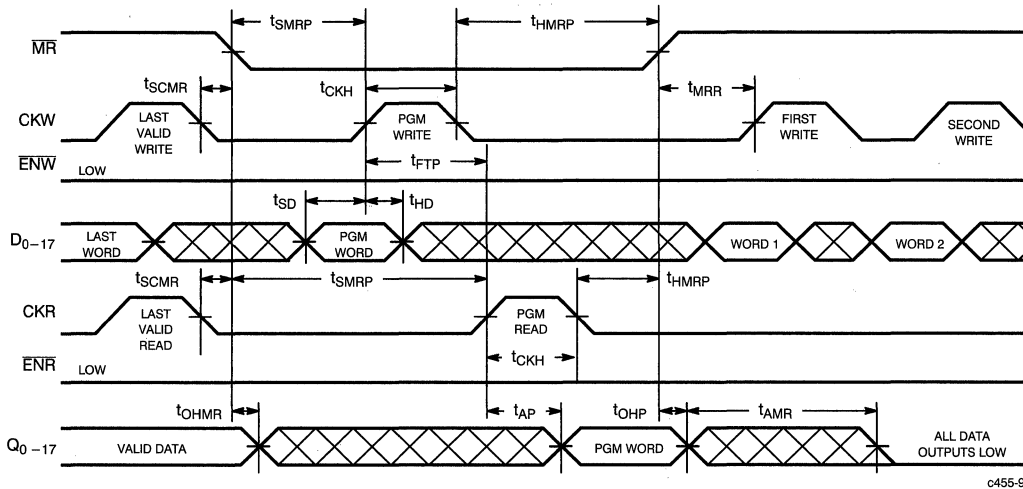
Parameter	Description	7C45X-14		7C45X-20		7C45X-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CKW}	Write Clock Cycle	14		20		30		ns
t _{CKR}	Read Clock Cycle	14		20		30		ns
t _{CKH}	Clock HIGH	6.5		9		12		ns
t _{CKL}	Clock LOW	6.5		9		12		ns
t _A	Data Access Time		10		15		20	ns
t _{OH}	Previous Output Data Hold After Read HIGH	0		0		0		ns
t _{FH}	Previous Flag Hold After Read/Write HIGH	0		0		0		ns
t _{SD}	Data Set-Up	5		7		9		ns
t _{HD}	Data Hold	1		1		1		ns
t _{SEN}	Enable Set-Up	5		7		9		ns
t _{HEN}	Enable Hold	1		1		1		ns
t _{OE}	\overline{OE} LOW to Output Data Valid		10		15		20	ns
t _{OLZ} ^[9, 16]	\overline{OE} LOW to Output Data in Low Z	0		0		0		ns
t _{OZH} ^[9, 16]	\overline{OE} HIGH to Output Data in High Z		10		15		20	ns
t _{PG}	Read HIGH to Parity Generation		10		15		20	ns
t _{PE}	Read HIGH to Parity Error Flag		10		15		20	ns
t _{FD}	Flag Delay		10		15		20	ns
t _{SKEW1} ^[17]	Opposite Clock After Clock	0		0		0		ns
t _{SKEW2} ^[18]	Opposite Clock Before Clock	14		20		30		ns
t _{PMR}	Master Reset Pulse Width (\overline{MR} LOW)	14		20		30		ns
t _{SCMR}	Last Valid Clock Low Set-Up to \overline{MR} LOW	0		0		0		ns
t _{OHMR}	Data Hold From \overline{MR} LOW	0		0		0		ns
t _{MRR}	Master Reset Recovery (\overline{MR} HIGH Set-Up to First Enabled Write/Read)	14		20		30		ns
t _{MRF}	\overline{MR} HIGH to Flags Valid		14		20		30	ns
t _{AMR}	\overline{MR} HIGH to Data Outputs LOW		14		20		30	ns
t _{SMRP}	Program Mode— \overline{MR} LOW Set-Up	14		20		30		ns
t _{HMRP}	Program Mode— \overline{MR} LOW Hold	10		15		20		ns
t _{FTP}	Program Mode—Write HIGH to Read HIGH	14		20		30		ns
t _{AP}	Program Mode—Data Access Time		14		20		30	ns
t _{OHP}	Program Mode—Data Hold Time from \overline{MR} HIGH	0		0		0		ns

Notes:

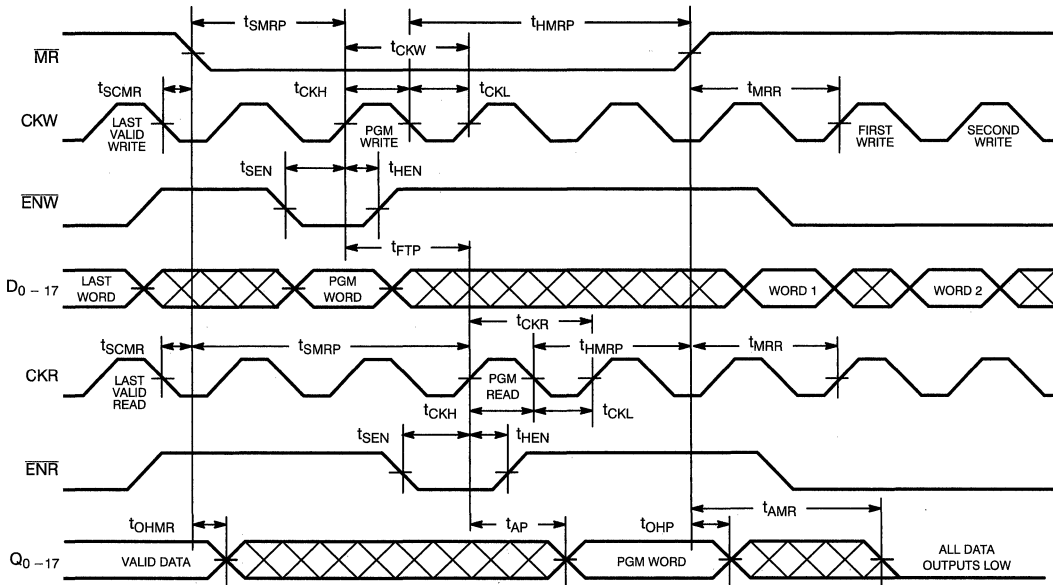
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and output loading as shown in AC Test Loads and Waveforms and capacitance as in notes 10 and 11, unless otherwise specified.
- At any given temperature and voltage condition, t_{OLZ} is greater than t_{OZH} for any given device.
- t_{SKEW1} is the minimum time an opposite clock can occur after a clock and still be guaranteed not to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW1} after the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. *Note:* The opposite clock is the signal to which a flag is not synchronized; i.e., CKW is the opposite

clock for Empty and Almost Empty flags, and CKR is the the opposite clock for the Almost Full, Half Full, and Full flags. The clock is the signal to which a flag is synchronized; i.e., CKW is the clock for the Half Full, Almost Full, and Full flags, and CKR is the clock for Empty and Almost Empty flags.

- t_{SKEW2} is the minimum time an opposite clock can occur before a clock and still be guaranteed to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW2} before the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. See Note 17 for definition of clock and opposite clock.

Switching Waveforms (continued)
Master Reset (Programming Mode) Timing Diagram^[21, 22]


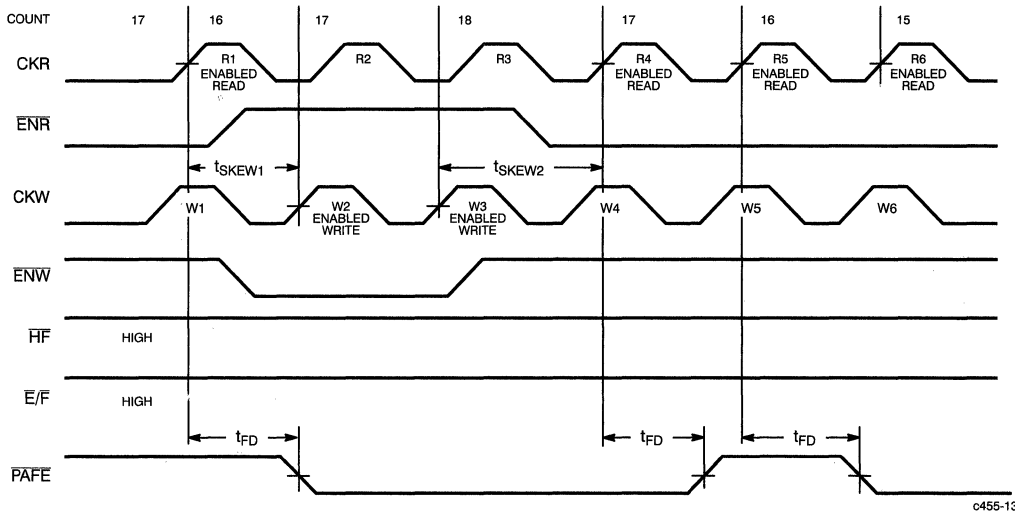
c455-9

Master Reset (Programming Mode with Free-Running Clocks) Timing Diagram^[21, 22]


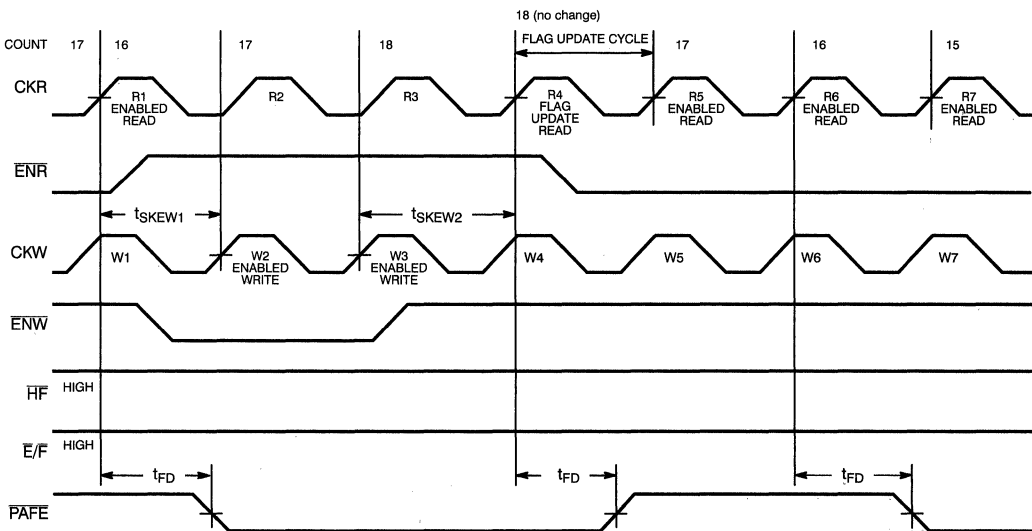
c455-10

Notes:

19. To only perform reset (no programming), the following criteria must be met: ENW or CKW must be inactive while MR is LOW.
20. To only perform reset (no programming), the following criteria must be met: ENR or CKR must be inactive while MR is LOW.
21. All data outputs (Q₀₋₁₇) go LOW as a result of the rising edge of \overline{MR} after t_{AMR}.
22. In this example, Q₀₋₁₇ will remain valid until t_{OHMR} if either the first read shown did not occur or if the read occurred soon enough such that the valid data was caused by it.

Switching Waveforms (continued)
Read to Almost Empty Timing Diagram with Free-Running Clocks^[23, 26, 28]


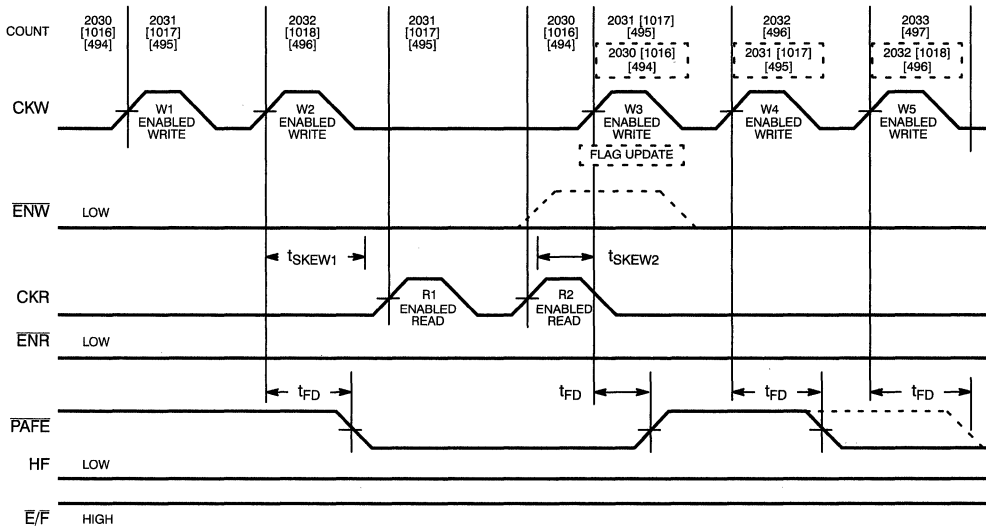
c455-13

Read to Almost Empty Timing Diagram with Read Flag Update Cycle with Free-Running Clocks^[23, 26, 28, 29, 30]


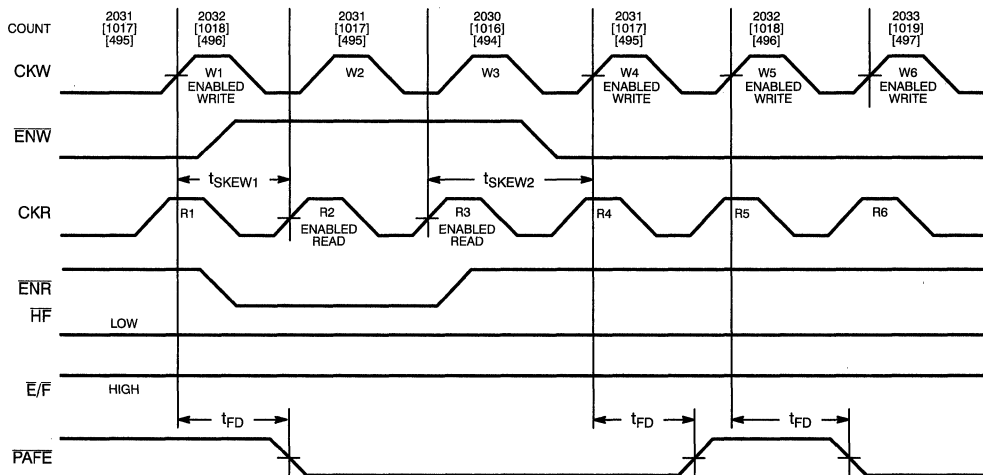
c455-14

Notes:

28. The FIFO in this example is assumed to be programmed to its default flag values. Almost Empty is 16 words from Empty; Almost Full is 16 locations from Full.
29. R4 only updates the flag status. It does not affect the count because ENR is HIGH.
30. When making the transition from Almost Empty to Intermediate, the count must increase by two (16 → 18; two enabled writes: W2, W3) before a read (R4) can update flags to the Less Than Half Full state.

Switching Waveforms (continued)
Write to Almost Full Timing Diagram^[23, 28, 31, 36, 37]


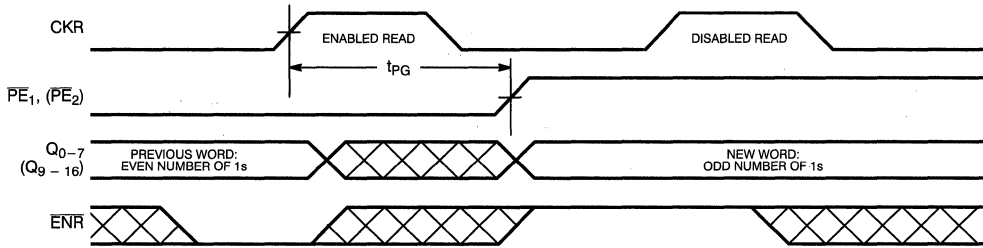
c455-17

Write to Almost Full Timing Diagram with Free-Running Clocks^[23, 28, 31]


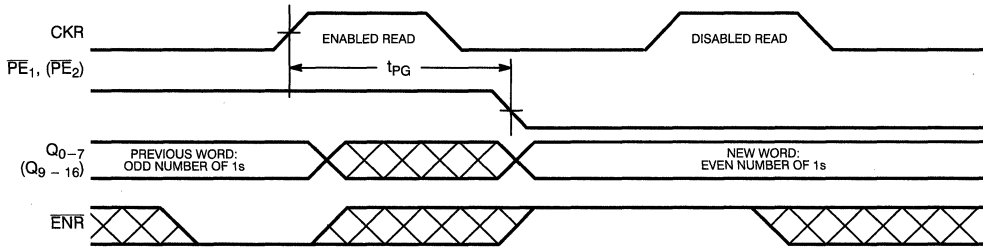
c455-18

Notes:

36. W2 updates the flag to the Almost Full state by asserting \overline{PAFE} . Because R1 occurs greater than t_{SKEW1} after W2, W2 does not recognize R1 when updating flag status. W3 includes R2 in the flag update because R2 occurs greater than t_{SKEW2} before W3. Note that W3 does not have to be enabled to update flags.
37. The dashed lines show W3 as a flag update write rather than an enabled write because ENW is HIGH.

Switching Waveforms (continued)
Even Parity Generation Timing Diagram^[39, 40]


c455-21

Even Parity Generation Timing Diagram^[39, 41]


c455-22

Notes:

39. In this example, the FIFO is assumed to be programmed to generate even parity. The **Q₀₋₇** word is shown. The example is similar for the **Q₉₋₁₆** word.

40. If **Q₀₋₇** "new word" also has an even number of 1s, then **PG1** stays LOW.

41. If **Q₀₋₇** "new word" also has odd number of 1s, then **PG1** stays HIGH.

Architecture

The CY7C45X consists of an array of 512, 1,024, or 2,048 words of 18 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (CKR, CKW, ENR, ENW, and MR), and flags (HF, E/F, PAFE). The CY7C45X also includes the control signals OE, FL, XI, and XO for depth expansion.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset (MR) cycle. This causes the FIFO to enter the Empty condition signified by E/F and PAFE being LOW and HF being HIGH. All data outputs (Q₀ – 17) go low at the rising edge of MR. In order for the FIFO to reset to its default state, a falling edge must occur on MR and the user must not read or write while MR is LOW (unless ENR and/or ENW are HIGH or unless the device is being programmed). Upon completion of the master reset cycle, all data outputs will go LOW t_{AMR} after MR is deasserted. All flags are guaranteed to be valid t_{MRF} after MR is taken HIGH.

FIFO Operation

When the ENW signal is active (LOW), data present on the D₀ – 17 pins is written into the FIFO on each rising edge of the CKW signal. Similarly, when the ENR signal is active, data in the FIFO memory will be presented on the Q₀ – 17 outputs. New data will be presented on each rising edge of CKR while ENR is active. ENR must set up t_{SEN} before CKR for it to be a valid read function. ENW must occur t_{SEN} before CKW for it to be a valid write function.

An output enable (OE) pin is provided to three-state the Q₀ – 17 outputs when OE is asserted. When OE is enabled (low), data in the output register will be available to the Q₀ – 17 outputs after t_{OE}. If devices are cascaded, the OE function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q₀ – 17 outputs even after additional reads occur.

Programming

The CY7C45X is programmed during a master reset cycle. If MR and ENW are LOW, a rising edge on CKW will write the D₀ – 9, 10 or 11 inputs into the programming register^[45]. MR must be set up a minimum of t_{SMP} before the program write rising edge and held

t_{HMRP} after the program write falling edge. The user has the ability to also perform a program read during the master reset cycle. This will occur at the rising edge of CKR when MR and ENR are asserted. The program read must be performed a minimum of t_{TRP} after a program write, and the program word will be available t_{AP} after the read occurs. If a program write does not occur, a program read may occur a minimum of t_{SMP} after MR is asserted. This will read the default program value.

When free-running clocks are tied to CKW and CKR, programming can still occur during a master reset cycle with the adherence to a few additional timing parameters. The enable pins must be set-up t_{SEN} before the rising edge of CKW or CKR. Hold times of t_{HEN} must also be met for ENW and ENR.

Data present on D₀ – 9 during a program write will determine the distance from Empty (Full) that the Almost Empty (Almost Full) flags will become active. See Table 1 for a description of the six possible FIFO states. P in Table 1 refers to the decimal equivalent of the binary number represented by D₀ – 7, 8 or 9. Programming options for the CY7C45X are listed in Table 4.

The programmable PAFE function on the CY7C45X is only valid when not cascaded. If the user elects not to program the FIFO's flags, the default is as follows: the Almost Empty condition (Almost Full condition) is activated when the FIFO contains 16 or less words (empty locations).

Parity is programmed with the D₁₅ – 17 bits. See Table 4 for a summary of the various parity programming options. Data present on D₁₅ – 17 during a program write will determine whether the FIFO will generate or check even/odd parity for the data present on D₀ – 7 and D₉ – 16 thereafter. If the user elects not to program the FIFO, the parity function is disabled. Flag operation and parity are described in greater detail in subsequent sections.

Flag Operation

The CY7C45X provides three status pins when not cascaded. The three pins, E/F, PAFE, and HF, allow decoding of six FIFO states (Table 1). PAFE is not available when the CY7C45X is cascaded for depth expansion. All flags are synchronous, meaning that the change of states is relative to one of the clocks (CKR or CKW, as appropriate).^[46] The Empty and Almost Empty flag states are exclusively updated by each rising edge of the read clock (CKR). For example, when the FIFO contains 1 word, the next read (rising edge of CKR while ENR = LOW) causes the flag pins to output a state that represents Empty. The Half Full, Almost Full, and Full flag states are updated exclusively by the write clock

Table 1. Flag Truth Table^[47]

E/F	PAFE	HF	State	7C455 Words in FIFO	7C456 Words in FIFO	7C457 Words in FIFO
0	0	1	Empty	0	0	0
1	0	1	Almost Empty	1 ♦ P	1 ♦ P	1 ♦ P
1	1	1	Less than or Equal to Half Full	P + 1 ♦ 256	P + 1 ♦ 512	P + 1 ♦ 1024
1	1	0	Greater than Half Full	257 ♦ 511 – P	513 ♦ 1023 – P	1025 ♦ 2047 – P
1	0	0	Almost Full	512 – P ♦ 511	1024 – P ♦ 1023	2048 – P ♦ 2047
0	0	0	Full	512	1024	2048

Notes:

45. CKW will write D₀ – 9 into the programming register. CKR will read D₀ – 9 during a programming register read.
 46. The synchronous architecture guarantees the flags valid for approximately one cycle of the clock they are synchronized to.

47. P is the decimal value of the binary number represented by D₀ – 7 for the CY7C455, D₀ – 8 for the CY7C456, and D₀ – 9 for the CY7C457. P = 0 signifies that the Almost Empty state = Empty state.



Table 2. Empty Flag (Boundary Flag) Operation Example

Status Before Operation					Operation	Status After Operation					Comments
Current State of FIFO	\overline{E}/F	\overline{A}/E	\overline{H}/F	Number of Words in FIFO		Next State of FIFO	\overline{E}/F	\overline{A}/E	\overline{H}/F	Number of words in FIFO	
Empty	0	0	1	0	Write ($\overline{ENW} = 0$)	Empty	0	0	1	1	Write
Empty	0	0	1	1	Write ($\overline{ENW} = 0$)	Empty	0	0	1	2	Write
Empty	0	0	1	2	Read ($\overline{ENR} = X$)	AE	1	0	1	2	Flag Update
AE	1	0	1	2	Read ($\overline{ENR} = 0$)	AE	1	0	1	1	Read
AE	1	0	1	1	Read ($\overline{ENR} = 0$)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)
Empty	0	0	1	0	Write ($\overline{ENR} = 0$)	Empty	0	0	1	1	Write
Empty	1	0	1	1	Read ($\overline{ENR} = X$)	AE	1	0	1	1	Flag Update
AE	1	0	1	1	Read ($\overline{ENR} = 0$)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)

Programmable Parity

Parity Disabled (Q_8/Q_{17} mode)

When parity is disabled (or the user does not program parity option) the FIFO stores all 18 bits present on $D_0 - 17$ inputs internally and will output all 18 bits on $Q_0 - 17$.

Parity Generate (PG mode)

This mode is used to generate either even or odd parity (as programmed) from $D_0 - 7$ and $D_0 - 16$. D_8 and D_{17} inputs are ignored. The parity bits are stored internally as D_8 and D_{17} , and during a subsequent read will be available on the PG1 and PG2 pins along with the data words from which the parity was generated ($Q_0 - 7$ and $Q_9 - 16$). For example, if parity generate is set to ODD and the $D_0 - 7$ inputs have an EVEN number of 1s, PG1 will be HIGH.

Parity Check (\overline{PE} mode)

If the FIFO is programmed for parity checking, it will compare the parity of $D_0 - 8$ and $D_9 - 17$ with the program register. For example, D_8 and D_{17} will be set according to the result of the parity check on each word. When these words are later read, \overline{PE}_1 and \overline{PE}_2 will reflect the result of the parity check. If a parity error occurs in $D_0 - 8$, D_8 will be set LOW internally. When this word is later read, \overline{PE}_1 will be LOW.

Width Expansion Modes

During width expansion all flags (programmable and nonprogrammable) are available. These FIFOs can be expanded in width to provide word width greater than 18 in increments of 18. During width expansion mode all control line inputs are common. When the FIFO is being read near the Empty (Full) boundary, it is important to note that both sets of flags should be checked to see if they have been updated to the Not Empty (Not Full) condition to insure that the next read (write) will perform the same operation on all devices.

Checking all sets of flags is critical so that data is not read from the FIFOs "staggered" by one clock cycle. This situation could occur when the first write to an empty FIFO and a read are very close together. If the read occurs less than t_{SKEW2} after the first write to two width-expanded devices, A and B, device A may go Almost

Empty (read recognized as flag update) while device B stays Empty (read ignored). This occurs because a read can be either recognized or ignored if it occurs within t_{SKEW2} of a write. The next read cycle outputs the first half of the first word on device A while device B updates its flags to Almost Empty. Subsequent reads will continue to output "staggered" data assuming more data has been written to FIFOs.

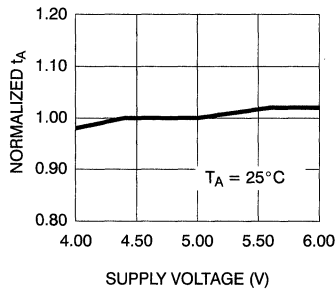
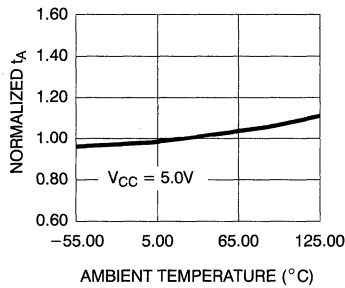
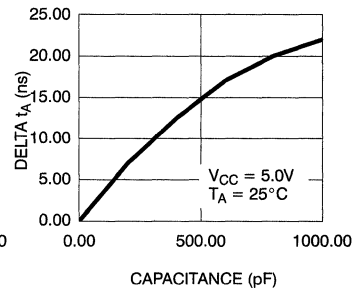
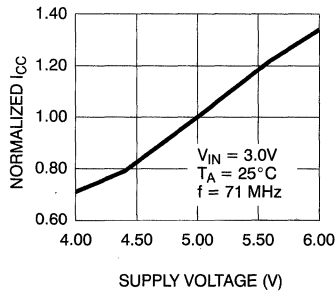
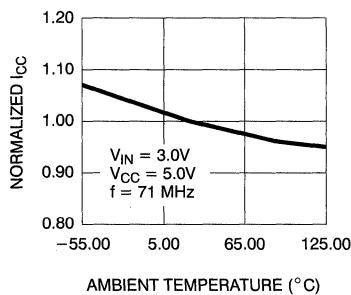
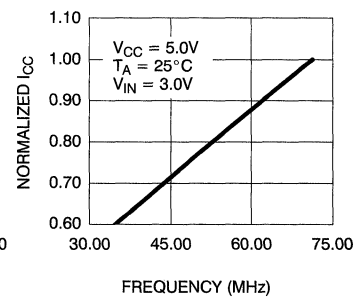
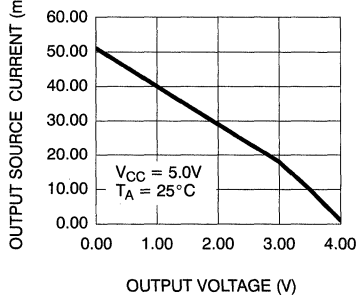
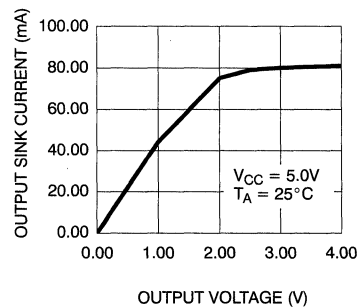
Depth Expansion Mode

The CY7C45X can operate up to 50 MHz when cascaded. Depth expansion is accomplished by connecting expansion out (\overline{XO}) of the first device to expansion in (\overline{XI}) of the next device, with \overline{XO} of the last device connected to \overline{XI} of the first device. The first device has its first load pin (\overline{FL}) tied to V_{SS} while all other devices must have this pin tied to V_{CC} . The first device will be the first to be write and read enabled after a master reset.

Proper operation also requires that all cascaded devices have common CKW, CKR, \overline{ENW} , \overline{ENR} , $D_0 - 17$, $Q_0 - 17$, and \overline{MR} pins. When cascaded, one device at a time will be read enabled so as to avoid bus contention. By asserting \overline{XO} when appropriate, the currently enabled FIFO alerts the next FIFO that it should be enabled. The next rising edge on CKR puts $Q_0 - 17$ outputs of the first device into a high-impedance state. This occurs regardless of the state of \overline{ENR} or the next FIFO's Empty flag. Therefore, if the next FIFO is empty or undergoing a latent cycle, the $Q_0 - 17$ bus will be in a high-impedance state until the next device receives its first read, which brings its data to the $Q_0 - 17$ bus.

Program Write/Read of Cascaded Devices

Programming of cascaded FIFOs is the same as for a single device. Because the controls of the FIFOs are in parallel when cascaded, they all get programmed the same. During program mode, only parity is programmed since Almost Full and Almost Empty flags are not available when CY7C45X is cascaded. Only the "first device" (FIFO with $\overline{FL} = \text{LOW}$) will output its program register contents on $Q_0 - 17$ during a program read. $Q_0 - 17$ of all other devices will remain in a high-impedance state to avoid bus contention.

Typical AC and DC Characteristics
NORMALIZED t_A vs. SUPPLY VOLTAGE

NORMALIZED t_A vs. AMBIENT TEMPERATURE

TYPICAL t_A CHANGE vs. OUTPUT LOADING

NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE

NORMALIZED SUPPLY CURRENT vs. FREQUENCY

OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE




CYPRESS

CY7C460
CY7C462
CY7C464

Cascadable 8K x 9 FIFO
Cascadable 16K x 9 FIFO
Cascadable 32K x 9 FIFO

Features

- 8K x 9 FIFO (CY7C460)
- 16K x 9 FIFO (CY7C462)
- 32K x 9 FIFO (CY7C464)
- Asynchronous read/write
- High-speed 33.3-MHz read/write independent of depth/width
- Low operating power
— I_{CC} = 70 mA (max.)
- Half Full flag in standalone
- Empty and Full flags
- Retransmit in standalone
- Expandable in width and depth
- 5V ± 10% supply
- PLCC, LCC, and 600-mil DIP packaging
- TTL compatible
- Three-state outputs
- Pin compatible and functionally equivalent to IDT7205, IDT7206

Functional Description

The CY7C460, CY7C462, and CY7C464 are respectively, 8K, 16K, and 32K words by 9-bit wide first-in-first-out (FIFO) memories. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays, so that throughput is not reduced. Data is steered in a similar manner.

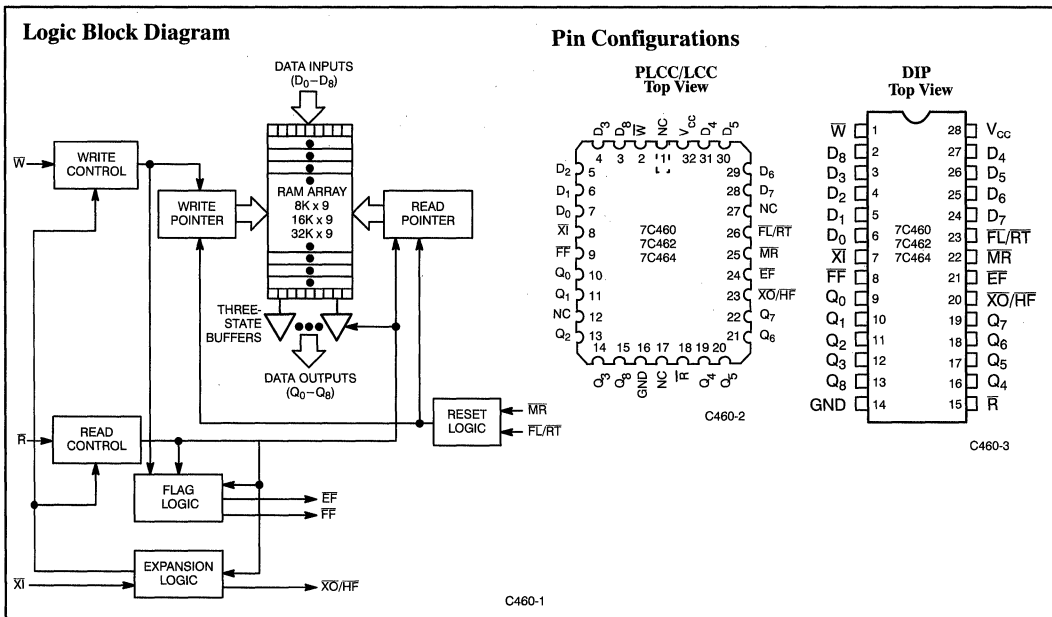
The read and write operations may be asynchronous; each can occur at a rate of 33.3 MHz. The write operation occurs when the write (W) signal is LOW. Read occurs when read (R) goes LOW. The nine

data outputs go to the high-impedance state when R is HIGH.

A Half Full (HF) output flag is provided that is valid in the standalone (single device) and width expansion configurations. In the depth expansion configuration, this pin provides the expansion out (XO) information that is used to tell the next FIFO that it will be activated.

In the standalone and width expansion configurations, a LOW on the retransmit (RT) input causes the FIFOs to retransmit the data. Read enable (R) and write enable (W) must both be HIGH during a retransmit cycle, and then R is used to access the data.

The CY7C460, CY7C462, and CY7C464 are fabricated using an advanced 0.8-micron N-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by careful layout, guard rings, and a substrate bias generator.

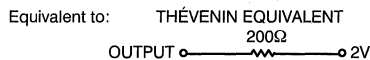
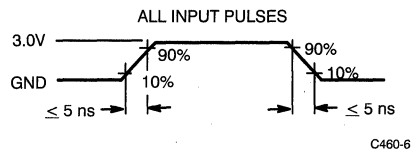
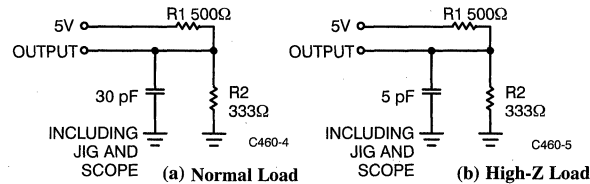


Electrical Characteristics Over the Operating Range (continued)^[2]

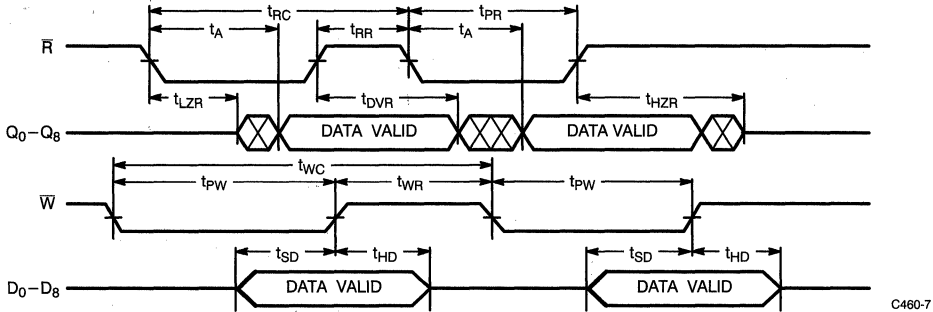
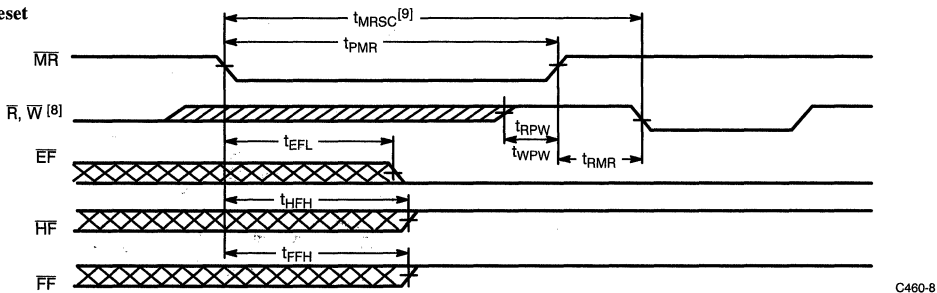
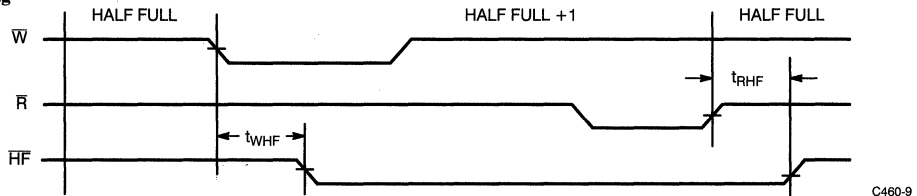
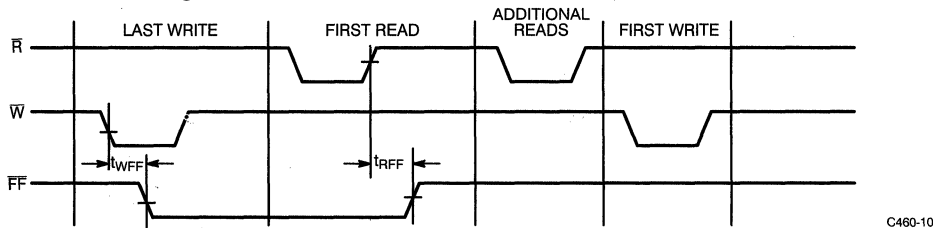
Parameter	Description	Test Conditions	7C460-40 7C462-40 7C464-40		7C460-65 7C462-65 7C464-65		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -2.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4	0.4		V
V _{IH}	Input HIGH Voltage		Com'l	2.2	2.2		V
			Mil/Ind	2.2	2.2		
V _{IL}	Input LOW Voltage			0.8	0.8		V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	R ≥ V _{IH} , GND ≤ V _O ≤ V _{CC}	-10	+10	-10	+10	μA
I _{CC}	Operating Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	70	70		mA
			Mil/Ind	75			
I _{SB1}	Standby Current	All Inputs = V _{IH} Min.	Com'l	25	25		mA
			Mil/Ind	30	30		
I _{SB2}	Power-Down Current	All Inputs V _{CC} - 0.2V	Com'l	20	20		mA
			Mil/Ind	25	25		
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-90	-90		mA

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 4.5V	10	pF
C _{OUT}	Output Capacitance		12	pF

AC Test Loads and Waveforms

Notes:

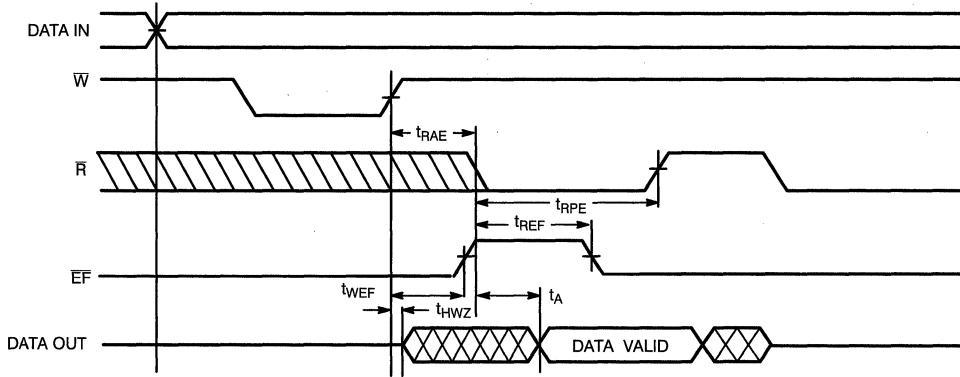
- Tested initially and after any design or process changes that may affect these parameters.

Switching Waveforms^[7]
Asynchronous Read and Write

Master Reset

Half Full Flag

Last Write to First Read Full Flag

Notes:

7. A HIGH-to-LOW transition of either the write or read strobe causes a HIGH-to-LOW transition of the responding flag. Correspondingly, a LOW-to-HIGH strobe transition causes a LOW-to-HIGH flag transition.
8. \bar{W} and $\bar{R} = V_{IH}$ around the rising edge of \bar{MR} .
9. $t_{MRSC} = t_{PMR} + t_{RMR}$.

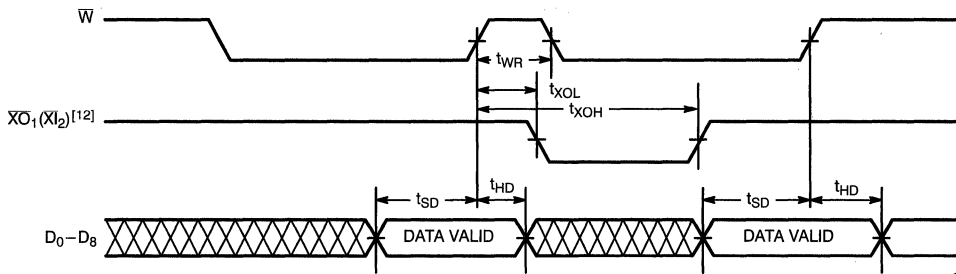
Switching Waveforms (continued)

Empty Flag and Read Data Flow-Through Mode

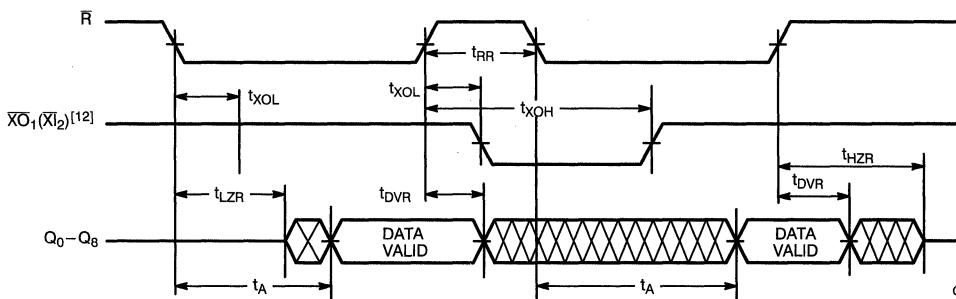


C460-14

Expansion Timing Diagrams



C460-15



C460-16

Note:

12. Expansion out of device 1 (\overline{XO}_1) is connected to expansion in of device 2 (\overline{XI}_2).

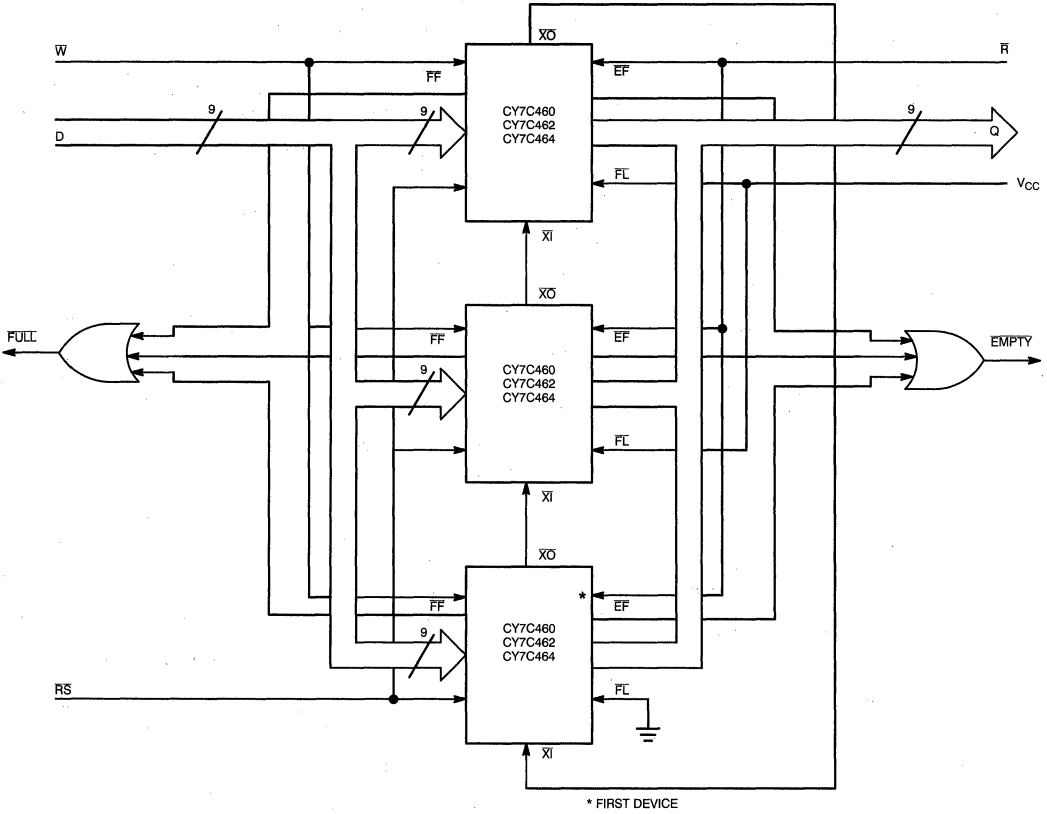


Figure 1. Depth Expansion

C460-17

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C460-15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C460-15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C460-20DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C460-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C460-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C460-25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460-25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C460-25DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C460-25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C460-40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C460-40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460-40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C460-40DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C460-40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C460-65JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C460-65PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460-65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C462-15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C462-15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C462-20DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C462-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C462-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C462-25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462-25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C462-25DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C462-25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C462-40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C462-40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462-40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C462-40DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C462-40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C462-65JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C462-65PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462-65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial



MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{Ix}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3
I _{OS}	1, 2, 3
I _{OZ}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{RC}	9, 10, 11
t _A	9, 10, 11
t _{RR}	9, 10, 11
t _{PR}	9, 10, 11
t _{LZR}	9, 10, 11
t _{DVR}	9, 10, 11
t _{HZR}	9, 10, 11
t _{WC}	9, 10, 11
t _{PW}	9, 10, 11
t _{HWZ}	9, 10, 11
t _{WR}	9, 10, 11
t _{SD}	9, 10, 11
t _{HD}	9, 10, 11
t _{MRSC}	9, 10, 11
t _{PMR}	9, 10, 11
t _{RMR}	9, 10, 11
t _{RPW}	9, 10, 11
t _{WPW}	9, 10, 11
t _{RTC}	9, 10, 11
t _{PRT}	9, 10, 11
t _{RTR}	9, 10, 11
t _{EFL}	9, 10, 11
t _{HFH}	9, 10, 11
t _{FFH}	9, 10, 11
t _{REF}	9, 10, 11
t _{RFF}	9, 10, 11
t _{WEF}	9, 10, 11
t _{WFF}	9, 10, 11
t _{WHF}	9, 10, 11
t _{RHF}	9, 10, 11
t _{RAE}	9, 10, 11
t _{RPE}	9, 10, 11
t _{WAF}	9, 10, 11
t _{WPF}	9, 10, 11
t _{XOL}	9, 10, 11
t _{XOH}	9, 10, 11

Document #: 38-00141-G



Selection Guide

		7C470-15 7C472-15 7C474-15	7C470-20 7C472-20 7C474-20	7C470-25 7C472-25 7C474-25	7C470-40 7C472-40 7C474-40
Frequency (MHz)		33.3	33.3	28.5	20
Maximum Access Time (ns)		15	20	25	40
Maximum Operating Current (mA)	Commercial	105		90	70
	Military/Industrial		110	95	75

Maximum Ratings

Storage Temperature -65°C to +150°C
 Ambient Temperature with
 Power Applied -55°C to +125°C
 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Voltage Applied to Outputs
 in High Z State -0.5V to +7.0V
 DC Input Voltage -3.0V to +7.0V
 Power Dissipation 1.0W
 Output Current, into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)
 Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Military ^[1]	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[2]

Parameter	Description	Test Conditions	7C470-15 7C472-15 7C474-15		7C470-20 7C472-20 7C474-20		7C470-25 7C472-25 7C474-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -2.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		Com'l	2.2			2.2		V
			Mil/Ind			2.2		2.2	
V _{IL}	Input LOW Voltage			0.8		0.8		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	-10	+10	µA
I _{OZ}	Output Leakage Current	R̄ ≥ V _{IH} , GND ≤ V _O ≤ V _{CC}	-10	+10	-10	+10	-10	+10	µA
I _{CC}	Operating Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	105				90	mA
			Mil/Ind			110		95	
I _{SB1}	Standby Current	All Inputs = V _{IH} Min.	Com'l	25				25	mA
			Mil/Ind			30		30	
I _{SB2}	Power-Down Current	All Inputs = V _{CC} - 0.2V	Com'l	20				20	mA
			Mil/Ind			25		25	
I _{OS} ^[3]	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = GND		-90		-90		-90	mA

Notes:

- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.



Switching Characteristics Over the Operating Range^[5, 6]

Parameter	Description	7C470-15 7C472-15 7C474-15		7C470-20 7C472-20 7C474-20		7C470-25 7C472-25 7C474-25		7C470-40 7C472-40 7C474-40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{CY}	Cycle Time	30		30		35		50		ns
t _A	Access Time		15		20		25		40	ns
t _{RV}	Recovery Time	15		10		10		10		ns
t _{PW}	Pulse Width	15		20		25		40		ns
t _{LZR}	Read LOW to Low Z	3		3		3		3		ns
t _{DV} ^[7]	Valid Data from Read HIGH	3		3		3		3		ns
t _{HZ} ^[7]	Read HIGH to High Z		15		15		18		25	ns
t _{HWZ}	Write HIGH to Low Z	5		5		5		5		ns
t _{SD}	Data Set-Up Time	11		12		15		20		ns
t _{HD}	Data Hold Time	0		0		0		0		ns
t _{EFD}	$\overline{E}/\overline{F}$ Delay		15		20		25		40	ns
t _{EFL}	$\overline{M}R$ to $\overline{E}/\overline{F}$ LOW		25		30		35		50	ns
t _{HFD}	$\overline{H}F$ Delay		25		30		35		50	ns
t _{AFED}	$\overline{P}A\overline{F}E$ Delay		25		30		35		50	ns
t _{RAE}	Effective Read from Write HIGH	15		20		25		40		ns
t _{WAF}	Effective Write from Read HIGH	15		20		25		40		ns

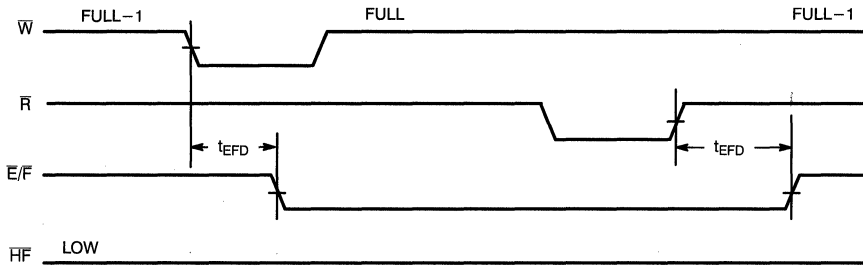
Notes:

- Test conditions assume signal transmission time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in part (a) of AC Test Load and Waveforms, unless otherwise specified.
- See the last page of this specification for Group A subgroup testing information.
- t_{HZR} and t_{PVR} use capacitance loading as in part (b) of AC Test Loads. t_{HZR} transition is measured at +500 mV from V_{OL} and -500 mV from V_{OH}. t_{PVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.



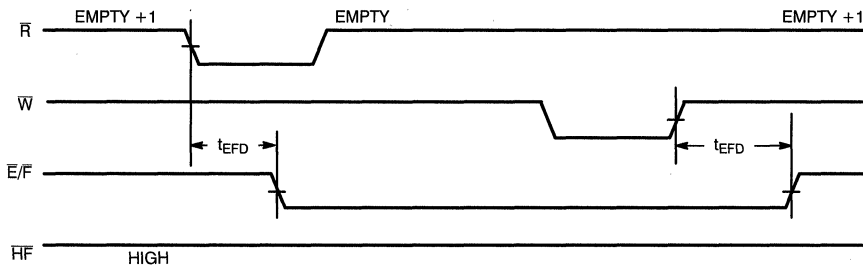
Switching Waveforms (continued)

$\overline{E}/\overline{F}$ Flag (Last Write to First Read Full Flag)



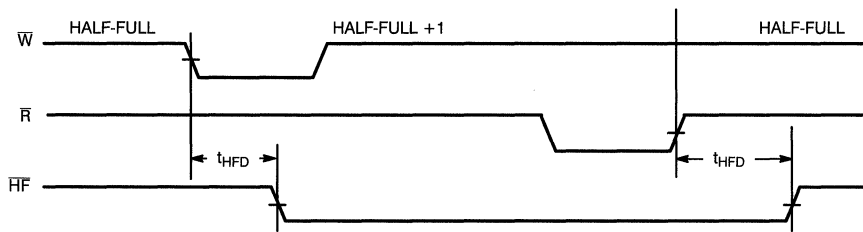
7C470-10

$\overline{E}/\overline{F}$ Flag (Last Read to First Write Empty Flag)



7C470-11

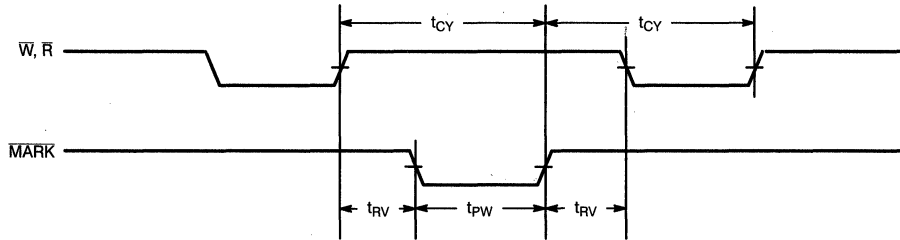
Half Full Flag



7C470-12

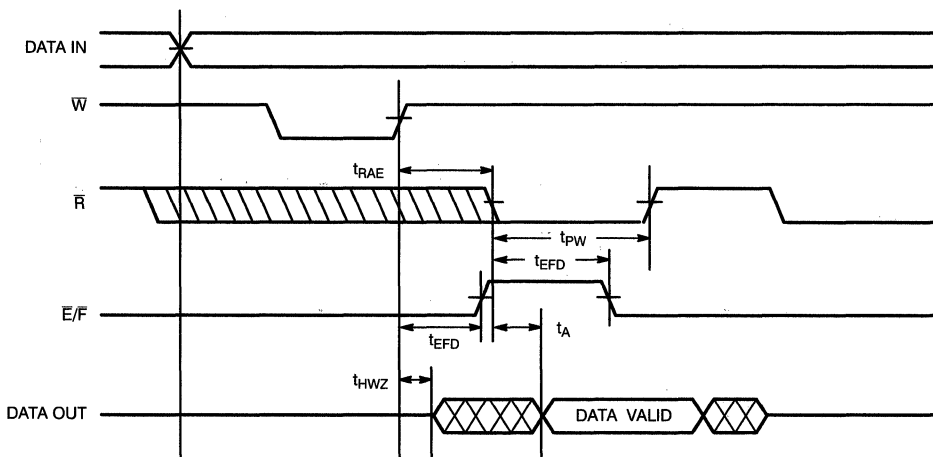
Switching Waveforms (continued)

Mark



7C470-16

Empty Flag and Read Data Flow-Through Mode



7C470-17



Table 1. Flag Truth Table^[13]

HF	E/F	PAFE	State	CY77C470 (8K x 9) Number of Words in FIFO	CY77C472 (16K x 9) Number of Words in FIFO	CY77C474 (32K x 9) Number of Words in FIFO
1	0	0	Empty	0	0	0
1	1	0	Almost Empty	1 \blacklozenge (P - 1)	1 \blacklozenge (P - 1)	1 \blacklozenge (P - 1)
1	1	1	Less than Half Full	P \blacklozenge 4096	P \blacklozenge 8192	P \blacklozenge 16384
0	1	1	Greater than Half Full	4097 \blacklozenge (8192 - P)	8193 \blacklozenge (16384 - P)	16385 \blacklozenge (32768 - P)
0	1	0	Almost Full	(8192 - P + 1) \blacklozenge 8191	(16384 - P + 1) \blacklozenge 16383	(32768 - P + 1) \blacklozenge 32767
0	0	0	Full	8192	16384	32768

Table 2. Programmable Almost Full/Empty Options^[14]

D3	D2	D1	D0	PAFE Active when:	P
0	0	0	0	256 or less locations from Empty/Full (default)	256
0	0	0	1	16 or less locations from Empty/Full	16
0	0	1	0	32 or less locations from Empty/Full	32
0	0	1	1	64 or less locations from Empty/Full	64
0	1	0	0	128 or less locations from Empty/Full	128
0	1	0	1	256 or less locations from Empty/Full (default)	256
0	1	1	0	512 or less locations from Empty/Full	512
0	1	1	1	1024 or less locations from Empty/Full	1024
1	0	0	0	2048 or less locations from Empty/Full	2048
1	0	0	1	4098 or less locations from Empty/Full ^[15]	4098
1	0	1	0	8192 or less locations from Empty/Full ^[16]	8192

Notes:

13. See Table 2 for P values.

14. Almost flags default to 256 locations from Empty/Full.

15. Only for CY7C472 and CY7C474.

16. Only for CY7C470.



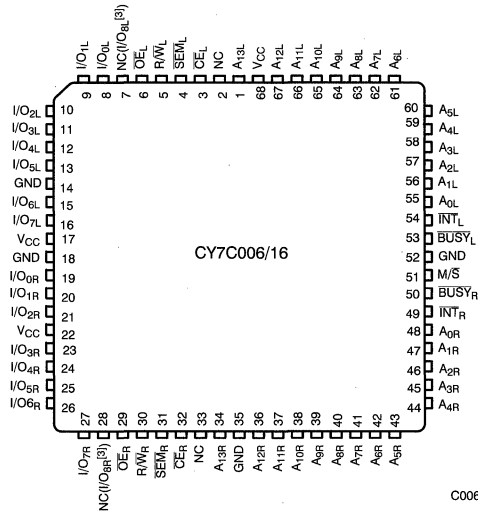
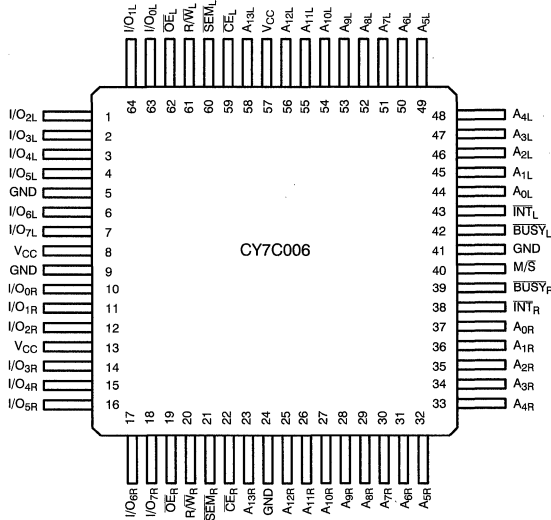
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C470-15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C470-15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C470-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C470-20DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C470-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C470-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C470-25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C470-25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C470-25DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C470-25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C470-40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C470-40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C470-40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C470-40DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C470-40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C472-15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C472-15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C472-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C472-20DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C472-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C472-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C472-25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C472-25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C472-25DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C472-25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C472-40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C472-40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C472-40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C472-40DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C472-40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Dual-Port Memories
Page Number

Device	Description	Page Number
CY7C006	16K x 8 Dual-Port Static RAM with Sem, Int, Busy	6-1
CY7C016	16K x 9 Dual-Port Static RAM with Sem, Int, Busy	6-1
CY7C024	4K x 16 Dual-Port Static RAM with Sem, Int, Busy	6-18
CY7C0241	4K x 18 Dual-Port Static RAM with Sem, Int, Busy	6-18
CY7C025	8K x 16 Dual-Port Static RAM with Sem, Int, Busy	6-18
CY7C0251	8K x 18 Dual-Port Static RAM with Sem, Int, Busy	6-18
CY7C130	1K x 8 Dual-Port Static RAM	6-37
CY7C131	1K x 8 Dual-Port Static RAM	6-37
CY7C140	1K x 8 Dual-Port Static RAM	6-37
CY7C141	1K x 8 Dual-Port Static RAM	6-37
CY7C132	2K x 8 Dual-Port Static RAM	6-50
CY7C136	2K x 8 Dual-Port Static RAM	6-50
CY7C142	2K x 8 Dual-Port Static RAM	6-50
CY7C146	2K x 8 Dual-Port Static RAM	6-50
CY7C133	2K x 16 Dual-Port Static RAM	6-63
CY7C143	2K x 16 Dual-Port Static RAM	6-63
CY7B134	4K x 8 Dual-Port Static RAM	6-74
CY7B135	4K x 8 Dual-Port Static RAM	6-74
CY7B1342	4K x 8 Dual-Port Static RAM with Semaphores	6-74
CY7B138	4K x 8 Dual-Port Static RAM with Sem, Int, Busy	6-87
CY7B139	4K x 9 Dual-Port Static RAM with Sem, Int, Busy	6-87
CY7B144	8K x 8 Dual-Port Static RAM with Sem, Int, Busy	6-103
CY7B145	8K x 9 Dual-Port Static RAM with Sem, Int, Busy	6-103

Pin Configurations
**68-Pin LCC/PLCC
Top View**

**64-Pin TQFP
Top View**


Note:
3. I/O for 7C016 only.



Selection Guide

	7C006-15 7C016-15	7C006-25 7C016-25	7C006-35 7C016-35	7C006-55 7C016-55
Maximum Access Time (ns)	15	25	35	55
Maximum Operating Current (mA)	260	220	210	200
Maximum Standby Current for I _{SB1} (mA)	70	60	50	40

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature -65°C to +150°C
- Ambient Temperature with Power Applied -55°C to +125°C
- Supply Voltage to Ground Potential -0.5V to +7.0V
- DC Voltage Applied to Outputs in High Z State -0.5V to +7.0V
- DC Input Voltage^[4] -0.5V to +7.0V
- Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

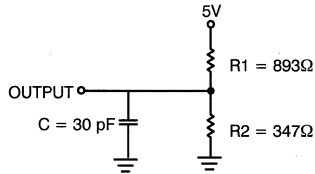
Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

Note:

- 4. Pulse width < 20 ns.

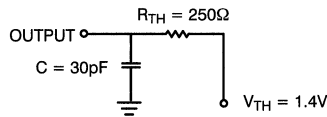
Capacitance^[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{V}$	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms


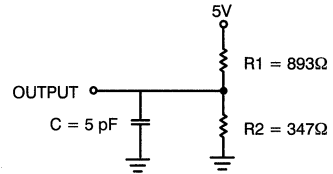
(a) Normal Load (Load 1)

C006-5



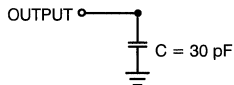
(b) Thévenin Equivalent (Load 1)

C006-6



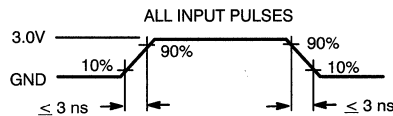
(c) Three-State Delay (Load 3)

C006-7



Load (Load 2)

C006-8



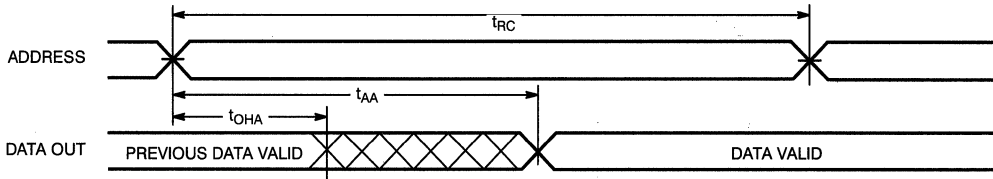
C006-9

Switching Characteristics Over the Operating Range^[5, 8]

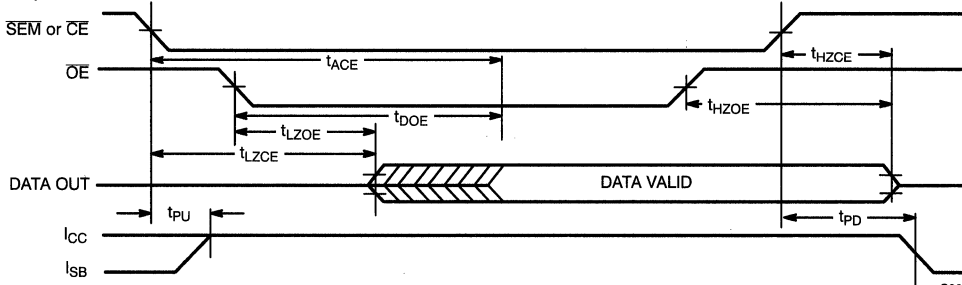
Parameter	Description	7C006-15 7C016-15		7C006-25 7C016-25		7C006-35 7C016-35		7C006-55 7C016-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15		25		35		55		ns
t_{AA}	Address to Data Valid		15		25		35		55	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		ns
t_{ACE}	\overline{CE} LOW to Data Valid		15		25		35		55	ns
t_{DOE}	\overline{OE} LOW to Data Valid		10		13		20		25	ns
$t_{LZOE}^{[9,10]}$	\overline{OE} Low to Low Z	3		3		3		3		ns
$t_{HZOE}^{[9,10]}$	\overline{OE} HIGH to High Z		10		15		15		25	ns
$t_{LZCE}^{[9,10]}$	\overline{CE} LOW to Low Z	3		3		3		3		ns
$t_{HZCE}^{[9,10]}$	\overline{CE} HIGH to High Z		10		15		15		25	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		15		25		35		55	ns

Notes:

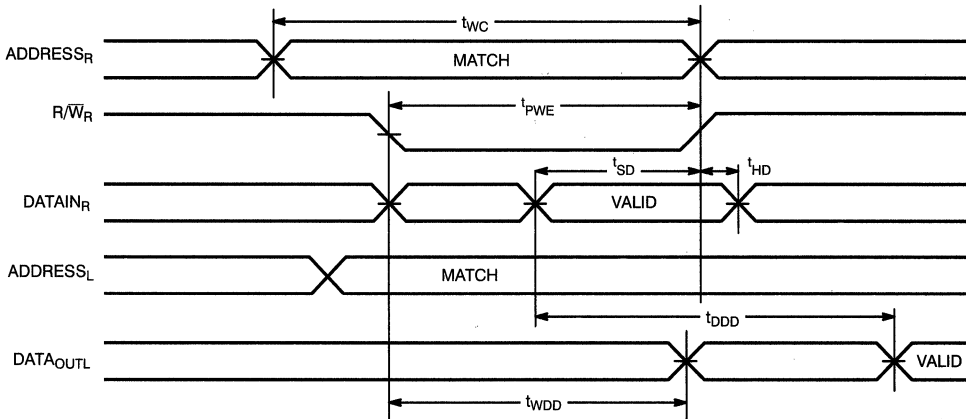
- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OI}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE} .
- Test conditions used are Load 3.

Switching Waveforms
Read Cycle No. 1 (Either Port Address Access)^[15, 16]


C006-10

Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access)^[15, 17, 18]


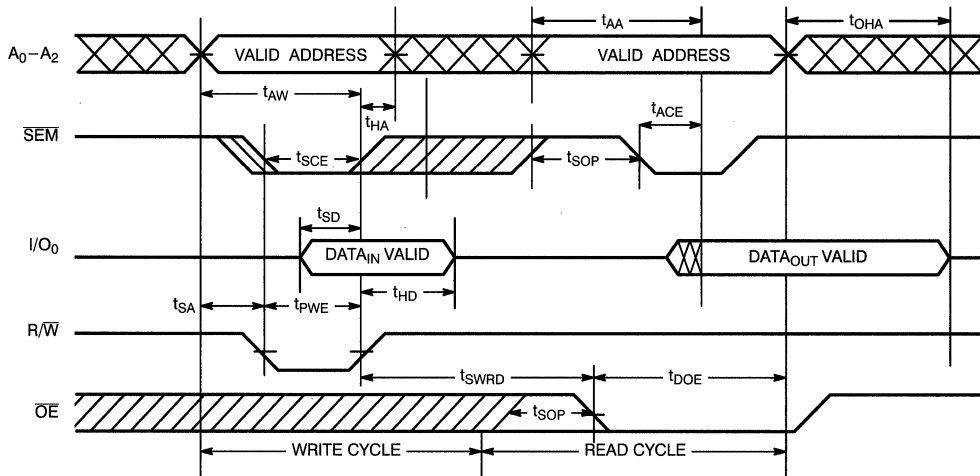
C006-11

Read Timing with Port-to-Port Delay ($M/\overline{S} = L$)^[19, 20]


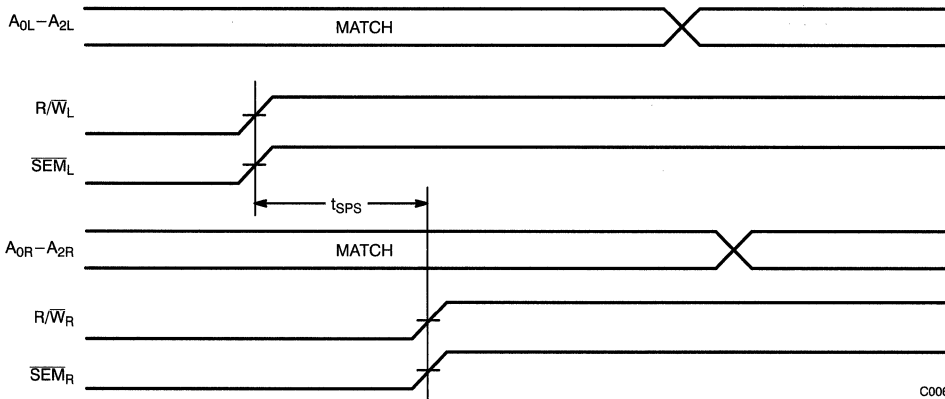
C006-12

Notes:

15. R/\overline{W} is HIGH for read cycle.
16. Device is continuously selected $\overline{CE} = \text{LOW}$ and $\overline{OE} = \text{LOW}$. This waveform cannot be used for semaphore reads.
17. Address valid prior to or coincident with \overline{CE} transition LOW.
18. $\overline{CE}_L = L, \overline{SEM} = H$ when accessing RAM. $\overline{CE} = H, \overline{SEM} = L$ when accessing semaphores.
19. $\overline{BUSY} = \text{HIGH}$ for the writing port.
20. $\overline{CE}_L = \overline{CE}_R = \text{LOW}$.

Switching Waveforms (continued)
Semaphore Read After Write Timing, Either Side^[25]


C006-15

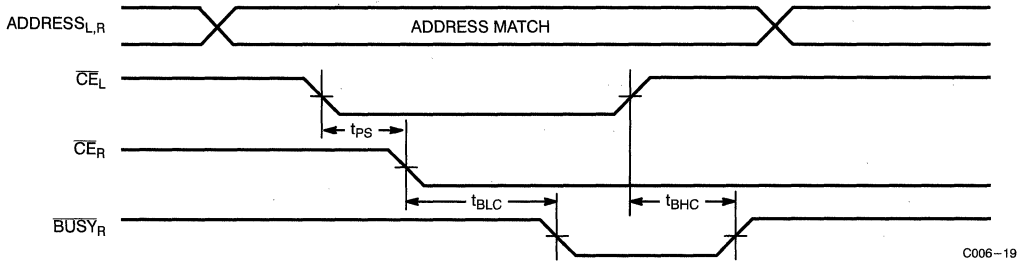
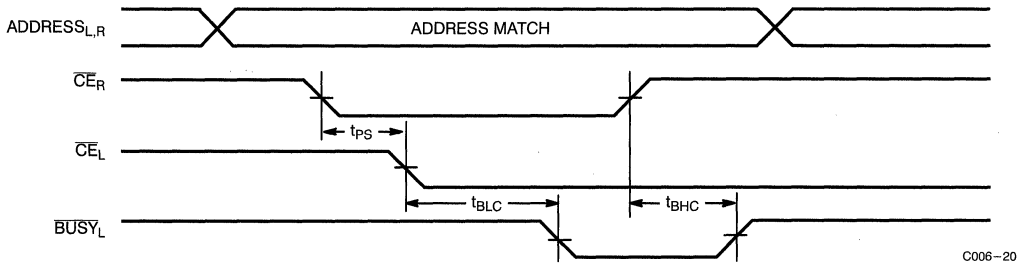
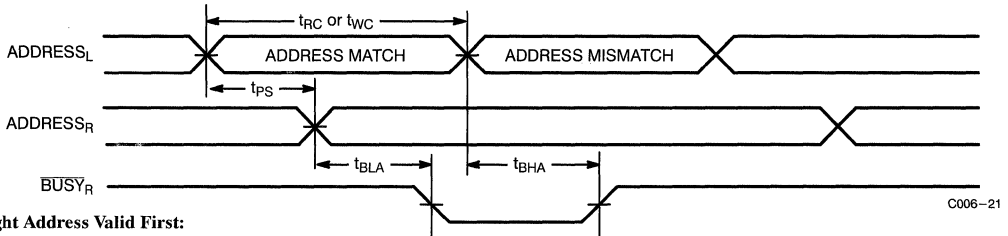
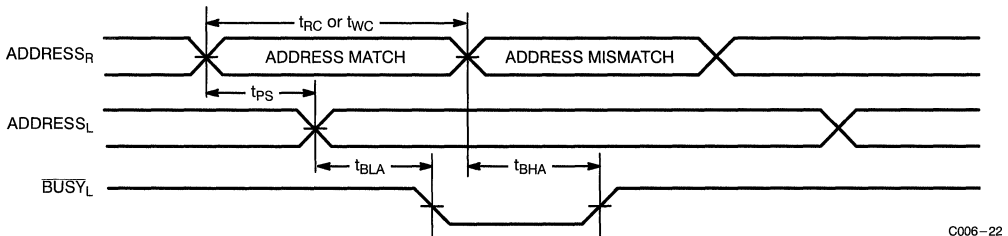
Semaphore Contention^[26, 27, 28]


C006-16

Notes:

25. \overline{CE} = HIGH for the duration of the above timing (both write and read cycle).
 26. $I/O_{0R} = I/O_{0L} = \text{LOW}$ (request semaphore); $\overline{CE}_R = \overline{CE}_L = \text{HIGH}$
 27. Semaphores are reset (available to both ports) at cycle start.

28. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Switching Waveforms (continued)
Busy Timing Diagram No. 1 (\overline{CE} Arbitration)^[29]
 \overline{CE}_L Valid First:

 \overline{CE}_R Valid First:

Busy Timing Diagram No. 2 (Address Arbitration)^[29]
Left Address Valid First:

Right Address Valid First:

Note:

29. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side \overline{BUSY} will be asserted.

30. t_{HA} depends on which enable pin (\overline{CE}_L or R/\overline{W}_L) is deasserted first.

31. t_{INS} or t_{INR} depends on which enable pin (\overline{CE}_L or R/\overline{W}_L) is asserted last.

Architecture

The CY7C006/016 consists of an array of 16K words of 8/9 bits each of dual-port RAM cells, I/O and address lines, and control signals (\overline{CE} , \overline{OE} , R/\overline{W}). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a \overline{BUSY} pin is provided on each port. Two interrupt (\overline{INT}) pins can be utilized for port-to-port communication. Two semaphore (\overline{SEM}) control pins are used for allocating shared resources. With the M/\overline{S} pin, the CY7C006/016 can function as a Master (\overline{BUSY} pins are outputs) or as a slave (\overline{BUSY} pins are inputs). The CY7C006/016 has an automatic power-down feature controlled by \overline{CE} . Each port is provided with its own output enable control (\overline{OE}), which allows data to be read from the device.


Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/\overline{W} in order to guarantee a valid write. A write operation is controlled by either the \overline{OE} pin (see Write Cycle No.1 waveform) or the R/\overline{W} pin (see Write Cycle No.2 waveform). Data can be written to the device t_{HZOE} after the \overline{OE} is deasserted or t_{HZWE} after the falling edge of R/\overline{W} . Required inputs for non-contention operations are summarized in Table 1.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DD} after the data is presented on the other port.

Table 1. Non-Contending Read/Write

Inputs				Outputs	
\overline{CE}	R/\overline{W}	\overline{OE}	\overline{SEM}	I/O_{0-7}	Operation
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read Data in Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H		X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Read Operation

When reading the device, the user must assert both the \overline{OE} and \overline{CE} pins. Data will be available t_{ACE} after \overline{CE} or t_{DOE} after \overline{OE} are asserted. If the user of the CY7C006/016 wishes to access a semaphore flag, then the \overline{SEM} pin must be asserted instead of the \overline{CE} pin.

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L = \overline{BUSY}_R = \text{HIGH}$)

Function	Left Port					Right Port				
	R/\overline{W}	\overline{CE}	\overline{OE}	A_{0L-13L}	\overline{INT}	R/\overline{W}	\overline{CE}	\overline{OE}	A_{0R-13R}	\overline{INT}
Set Left \overline{INT}	X	X	X	X	L	L	L	X	3FFE	X
Reset Left \overline{INT}	X	L	L	3FFE	H	X	L	L	X	X
Set Right \overline{INT}	L	L	X	3FFE	X	X	X	X	X	L
Reset Right \overline{INT}	X	X	X	X	X	X	L	L	3FFE	H

Interrupts

The interrupt flag (\overline{INT}) permits communications between ports. When the left port writes to location 3FFE(HEX), the right port's interrupt flag (\overline{INT}_R) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag (\overline{INT}_L) is accomplished when the right port writes to location 3FFE(HEX). This flag is cleared when the left port reads location 3FFE(HEX). The message at 3FFE(HEX) is user-defined. See Table 2 for input requirements for \overline{INT} . \overline{INT}_R and \overline{INT}_L are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7C006/016 provides on-chip arbitration to alleviate simultaneous memory location access (contention). If both ports' \overline{CE} s are asserted and an address match occurs within t_{PS} of each other the Busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. \overline{BUSY} will be asserted t_{BLA} after an address match or t_{BLC} after \overline{CE} is taken LOW. \overline{BUSY}_L and \overline{BUSY}_R in master mode are push-pull outputs and do not require pull-up resistors to operate.

Master/Slave

An M/\overline{S} pin is provided in order to expand the word width by configuring the device as either a master or a slave. The \overline{BUSY} output of the master is connected to the \overline{BUSY} input of the slave. This will allow the device to interface to a master device with no external components. Writing of slave devices must be delayed until after the \overline{BUSY} input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation. When presented a HIGH input, the M/\overline{S} pin allows the device to be used as a master and therefore the \overline{BUSY} line is an output. \overline{BUSY} can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C006/016 provides eight semaphore latches which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a 0 to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, \overline{SEM} or \overline{OE} must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a 0), it assumes control over the shared resource, otherwise (reads a 1) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a 1), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a 1 is written to cancel its request.



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C006-15AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006-15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C006-25AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006-25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006-25AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006-25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C006-35AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006-35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006-35AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006-35JI	J81	68-Lead Plastic Leaded Chip Carrier	
55	CY7C006-55AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006-55JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006-55AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006-55JI	J81	68-Lead Plastic Leaded Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C016-15AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016-15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C016-25AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016-25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C016-25AI	A80	80-Lead Thin Quad Flat Package	Industrial
	CY7C016-25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C016-35AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016-35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C016-35AI	A80	80-Lead Thin Quad Flat Package	Industrial
	CY7C016-35JI	J81	68-Lead Plastic Leaded Chip Carrier	
55	CY7C016-55AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016-55JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C016-55AI	A80	80-Lead Thin Quad Flat Package	Industrial
	CY7C016-55JI	J81	68-Lead Plastic Leaded Chip Carrier	



4K x 16/18 and 8K x 16/18 Dual-Port Static RAM with Sem, Int, Busy

Features

- 4K x 16 organization (CY7C024)
- 4K x 18 organization (CY7C0241)
- 8K x 16 organization (CY7C025)
- 8K x 18 organization (CY7C0251)
- High-speed access
— 15 ns
- Automatic power-down
- Low operating power
— $I_{CC} = 150 \text{ mA (typ.)}$
- Expandable data bus to 32/36 bits or more using Master/Slave chip select when using more than one device
- On chip arbitration logic
- Semaphores included to permit software handshaking between ports
- INT flag for port-to-port communication
- Separate upper byte and lower byte control
- Pin select for Master or Slave
- Available in 84-pin PLCC and 100-pin TQFP

- Pin-compatible and functional equivalent to IDT7024/IDT7025

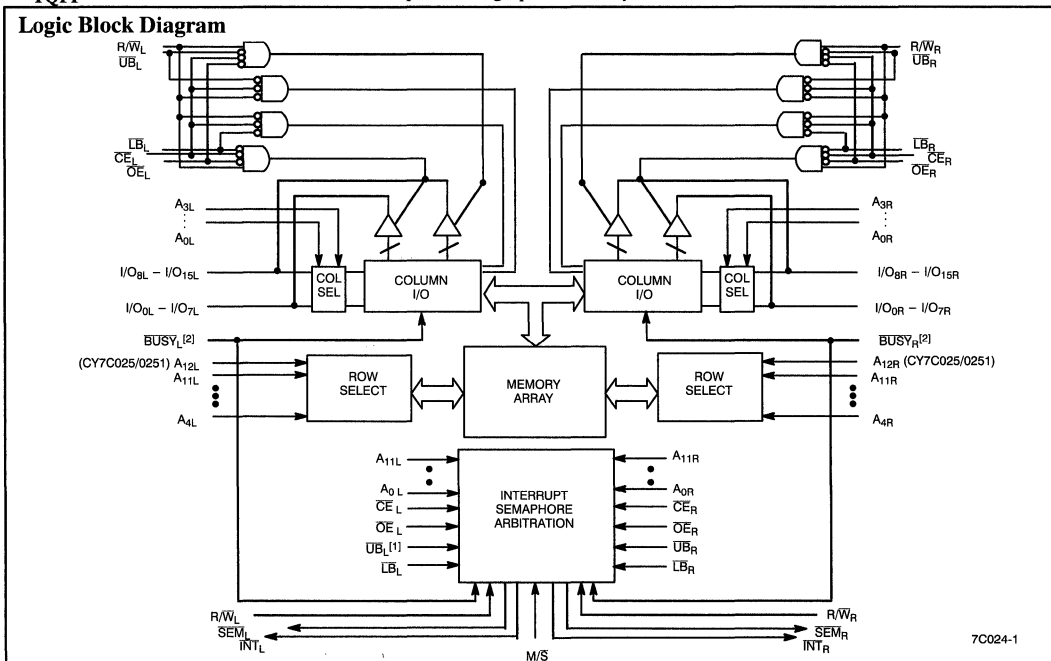
Functional Description

The CY7C024/0241 and CY7C025/0251 are low-power CMOS 4K x 16/18 and 8K x 16/18 dual-port static RAMs. Various arbitration schemes are included on the CY7C024/0241 and CY7C025/0251 to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7C024/0241 and CY7C025/0251 can be utilized as standalone 16-/18-bit dual-port static RAMs or multiple devices can be combined in order to function as a 32-/36-bit or wider master/slave dual-port static RAM. An M/S pin is provided for implementing 32-/36-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering and dual-port video/graphics memory.

Each port has independent control pins: chip enable (CE), read or write enable (R/W), and output enable (OE). Two flags are provided on each port (BUSY and INT). BUSY signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag (INT) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip select (CE) pin.

The CY7C024/0241 and CY7C025/0251 are available in 84-pin PLCCs (CY7C024 and CY7C025 only) and 100-pin Thin Quad Plastic Flatpack (TQFP).

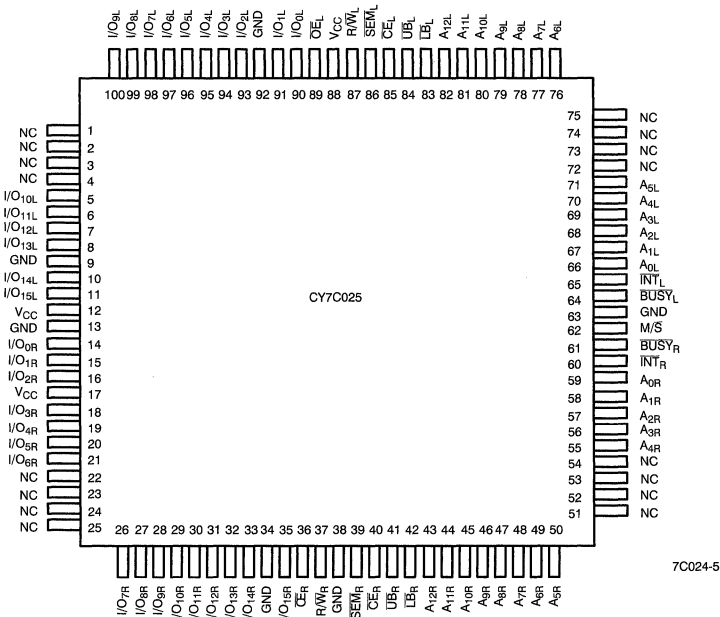
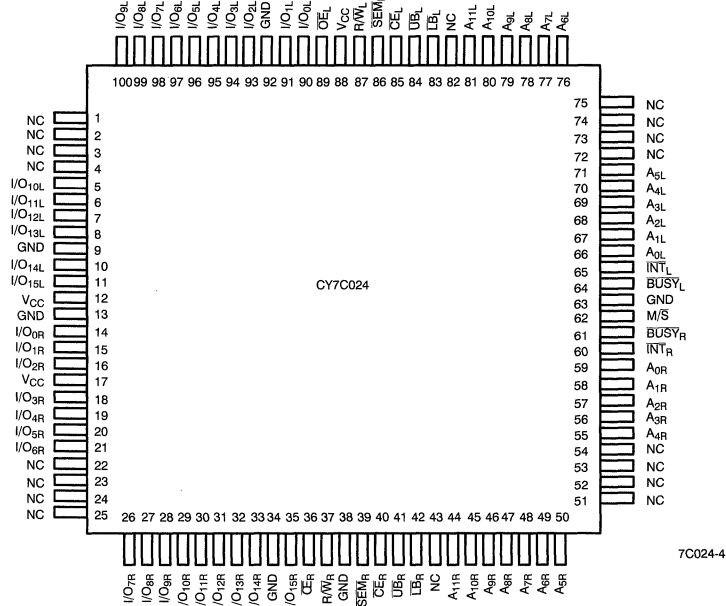
Logic Block Diagram



Notes:

1. LB=Lower Byte. UB=Upper Byte.

2. BUSY is an output in master mode and an input in slave mode.

Pin Configurations (continued)
**100-Pin TQFP
Top View**




Pin Definitions

Left Port	Right Port	Description
CE _L	CE _R	Chip Enable
R/W _L	R/W _R	Read/Write Enable
OE _L	OE _R	Output Enable
A _{0L} -A _{12L}	A _{0R} -A _{12R}	Address
I/O _{0L} -I/O _{15L}	I/O _{0R} -I/O _{15R}	Data Bus Input/Output
SEM _L	SEM _R	Semaphore Enable
UB _L	UB _R	Upper Byte Select
LB _L	LB _R	Lower Byte Select
INT _L	INT _R	Interrupt Flag
BUSY _L	BUSY _R	Busy Flag
M/S		Master or Slave Select
V _{CC}		Power
GND		Ground

Selection Guide

	7C024/0241-15 7C025/0251-15	7C024/0241-25 7C025/0251-25	7C024/0241-35 7C025/0251-35	7C024/0241-55 7C025/0251-55
Maximum Access Time (ns)	15	25	35	55
Maximum Operating Current (mA)	280	250	230	220
Maximum Standby Current for I _{SB1} (mA)	70	60	50	40

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature -65°C to + 150°C
- Ambient Temperature with Power Applied -55°C to + 125°C
- Supply Voltage to Ground Potential -0.3V to + 7.0V
- DC Voltage Applied to Outputs in High Z State -0.5V to + 7.0V
- DC Input Voltage³⁾ -0.5V to + 7.0V
- Output Current into Outputs (LOW) 20 mA

- Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current >200 mA

Operating Range

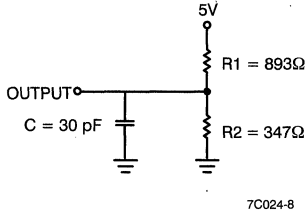
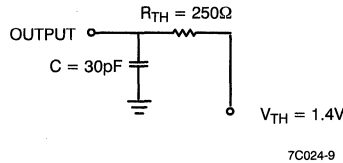
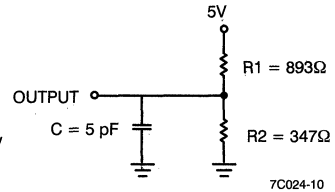
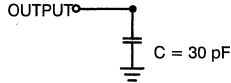
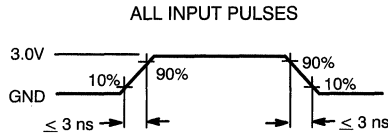
Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

Note:

- 3. Pulse width < 20 ns.

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$,	10	pF
C_{OUT}	Output Capacitance	$V_{CC} = 5.0\text{V}$	10	pF

AC Test Loads and Waveforms

(a) Normal Load (Load 1)

(b) Thévenin Equivalent (Load 1)

(c) Three-State Delay (Load 3)

Load (Load 2)

Switching Characteristics Over the Operating Range^[6]

Parameter	Description	7C024/0241-15 7C025/0251-15		7C024/0241-25 7C025/0251-25		7C024/0241-35 7C025/0251-35		7C024/0241-55 7C025/0251-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15		25		35		55		ns
t_{AA}	Address to Data Valid		15		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		ns
$t_{ACE}^{[7]}$	\overline{CE} LOW to Data Valid		15		25		35		55	ns
t_{DOE}	\overline{OE} LOW to Data Valid		10		13		20		25	ns
$t_{LZOE}^{[8,9]}$	\overline{OE} Low to Low Z	3		3		3		3		ns
$t_{HZOE}^{[8,9]}$	\overline{OE} HIGH to High Z		10		15		20		25	ns
$t_{LZCE}^{[8,9]}$	\overline{CE} LOW to Low Z	3		3		3		3		ns
$t_{HZCE}^{[8,9]}$	\overline{CE} HIGH to High Z		10		15		20		25	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		15		25		25		25	ns
$t_{ABE}^{[7]}$	Byte Enable Access Time		15		25		35		55	ns

Notes:

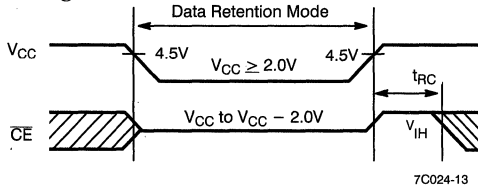
- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OI}/I_{OH} and 30-pF load capacitance.
- To access RAM, $\overline{CE}=L$, $\overline{UB}=L$, $\overline{SEM}=H$. To access semaphore, $\overline{CE}=H$ and $\overline{SEM}=L$. Either condition must be valid for the entire t_{SCE} time.
- At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE} .
- Test conditions used are Load 3.

Data Retention Mode

The CY7C024/0241 is designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip enable (\overline{CE}) must be held HIGH during data retention, within V_{CC} to $V_{CC} - 0.2V$.

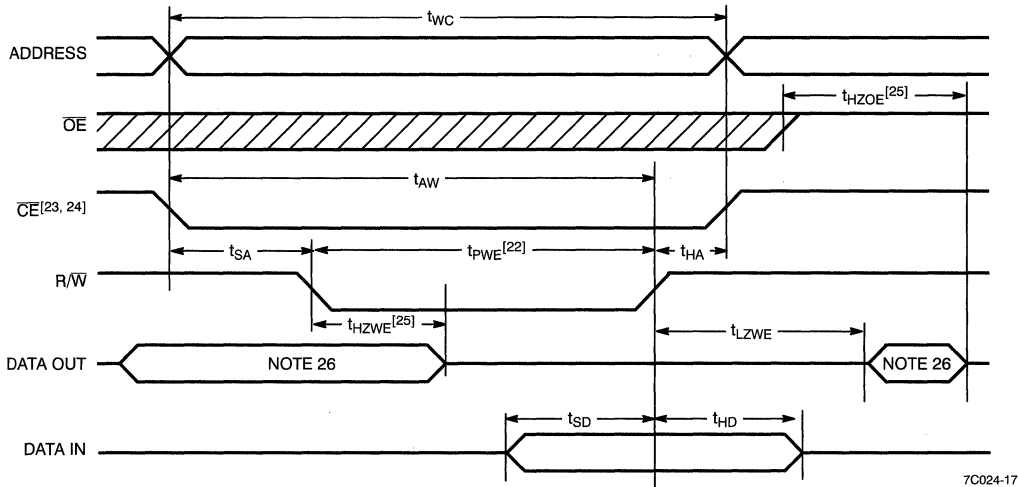
2. \overline{CE} must be kept between $V_{CC} - 0.2V$ and 70% of V_{CC} during the power-up and power-down transitions.
3. The RAM can begin operation $>t_{RC}$ after V_{CC} reaches the minimum operating voltage (4.5 volts).

Timing


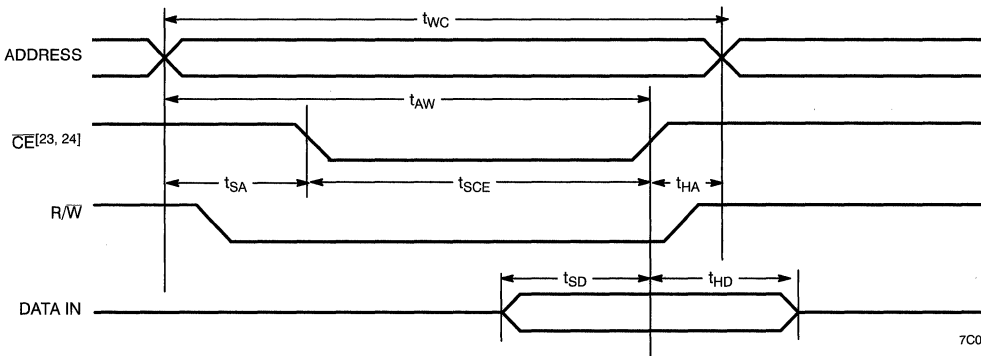
Parameter	Test Conditions ^[13]	Max.	Unit
ICC_{DR1}	@ $V_{CC_{DR}} = 2V$	1.5	mA

Note:

13. $\overline{CE} = V_{CC}$, $V_{IH} = GND$ to V_{CC} , $T_A = 25^\circ C$. This parameter is guaranteed but not tested.

Switching Waveforms (continued)
Write Cycle No. 1: R/W Controlled Timing^[19, 20, 21, 22]


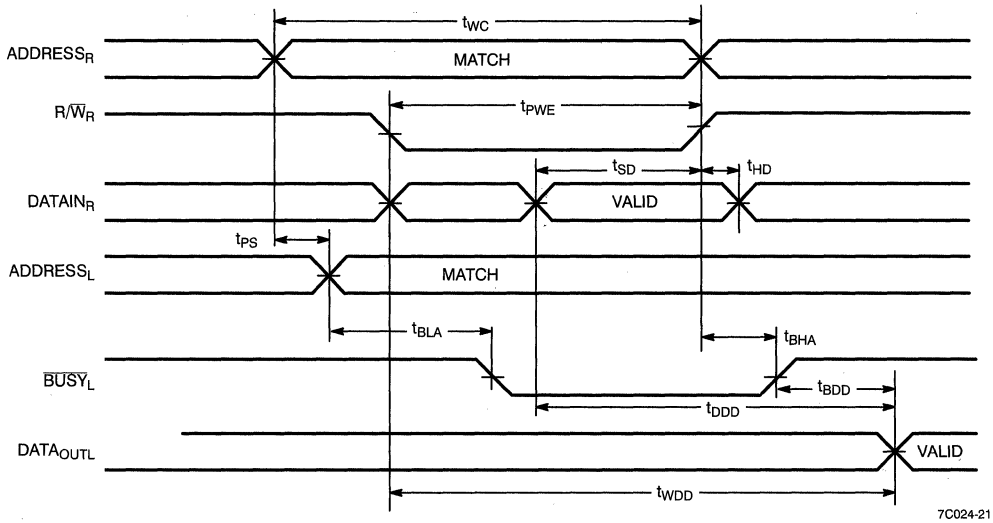
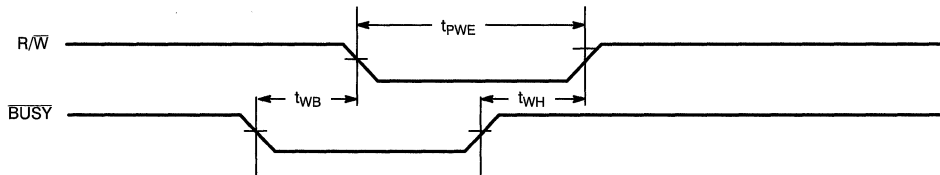
7C024-17

Write Cycle No. 2: CE Controlled Timing^[19, 20, 21, 27]


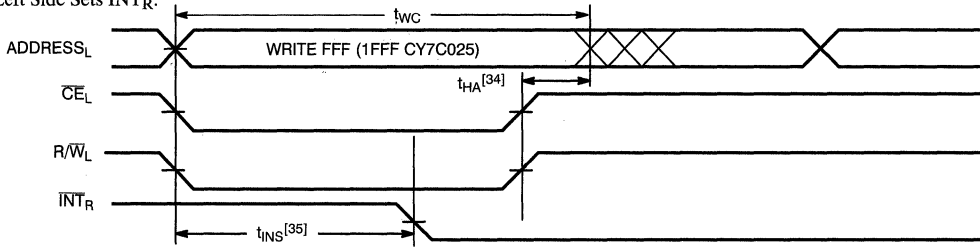
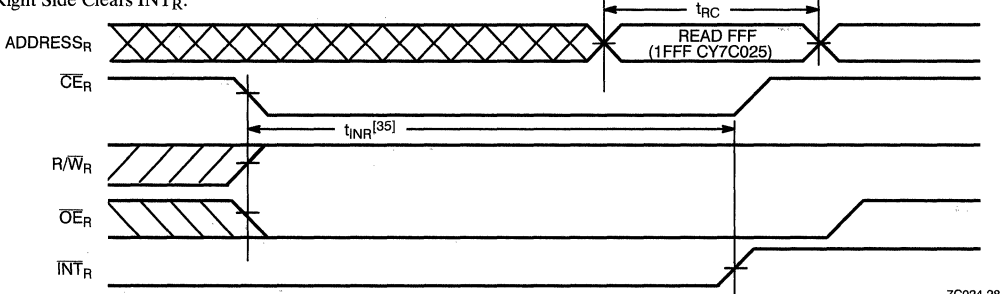
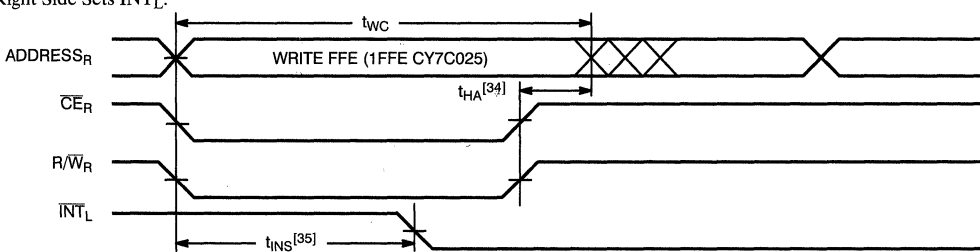
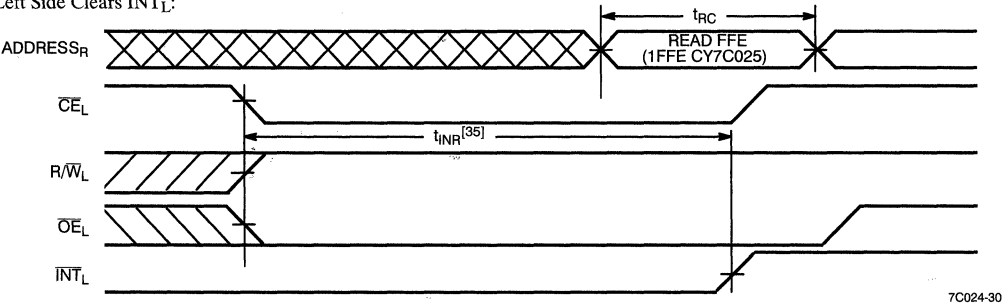
7C024-18

Notes:

19. R/W must be HIGH during all address transitions.
20. A write occurs during the overlap (t_{SCE} or t_{PWE}) of a LOW \overline{CE} or \overline{SEM} and a LOW \overline{UB} or \overline{LB} .
21. t_{HA} is measured from the earlier of \overline{CE} or R/W or (\overline{SEM} or R/W) going HIGH at the end of write cycle.
22. If \overline{OE} is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{PWE} or ($t_{HZWE} + t_{SD}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD} . If \overline{OE} is HIGH during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{PWE} .
23. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$.
24. To access upper byte, $\overline{CE} = V_{IL}$, $\overline{UB} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access lower byte, $\overline{CE} = V_{IL}$, $\overline{LB} = V_{IL}$, $\overline{SEM} = V_{IH}$.
25. Transition is measured ± 500 mV from steady state with a 5-pF load (including scope and jig). This parameter is sampled and not 100% tested.
26. During this period, the I/O pins are in the output state, and input signals must not be applied.
27. If the \overline{CE} or \overline{SEM} LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the high-impedance state.

Switching Waveforms (continued)
Timing Diagram of Read with $\overline{\text{BUSY}}$ ($\text{M}/\overline{\text{S}}=\text{HIGH}$)^[32]

Write Timing with Busy Input ($\text{M}/\overline{\text{S}}=\text{LOW}$)


Note:
 32. $\overline{\text{CE}}_L = \overline{\text{CE}}_R = \text{LOW}$.

Switching Waveforms (continued)
Interrupt Timing Diagrams
Left Side Sets \overline{INT}_R :

Right Side Clears \overline{INT}_R :

Right Side Sets \overline{INT}_L :

Left Side Clears \overline{INT}_L :

Notes:

34. t_{HA} depends on which enable pin (\overline{CE}_L or R/\overline{W}_L) is deasserted first. 35. t_{INS} or t_{INR} depends on which enable pin (\overline{CE}_L or R/\overline{W}_L) is asserted last.

Table 1. Non-Contending Read/Write



Inputs						Outputs		Operation
CE	R/W	OE	UB	LB	SEM	I/O ₈ -I/O ₁₅	I/O ₀ -I/O ₇	
H	X	X	X	X	H	High Z	High Z	Deselected: Power-Down
X	X	X	H	H	H	High Z	High Z	Deselected: Power-Down
L	L	X	L	H	H	Data In	High Z	Write to Upper Byte Only
L	L	X	H	L	H	High Z	Data In	Write to Lower Byte Only
L	L	X	L	L	H	Data In	Data In	Write to Both Bytes
L	H	L	L	H	H	Data Out	High Z	Read Upper Byte Only
L	H	L	H	L	H	High Z	Data Out	Read Lower Byte Only
L	H	L	L	L	H	Data Out	Data Out	Read Both Bytes
X	X	H	X	X	X	High Z	High Z	Outputs Disabled
H	H	L	X	X	L	Data Out	Data Out	Read Data in Semaphore Flag
X	H	L	H	H	L	Data Out	Data Out	Read Data in Semaphore Flag
H		X	X	X	L	Data In	Data In	Write D _{IN0} into Semaphore Flag
X		X	H	H	L	Data In	Data In	Write D _{IN0} into Semaphore Flag
L	X	X	L	X	L			Not Allowed
L	X	X	X	L	L			Not Allowed

Table 2. Interrupt Operation Example (assumes $\overline{\text{BUSY}}_L = \overline{\text{BUSY}}_R = \text{HIGH}$)^[36]

Function	Left Port					Right Port				
	R/W _L	CE _L	OE _L	A _{0L-11L}	INT _L	R/W _R	CE _R	OE _R	A _{0R-11R}	INT _R
Set Right INT _R Flag	L	L	X	(1)FFF	X	X	X	X	X	L ^[38]
Reset Right INT _R Flag	X	X	X	X	X	X	L	L	(1)FFF	H ^[37]
Set Left INT _L Flag	X	X	X	X	L ^[37]	L	L	X	(1)FFE	X
Reset Left INT _L Flag	X	L	L	(1)FFE	H ^[38]	X	X	X	X	X

Table 3. Semaphore Operation Example

Function	D ₀ -D ₁₅ Left	D ₀ -D ₁₅ Right	Status
No action	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left Port has semaphore token
Right port writes 0 to semaphore	0	1	No change. Right side has no write access to semaphore.
Left port writes 1 to semaphore	1	0	Right port obtains semaphore token
Left port writes 0 to semaphore	1	0	No change. Left port has no write access to semaphore
Right port writes 1 to semaphore	0	1	Left port obtains semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free
Right port writes 0 to semaphore	1	0	Right port has semaphore token
Right port writes 1 to semaphore	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free

Notes:

36. A_{0L-12L} and A_{0R-12R}, 1FFF/1FFE for the CY7C025.

37. If $\overline{\text{BUSY}}_R = L$, then no change.

38. If $\overline{\text{BUSY}}_L = L$, then no change.

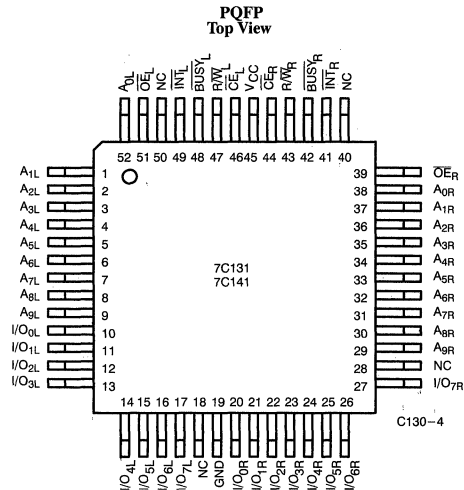
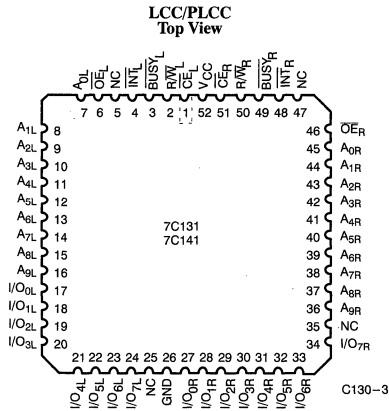


Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C0241-15AC	A100	100-Pin Thin Quad Flat Pack	Commercial
25	CY7C0241-25AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0241-25AI	A100	100-Pin Thin Quad Flat Pack	Industrial
35	CY7C0241-35AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0241-35AI	A100	100-Pin Thin Quad Flat Pack	Industrial
55	CY7C0241-55AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0241-55AI	A100	100-Pin Thin Quad Flat Pack	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C0251-15AC	A100	100-Pin Thin Quad Flat Pack	Commercial
25	CY7C0251-25AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0251-25AI	A100	100-Pin Thin Quad Flat Pack	Industrial
35	CY7C0251-35AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0251-35AI	A100	100-Pin Thin Quad Flat Pack	Industrial
55	CY7C0251-55AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0251-55AI	A100	100-Pin Thin Quad Flat Pack	Industrial

Document #: 38-00255-A

Pin Configurations (continued)

Selection Guide

		7C130-25 ^[3] 7C131-25 7C140-25 7C141-25	7C130-30 7C131-30 7C140-30 7C141-30	7C130-35 7C131-35 7C140-35 7C141-35	7C130-45 7C131-45 7C140-45 7C141-45	7C130-55 7C131-55 7C140-55 7C141-55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Com'l/Ind	170	170	120	90	90
	Military			170	120	120
Maximum Standby Current (mA)	Com'l/Ind	65	65	45	35	35
	Military			65	45	45

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied -55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State -0.5V to +7.0V

DC Input Voltage -3.5V to +7.0V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

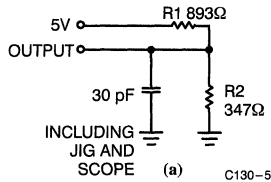
Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Military ^[4]	-55°C to +125°C	5V ± 10%

Notes:

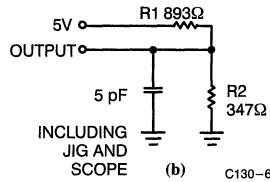
3. 25-ns version available only in PLCC/POFP packages.

4. T_A is the "instant on" case temperature

AC Test Loads and Waveforms

 INCLUDING
 JIG AND
 SCOPE

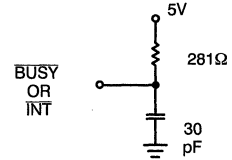
(a)

C130-5


 INCLUDING
 JIG AND
 SCOPE

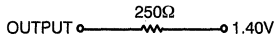
(b)

C130-6

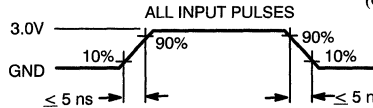

BUSY Output Load
 (CY7C130/CY7C131 ONLY)

C130-7

Equivalent to: THÉVENIN EQUIVALENT



C130-8



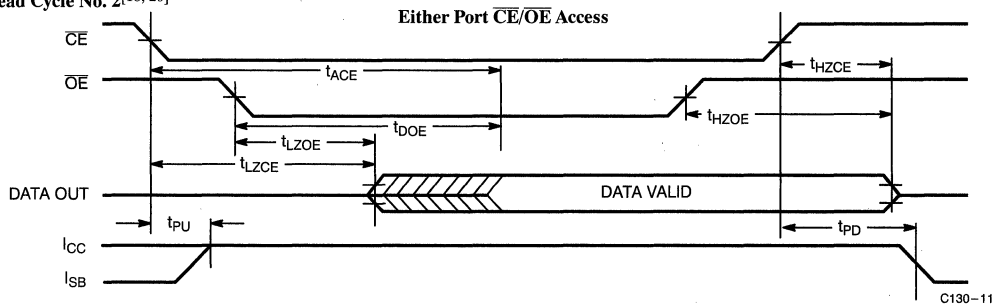
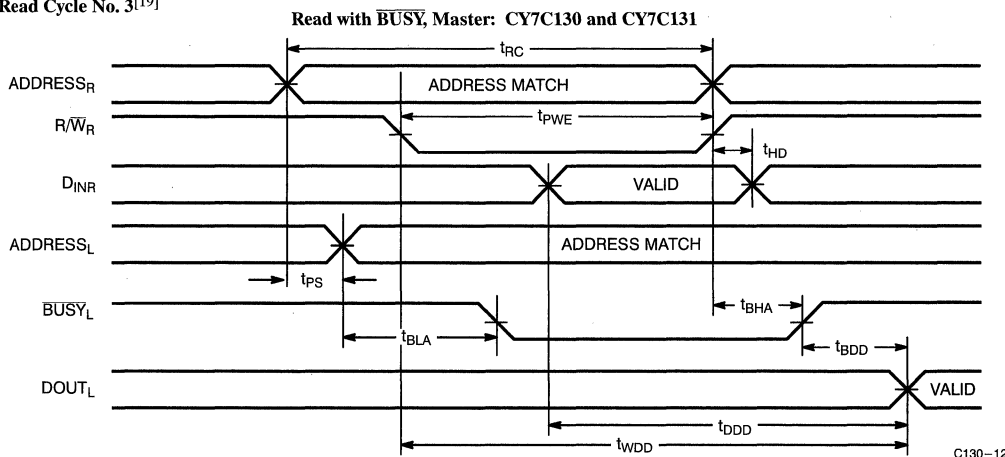
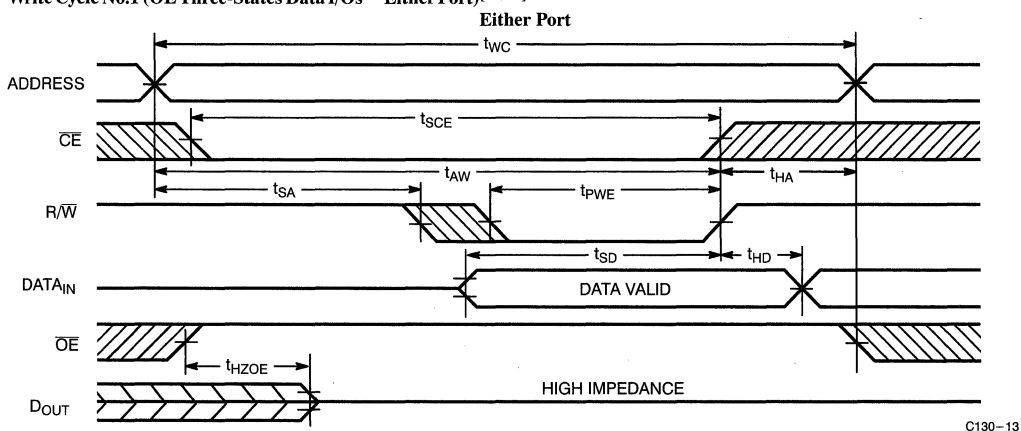
C130-9

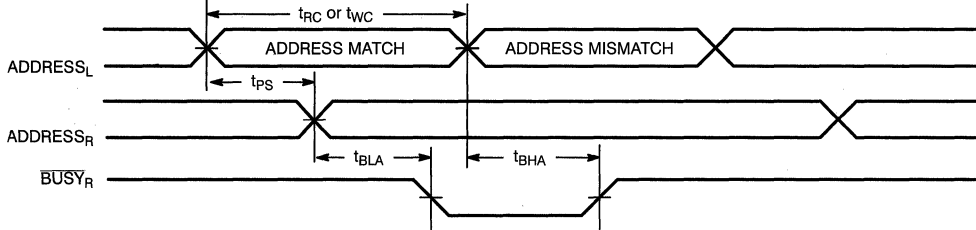
Switching Characteristics Over the Operating Range^[5, 10]

Parameter	Description	7C130-25 ^[3]		7C130-30		7C130-35		7C130-45		7C130-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	25		30		35		45		55		ns
t _{AA}	Address to Data Valid ^[11]		25		30		35		45		55	ns
t _{OHA}	Data Hold from Address Change	0		0		0		0		0		ns
t _{ACE}	\overline{CE} LOW to Data Valid ^[11]		25		30		35		45		55	ns
t _{DOE}	\overline{OE} LOW to Data Valid ^[11]		15		20		20		25		25	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[12, 13]	3		3		3		3		3		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[12, 13]		15		15		20		20		25	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[12, 13]	5		5		5		5		5		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[12, 13]		15		15		20		20		25	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		25		25		35		35		35	ns
WRITE CYCLE^[14]												
t _{WC}	Write Cycle Time	25		30		35		45		55		ns
t _{SCE}	\overline{CE} LOW to Write End	20		25		30		35		40		ns
t _{AW}	Address Set-Up to Write End	20		25		30		35		40		ns
t _{HA}	Address Hold from Write End	2		2		2		2		2		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t _{PWE}	R/ \overline{W} Pulse Width	15		25		25		30		30		ns
t _{SD}	Data Set-Up to Write End	15		15		15		20		20		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{HZWE}	R/ \overline{W} LOW to High Z ^[13]		15		15		20		20		25	ns
t _{LZWE}	R/ \overline{W} HIGH to Low Z ^[13]	0		0		0		0		0		ns

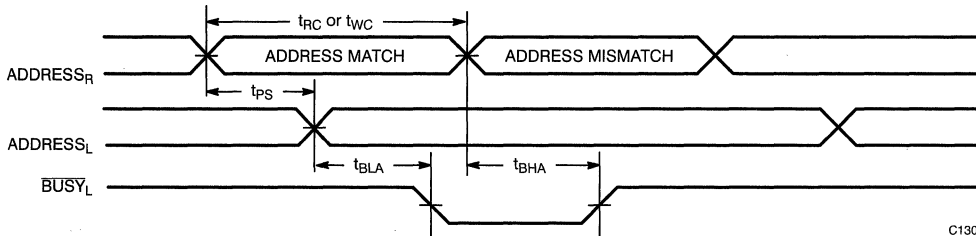
Notes:

10. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
11. AC Test Conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
12. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
13. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
14. The internal write time of the memory is defined by the overlap of \overline{CS} LOW and R/ \overline{W} LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

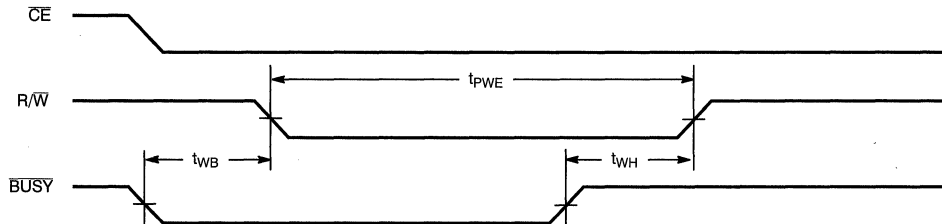
Switching Waveforms (continued)
Read Cycle No. 2^[18, 20]

Read Cycle No. 3^[19]

Write Cycle No. 1 (\overline{OE} Three-States Data I/Os - Either Port)^[14, 21]


Switching Waveforms (continued)
Busy Timing Diagram No. 2 (Address Arbitration)
Left Address Valid First:


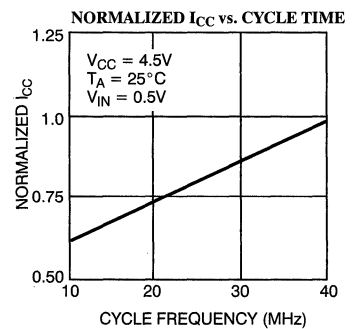
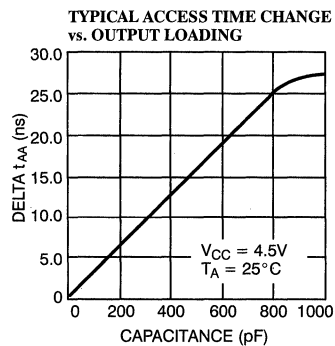
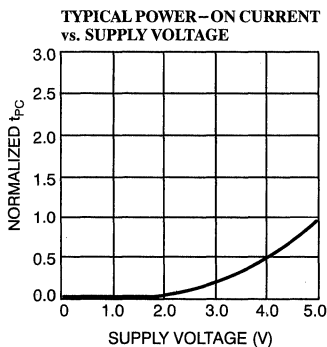
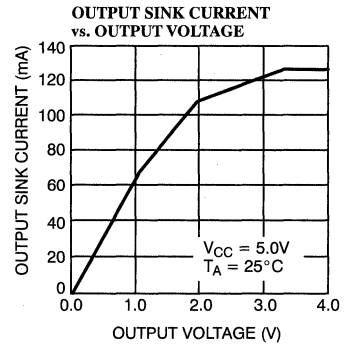
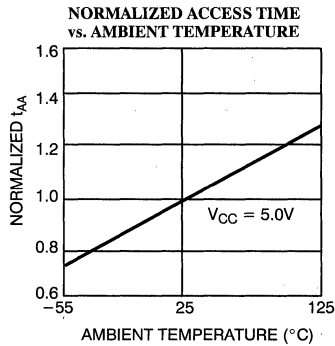
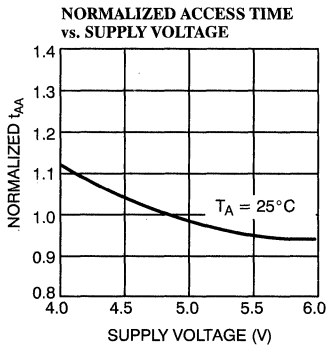
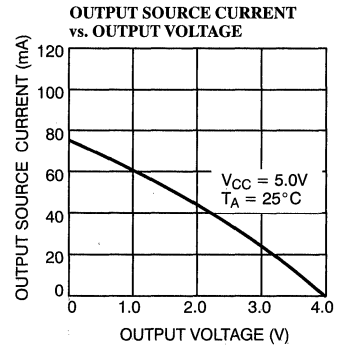
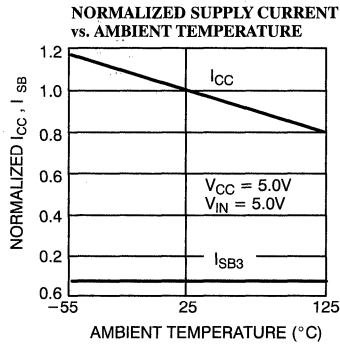
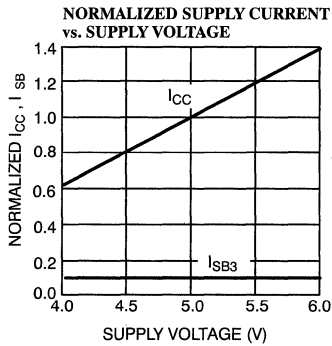
C130-17

Right Address Valid First:


C130-18

Busy Timing Diagram No. 3
Write with $\overline{\text{BUSY}}$ (Slave: CY7C140/CY7C141)


C130-19

Typical DC and AC Characteristics




Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C140-30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C140-35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140-35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
45	CY7C140-45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140-45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
55	CY7C140-55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140-55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C141-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-25NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-25NI	N52	52-Pin Plastic Quad Flatpack	
30	CY7C141-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C141-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-35NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C141-45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-45NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C141-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-55NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-55LMB	L69	52-Square Leadless Chip Carrier	Military

2K x 8 Dual-Port Static RAM

Features

- 0.8-micron CMOS for optimum speed/power
- Automatic power-down
- TTL compatible
- Capable of withstanding greater than 2001V electrostatic discharge
- Fully asynchronous operation
- Master CY7C132/CY7C136 easily expands data bus width to 16 or more bits using slave CY7C142/CY7C146
- **BUSY output flag on CY7C132/CY7C136; BUSY input on CY7C142/CY7C146**
- **INT flag for port-to-port communication (52-pin LCC/PLCC/PQFP versions)**

Functional Description

The CY7C132/CY7C136/CY7C142 and CY7C146 are high-speed CMOS 2K by 8 dual-port static RAMs. Two ports are provided to permit independent access to any location in memory. The CY7C132/CY7C136 can be utilized as either a stand-alone 8-bit dual-port static RAM or as a MASTER dual-port RAM in conjunction with the CY7C142/CY7C146 SLAVE dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice, or multiprocessor designs.

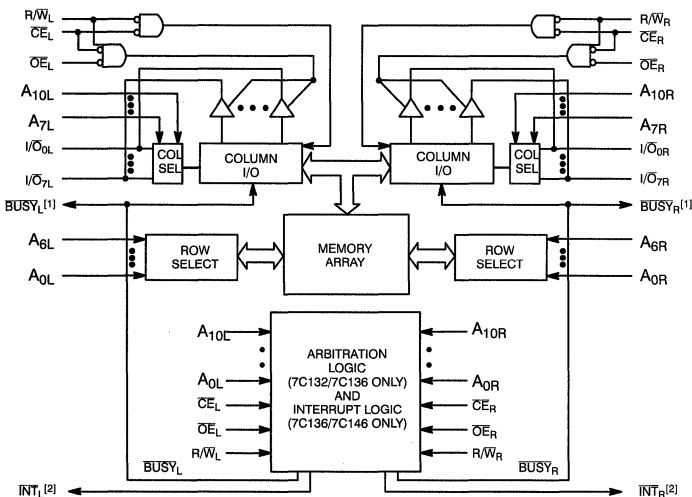
Each port has independent control pins; chip enable (CE), write enable (R/W), and

output enable (\overline{OE}). \overline{BUSY} flags are provided on each port. In addition, an interrupt flag (INT) is provided on each port of the 52-pin LCC and PLCC versions. \overline{BUSY} signals that the port is trying to access the same location currently being accessed by the other port. On the LCC/PLCC versions, INT is an interrupt flag indicating that data has been placed in a unique location (7FF for the left port and 7FE for the right port).

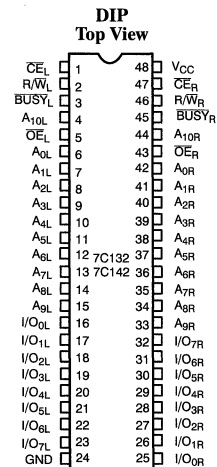
An automatic power-down feature is controlled independently on each port by the chip enable (CE) pins.

The CY7C132/CY7C142 are available in both 48-pin DIP and 48-pin LCC. The CY7C136/CY7C146 are available in 52-pin LCC, PLCC, and PQFP.

Logic Block Diagram



Pin Configuration



C132-1

C132-2

Notes:

1. CY7C132/CY7C136 (Master): \overline{BUSY} is open drain output and requires pull-up resistor.
CY7C142/CY7C146 (Slave): \overline{BUSY} is input.
2. Open drain outputs; pull-up resistor required.

Electrical Characteristics Over the Operating Range^[5]

Parameter	Description	Test Conditions	7C132-25, 30 ^[3] 7C136-25, 30 7C142-25, 30 7C146-25, 30		7C132-35 7C136-35 7C142-35 7C146-35		7C132-45, 55 7C136-45, 55 7C142-45, 55 7C146-45, 55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 4.0 mA		0.4		0.4		0.4	V
		I _{OL} = 16.0 mA ^[6]		0.5		0.5		0.5	
V _{IH}	Input HIGH Voltage		2.2		2.2		2.2		V
V _{IL}	Input LOW Voltage			0.8		0.8		0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	-5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} = Max., V _{OUT} = GND		-350		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	$\overline{CE} = V_{IL}$, Outputs Open, f = f _{MAX} ^[8]	Com'1	170		120		90	mA
			Mil			170		120	
I _{SB1}	Standby Current Both Ports, TTL Inputs	\overline{CE}_L and $\overline{CE}_R \geq V_{IH}$, f = f _{MAX} ^[8]	Com'1	65		45		35	mA
			Mil			65		45	
I _{SB2}	Standby Current One Port, TTL Inputs	\overline{CE}_L or $\overline{CE}_R \geq V_{IH}$, Active Port Outputs Open, f = f _{MAX} ^[8]	Com'1	115		90		75	mA
			Mil			115		90	
I _{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0	Com'1	15		15		15	mA
			Mil			15		15	
I _{SB4}	Standby Current One Port, CMOS Inputs	One Port \overline{CE}_L or $\overline{CE}_R \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, Active Port Outputs Open, f = f _{MAX} ^[8]	Com'1	105		85		70	mA
			Mil			105		85	

Capacitance^[9]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	15	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

- See the last page of this specification for Group A subgroup testing information.
- BUSY and INT pins only.
- Duration of the short circuit should not exceed 30 seconds.
- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of 1/t_{rc} and using AC Test Waveforms input levels of GND to 3V.
- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
- AC test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
- At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
- t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE}, and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and R/W LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

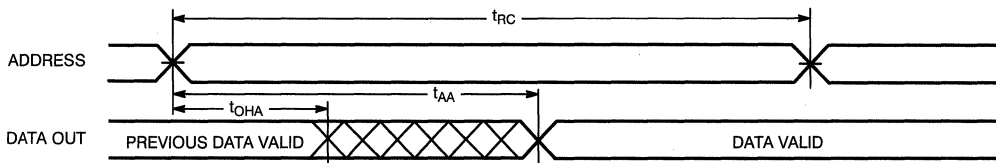
Switching Characteristics Over the Operating Range^[5, 10] (continued)

Parameter	Description	7C132-25 ^[3]		7C132-30		7C132-35		7C132-45		7C132-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING												
t _{BLA}	BUSY LOW from Address Match		20		20		20		25		30	ns
t _{BHA}	BUSY HIGH from Address Mismatch ^[15]		20		20		20		25		30	ns
t _{BLC}	BUSY LOW from CE LOW		20		20		20		25		30	ns
t _{BHC}	BUSY HIGH from CE HIGH ^[15]		20		20		20		25		30	ns
t _{PS}	Port Set Up for Priority	5		5		5		5		5		ns
t _{WBL} ^[16]	R/W LOW after BUSY LOW	0		0		0		0		0		ns
t _{WH}	R/W HIGH after BUSY HIGH	20		30		30		35		35		ns
t _{BDD}	BUSY HIGH to Valid Data		25		30		35		45		45	ns
t _{DDD}	Write Data Valid to Read Data Valid		Note 17		Note 17		Note 17		Note 17		Note 17	ns
t _{WDD}	Write Pulse to Data Delay		Note 17		Note 17		Note 17		Note 17		Note 17	ns
INTERRUPT TIMING^[18]												
t _{WINS}	R/W to INTERRUPT Set Time		25		25		25		35		45	ns
t _{EINS}	CE to INTERRUPT Set Time		25		25		25		35		45	ns
t _{INS}	Address to INTERRUPT Set Time		25		25		25		35		45	ns
t _{OINR}	OE to INTERRUPT Reset Time ^[15]		25		25		25		35		45	ns
t _{EINR}	CE to INTERRUPT Reset Time ^[15]		25		25		25		35		45	ns
t _{INR}	Address to INTERRUPT Reset Time ^[15]		25		25		25		35		45	ns

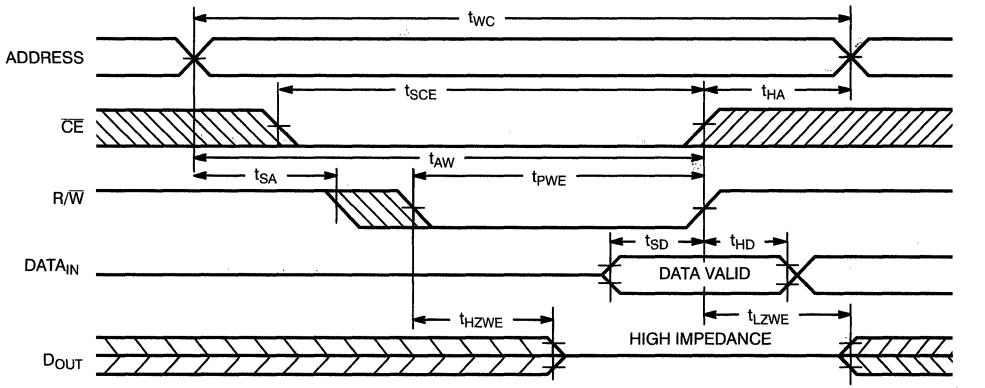
Notes:

15. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
16. CY7C142/CY7C146 only.
17. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
 - A. BUSY on Port B goes HIGH.
 - B. Port B's address toggled.
 - C. CE for Port B is toggled.
 - D. R/W for Port B is toggled during valid read.

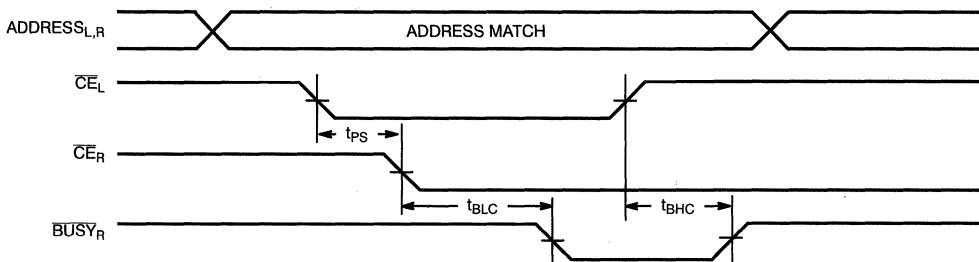
18. 52-pin LCC/PLCC versions only.
19. R/W is HIGH for read cycle.
20. Device is continuously selected, CE = V_{IL} and OE = V_{IL}.
21. Address valid prior to or coincident with CE transition LOW.
22. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{PWE} or t_{HZE} + t_{SD} to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.
23. If the CE LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in a high-impedance state.

Switching Waveforms
Read Cycle No. 1 (Either Port—Address Access)^[19, 20]


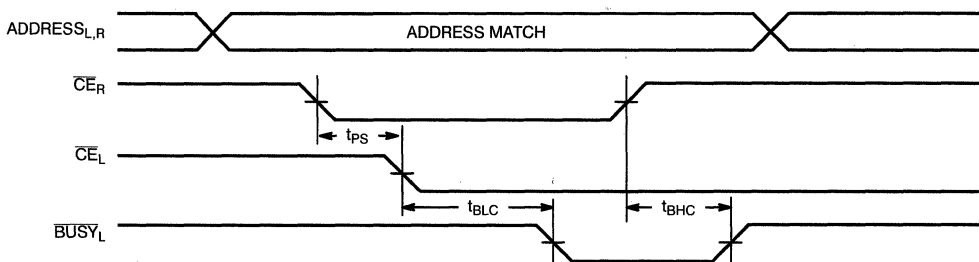
C132-10

Switching Waveforms (continued)
Write Cycle No. 2 (R/W Three-States Data I/Os – Either Port)^[14, 23]


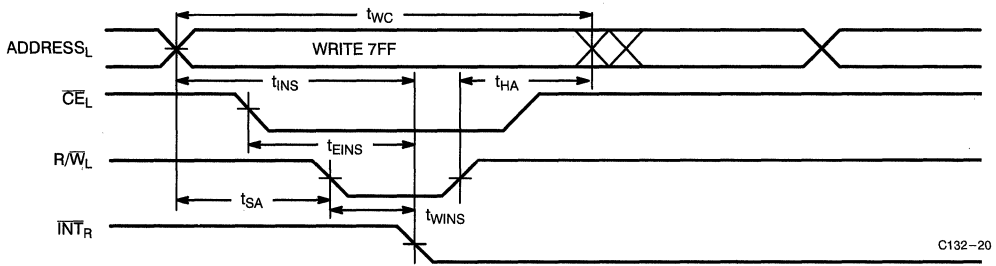
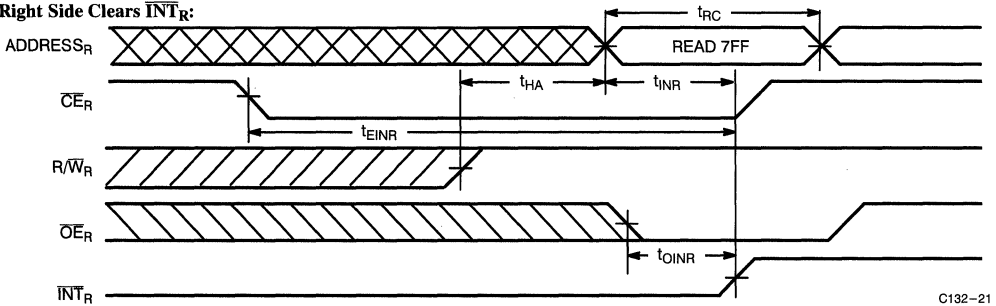
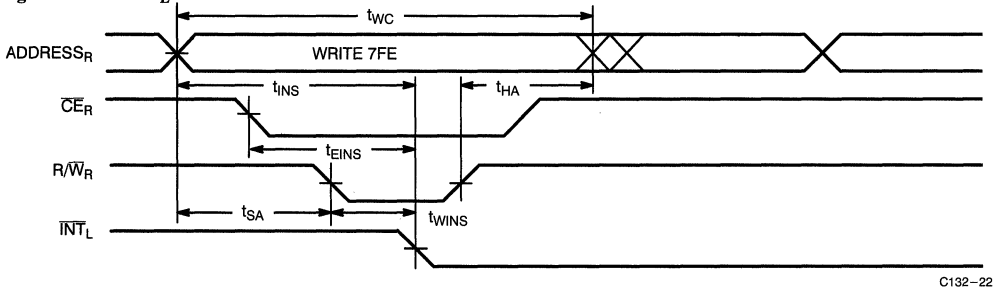
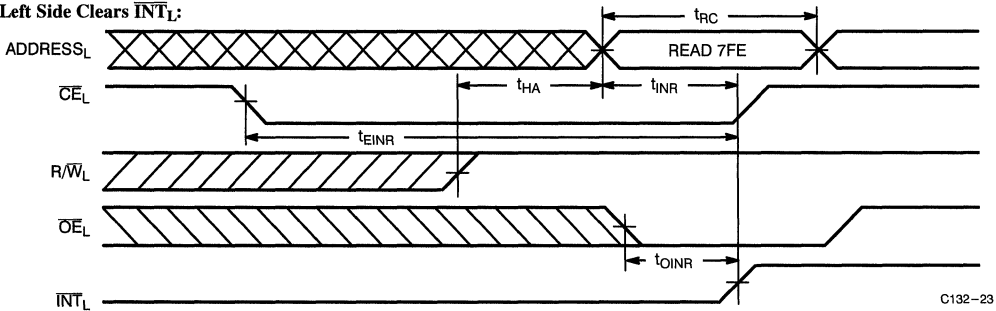
C132-14

Busy Timing Diagram No. 1 (CE Arbitration)
 \overline{CE}_L Valid First:


C132-15

 \overline{CE}_R Valid First:


C132-16

Interrupt Timing Diagrams^[18]
Left Side Sets \overline{INT}_R :

Right Side Clears \overline{INT}_R :

Right Side Sets \overline{INT}_L :

Left Side Clears \overline{INT}_L :




Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C132-30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132-30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C132-35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132-35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132-35DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
45	CY7C132-45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132-45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132-45DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
55	CY7C132-55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132-55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132-55DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C136-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-25NC	N52	52-Pin Plastic Quad Flatpack	
30	CY7C136-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C136-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136-35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C136-45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136-45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136-45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C136-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136-55LMB	L69	52-Square Leadless Chip Carrier	Military



MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{I_X}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3
I _{SB3}	1, 2, 3
I _{SB4}	1, 2, 3

Switching Characteristics

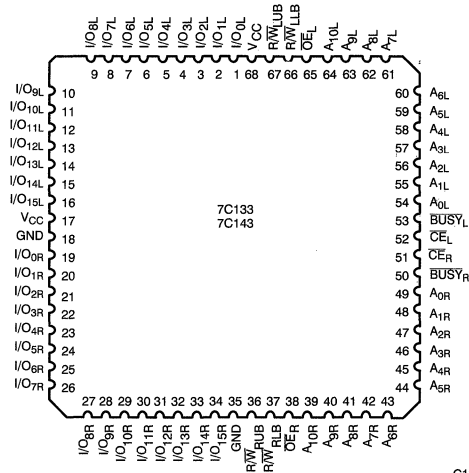
Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t _{BLA}	7, 8, 9, 10, 11
t _{BHA}	7, 8, 9, 10, 11
t _{BLC}	7, 8, 9, 10, 11
t _{BHC}	7, 8, 9, 10, 11
t _{PS}	7, 8, 9, 10, 11
t _{WINS}	7, 8, 9, 10, 11
t _{EINS}	7, 8, 9, 10, 11
t _{INS}	7, 8, 9, 10, 11
t _{OINR}	7, 8, 9, 10, 11
t _{EINR}	7, 8, 9, 10, 11
t _{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t _{WB} ^[24]	7, 8, 9, 10, 11
t _{WH}	7, 8, 9, 10, 11
t _{BDD}	7, 8, 9, 10, 11

Note:

24. CY7C142/CY7C146 only.

Document #: 38-00061-J

Pin Configuration
68-Pin LCC/PLCC
Top View


C133-2

Selection Guide

	7C133-25 7C143-25	7C133-35 7C143-35	7C133-55 7C143-55
Maximum Access Time (ns)	25	35	55
Typical Operating Current I _{CC} (mA)	170	160	150
Typical Standby Current for I _{SB1} (mA)	40	30	20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage to Ground Potential

(Pin 48 to Pin 24) -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State -0.5V to +7.0V

DC Input Voltage -3.5V to +7.0V

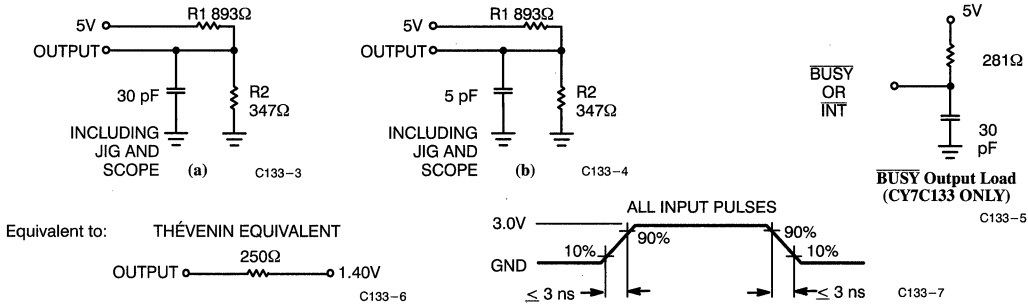
Output Current into Outputs (LOW) 20 mA

 Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

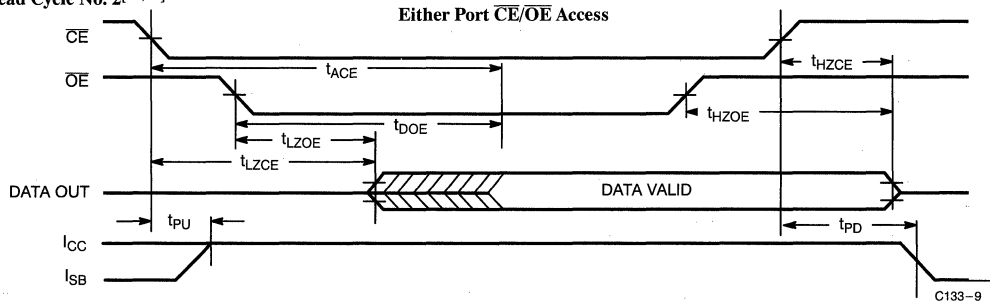
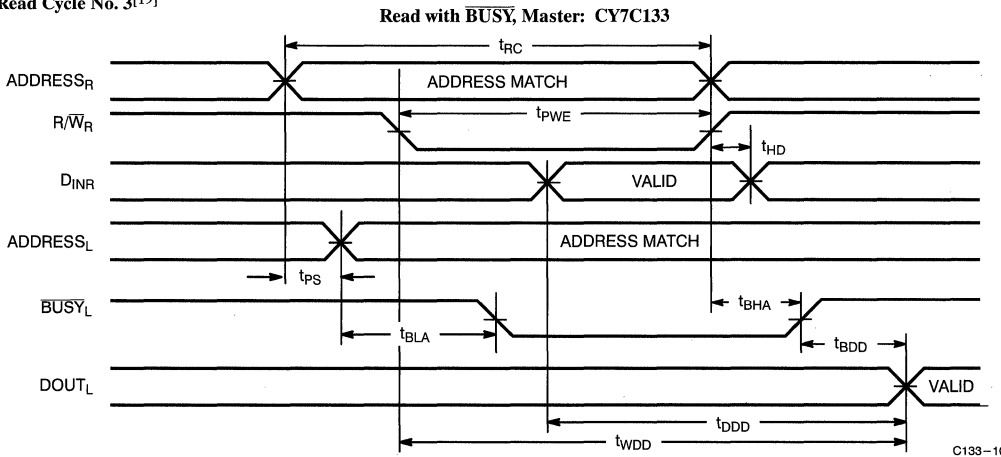
Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

AC Test Loads and Waveforms

Switching Characteristics Over the Operating Range^[7]

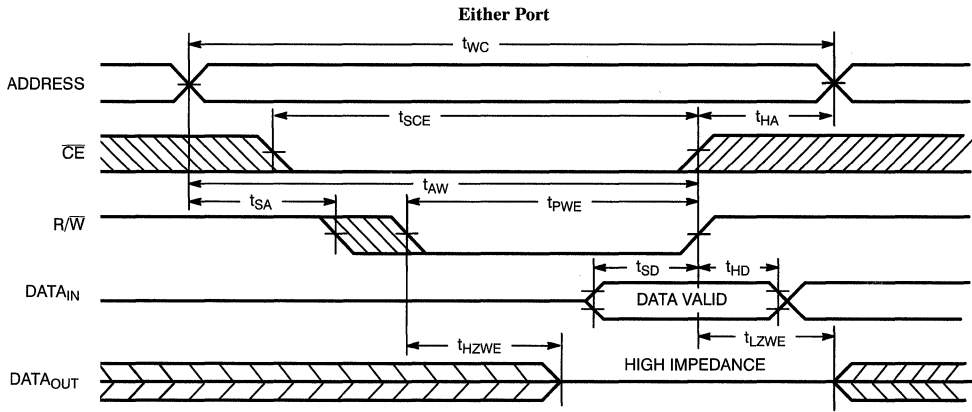
Parameter	Description	7C133-25 7C143-25		7C133-35 7C143-35		7C133-55 7C143-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	25		35		55		ns
t _{AA}	Address to Data Valid ^[8]		25		35		55	ns
t _{OHA}	Data Hold from Address Change	0		0		0		ns
t _{ACE}	\overline{CE} LOW to Data Valid ^[8]		25		35		55	ns
t _{DOE}	\overline{OE} LOW to Data Valid ^[8]		20		25		30	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[9, 10]	3		3		3		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[9, 10]		15		20		25	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[9, 10]	3		5		5		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[9, 10]		15		20		20	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		25		25		25	ns
WRITE CYCLE^[11]								
t _{WC}	Write Cycle Time	25		35		55		ns
t _{SCE}	\overline{CE} LOW to Write End	20		25		40		ns
t _{AW}	Address Set-Up to Write End	20		25		40		ns
t _{HA}	Address Hold from Write End	2		2		2		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	R/ \overline{W} Pulse Width	20		25		35		ns
t _{SD}	Data Set-Up to Write End	15		20		20		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{HZWE}	R/ \overline{W} LOW to High Z ^[10]		15		20		20	ns
t _{LZWE}	R/ \overline{W} HIGH to Low Z ^[10]	0		0		0		ns

Notes:

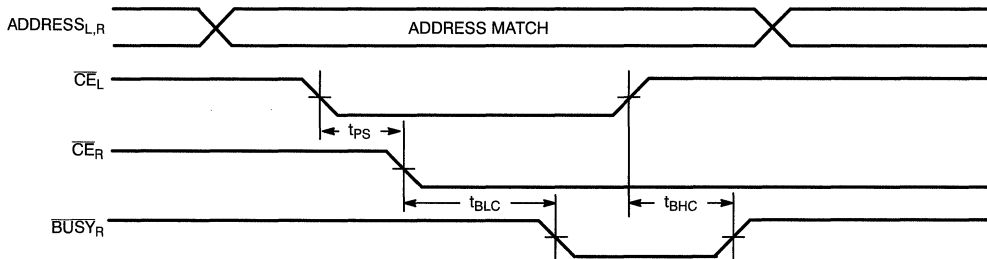
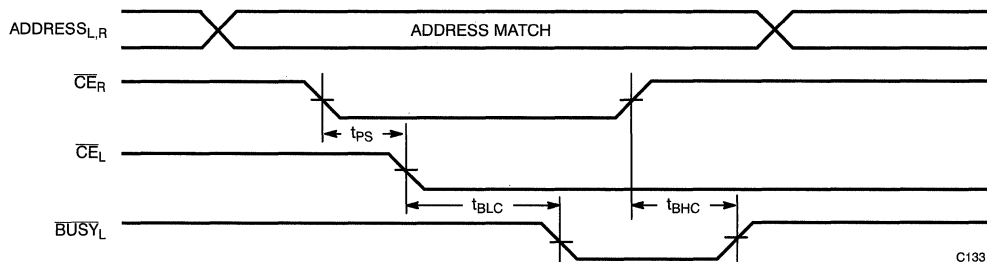
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
- AC Test Conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
- At any given temperature and voltage condition for any given device, t_{LZCE} is less than t_{HZCE} and t_{LZOE} is less than t_{HZOE}.
- t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CS} LOW and R/ \overline{W} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms (continued)
Read Cycle No. 2^[18,20]

Read Cycle No. 3^[19]

Notes:

 20. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)
Write Cycle No. 2 (R/W Three-States Data I/Os – Either Port)^[20,25]


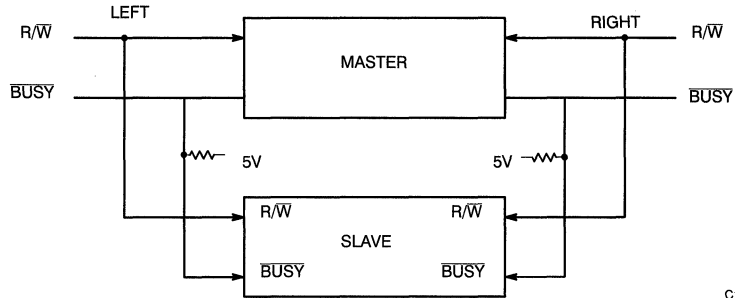
C133-14

Busy Timing Diagram No. 1 (\overline{CE} Arbitration)
 \overline{CE}_L Valid First:

 \overline{CE}_R Valid First:


C133-15

Note:

 25. If the \overline{CE} LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the high-impedance state.

32-Bit Master/Slave Dual-Port Memory Systems


C133-17

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C133-25JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C133-25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C133-35JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C133-35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
55	CY7C133-55JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C133-55JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C143-25JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C143-25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C143-35JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C143-35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
55	CY7C143-55JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C143-55JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial



4K x 8 Dual-Port Static RAMs and 4K x 8 Dual-Port Static RAM with Semaphores

Features

- 0.8-micron BiCMOS for high performance
- High-speed access
 - 15 ns (commercial)
 - 25 ns (military)
- Automatic power-down
- Fully asynchronous operation
- 7B1342 includes semaphores
- 7B134 available in 48-pin DIP
- 7B135/7B1342 available in 52-pin LCC/PLCC

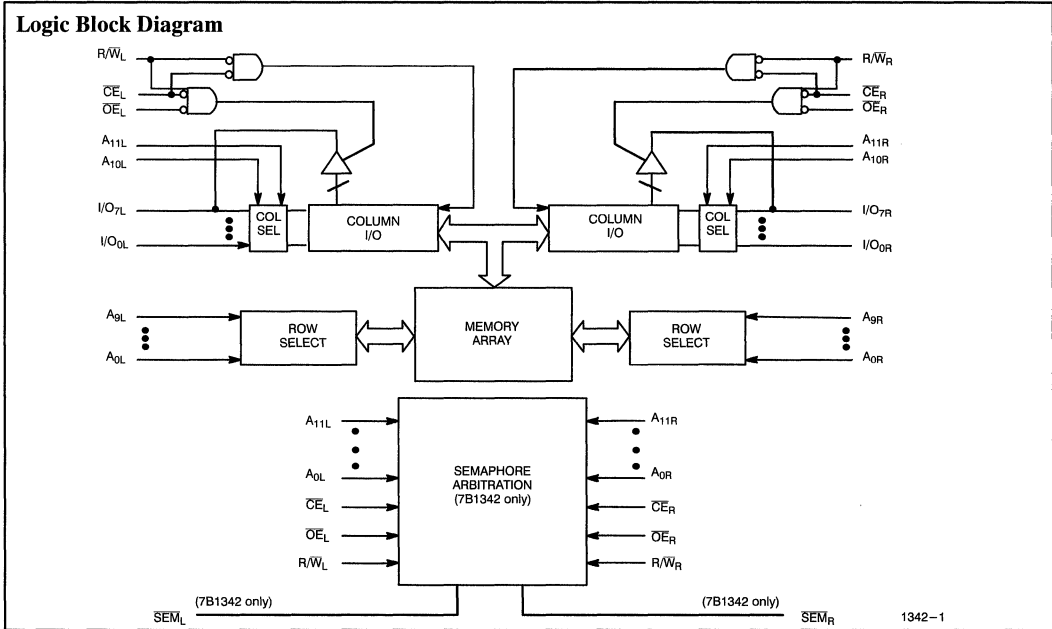
Functional Description

The CY7B134, CY7B135, and CY7B1342 are high-speed BiCMOS 4K x 8 dual-port static RAMs. The CY7B1342 includes semaphores that provide a means to allocate portions of the dual-port RAM or any shared resource. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable (\overline{CE}), read or write enable (R/\overline{W}), and output enable (\overline{OE}). The CY7B134/135 are suited for those systems

that do not require on-chip arbitration or are intolerant of wait states. Therefore, the user must be aware that simultaneous access to a location is possible. Semaphores are offered on the CY7B1342 to assist in arbitrating between ports. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable (\overline{CE}) pin or \overline{SEM} pin (CY7B1342 only).

The CY7B134 is available in 48-pin DIP. The CY7B135 and CY7B1342 are available in 52-pin LCC/PLCC.



Selection Guide

		7B135-15 7B1342-15	7B134-20 7B135-20 7B1342-20	7B134-25 7B135-25 7B1342-25	7B134-35 7B135-35 7B1342-35	7B134-55 7B135-55 7B1342-55
Maximum Access Time (ns)		15	20	25	35	55
Maximum Operating Current (mA)	Commercial	260	240	220	210	210
	Military			260	250	250
Maximum Standby Current (mA)	Commercial	110	100	95	90	90
	Military			100	95	95



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied -55°C to +125°C
 Supply Voltage to Ground Potential (Pin 48 to Pin 24) -0.5V to +7.0V
 DC Voltage Applied to Outputs in High Z State -0.5V to +7.0V
 DC Input Voltage^[1] -3.0V to +7.0V

Static Discharge Voltage > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current > 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Military ^[2]	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	7B135-15 7B1342-15		7B134-20 7B135-20 7B1342-20		7B134-25 7B135-25 7B1342-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 4.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2		2.2		2.2		V
V _{IL}	Input LOW Voltage			0.8		0.8		0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	-10	+10	µA
I _{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V _O ≤ V _{CC}	-10	+10	-10	+10	-10	+10	µA
I _{CC}	Operating Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'1	260		240		220	mA
			Mil/Ind					260	
I _{SB1}	Standby Current (Both Ports TTL Levels)	\overline{CE}_L and $\overline{CE}_R \geq V_{IH}$, f = f _{MAX} ^[4]	Com'1	110		100		95	mA
			Mil/Ind					100	
I _{SB2}	Standby Current (One Port TTL Level)	\overline{CE}_L and $\overline{CE}_R \geq V_{IH}$, f = f _{MAX} ^[4]	Com'1	165		155		145	mA
			Mil/Ind					170	
I _{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports \overline{CE} and $\overline{CE}_R \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0 ^[4]	Com'1	15		15		15	mA
			Mil/Ind					30	
I _{SB4}	Standby Current (One Port CMOS Level)	One Port \overline{CE}_L or $\overline{CE}_R \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, Active Port Outputs, f = f _{MAX} ^[4]	Com'1	160		150		140	mA
			Mil/Ind					160	

Notes:

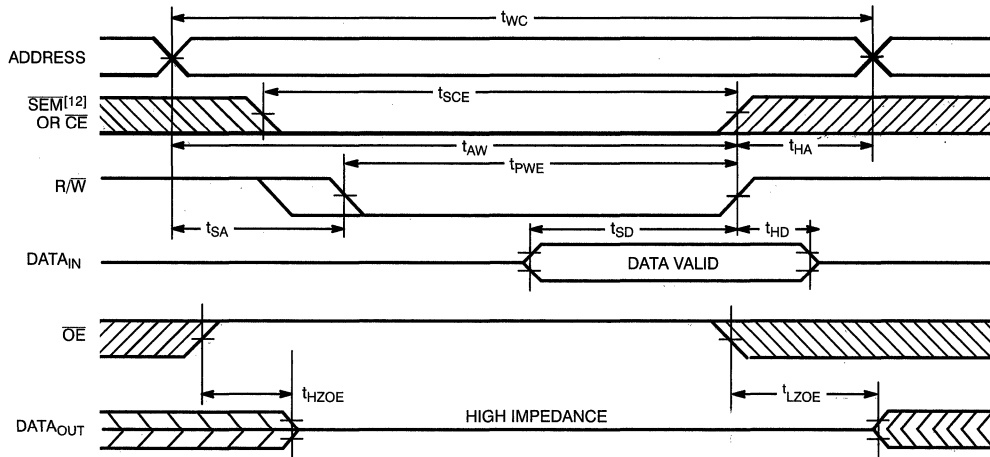
1. Pulse width < 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

Switching Characteristics Over the Operating Range^[7, 8]

Parameter	Description	7B135-15 7B1342-15		7B134-20 7B135-20 7B1342-20		7B134-25 7B135-25 7B1342-25		7B134-35 7B135-35 7B1342-35		7B134-55 7B135-55 7B1342-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	15		20		25		35		55		ns
t _{AA}	Address to Data Valid		15		20		25		35		55	ns
t _{OHA}	Output Hold From Address Change	3		3		3		3		3		ns
t _{ACE}	\overline{CE} LOW to Data Valid		15		20		25		35		55	ns
t _{DOE}	\overline{OE} LOW to Data Valid		10		13		15		20		25	ns
t _{LZOE} ^[9, 10]	\overline{OE} Low to Low Z	3		3		3		3		3		ns
t _{HZOE} ^[9, 10]	\overline{OE} HIGH to High Z		10		13		15		20		25	ns
t _{LZCE} ^[9, 10]	\overline{CE} LOW to Low Z	3		3		3		3		3		ns
t _{HZCE} ^[9, 10]	\overline{CE} HIGH to High Z		10		13		15		20		25	ns
t _{PU}	\overline{CE} LOW to Power Up	0		0		0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power Down		15		20		25		35		55	ns
WRITE CYCLE												
t _{WC}	Write Cycle Time	15		20		25		35		55		ns
t _{SCE}	\overline{CE} LOW to Write End	12		15		20		30		50		ns
t _{AW}	Address Set-Up to Write End	12		15		20		30		50		ns
t _{HA}	Address Hold from Write End	2		2		2		2		2		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t _{PWE}	Write Pulse Width	12		15		20		25		50		ns
t _{SD}	Data Set-Up to Write End	10		13		15		15		25		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{HZWE} ^[10]	R/ \overline{W} LOW to High Z		10		13		15		20		25	ns
t _{LZWE} ^[10]	R/ \overline{W} HIGH to Low Z	3		3		3		3		3		ns
t _{WDD} ^[11]	Write Pulse to Data Delay		30		40		50		60		70	ns
t _{DDD} ^[11]	Write Data Valid to Read Data Valid		25		30		30		35		40	ns
SEMAPHORE TIMING^[12]												
t _{SOP}	SEM Flag Update Pulse (\overline{OE} or SEM)	10		10		10		15		15		ns
t _{SWRD}	SEM Flag Write to Read Time	5		5		5		5		5		ns
t _{SPS}	SEM Flag Contention Window	5		5		5		5		5		ns

Notes:

- See the last page of this specification for Group A subgroup testing information.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance
- At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
- Test conditions used are Load 3.
- For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
- Semaphore timing applies only to CY7B1342.

Switching Waveforms (continued)
Write Cycle No. 1: \overline{OE} Three-States Data I/Os (Either Port)^[17, 18, 19]


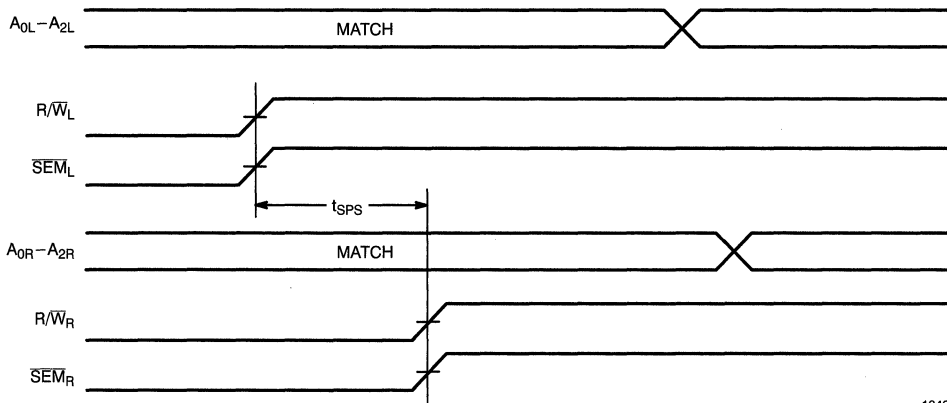
1342-12

Notes:

17. The internal write time of the memory is defined by the overlap of \overline{CE} or \overline{SEM} LOW and $\overline{R/W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
18. $\overline{R/W}$ must be HIGH during all address transactions.
19. If \overline{OE} is LOW during a $\overline{R/W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or $(t_{HZWE} + t_{SD})$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD} . If \overline{OE} is HIGH during a $\overline{R/W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE} .

Switching Waveforms (continued)

Timing Diagram of Semaphore Contention (CY7B1342 only)[22, 23, 24]

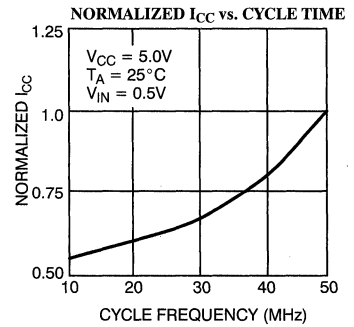
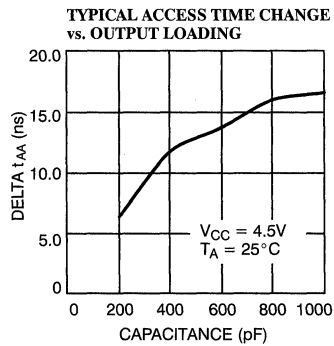
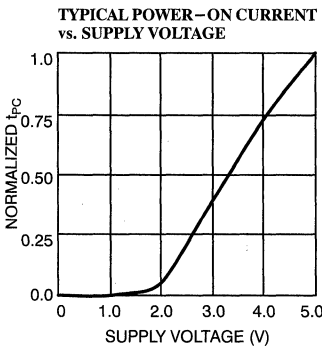
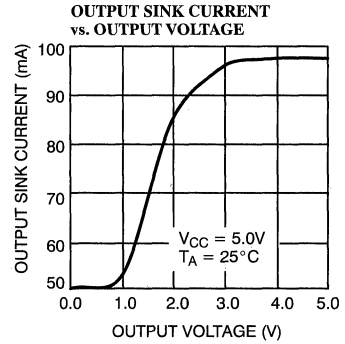
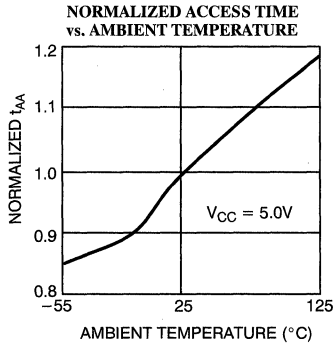
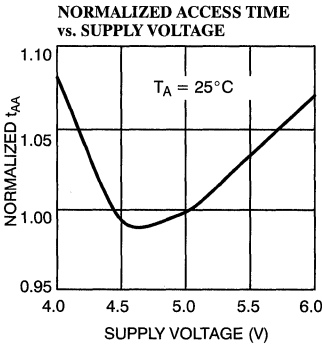
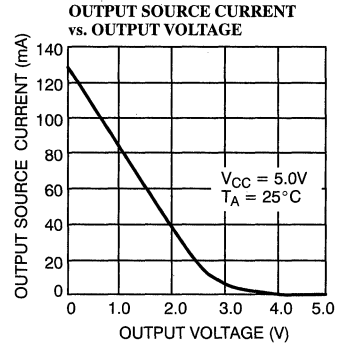
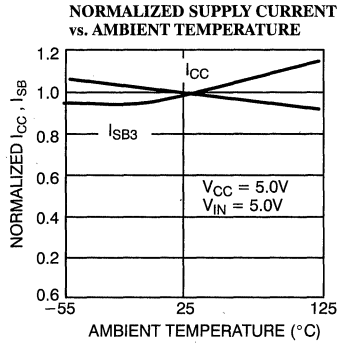
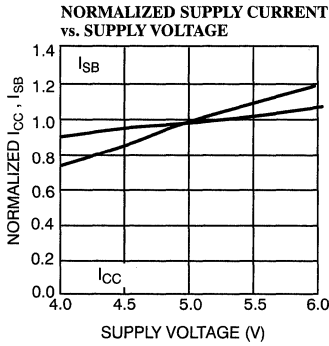


1342-15

Notes:

- 22. $I/O_{0R} = I/O_{0L} = \text{LOW}$ (request semaphore); $\overline{CE}_R = \overline{CE}_L = \text{HIGH}$.
- 23. Semaphores are reset (available to both ports) at cycle start.
- 24. If t_{SPS} is violated, it is guaranteed that only one side will gain access to the semaphore.

Typical DC and AC Characteristics





MILITARY SPECIFICATIONS
Group A Subgroup Testing

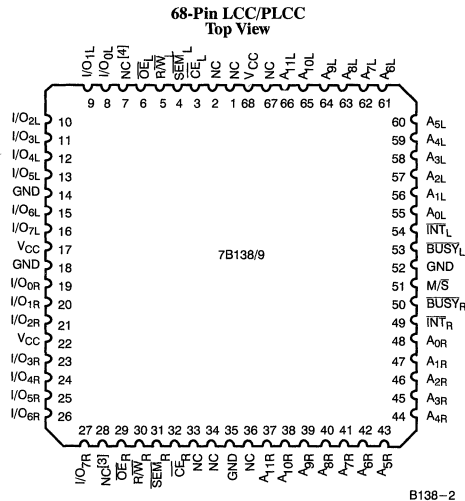
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3
I _{SB3}	1, 2, 3
I _{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11
SEMAPHORE CYCLE	
t _{SOD}	7, 8, 9, 10, 11
t _{SWRD}	7, 8, 9, 10, 11
t _{SPS}	7, 8, 9, 10, 11

Document #: 38-00161-D

Pin Configuration

Pin Definitions

Left Port	Right Port	Description
I/O _{0L} -7 _L (8 _L)	I/O _{0R} -7 _R (8 _R)	Data Bus Input/Output
A _{0L} -11 _L	A _{0R} -11 _R	Address Lines
\overline{CE}_L	\overline{CE}_R	Chip Enable
\overline{OE}_L	\overline{OE}_R	Output Enable
R/ \overline{W}_L	R/ \overline{W}_R	Read/Write Enable
SEM _L	SEM _R	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O ₀ pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.
INT _L	INT _R	Interrupt Flag. \overline{INT}_L is set when right port writes location FFE and is cleared when left port reads location FFE. \overline{INT}_R is set when left port writes location FFF and is cleared when right port reads location FFF.
BUSY _L	BUSY _R	Busy Flag
M/ \overline{S}		Master or Slave Select
V _{CC}		Power
GND		Ground

Selection Guide

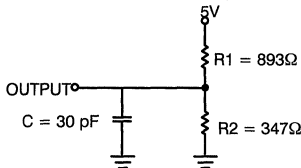
		7B138-15 7B139-15	7B138-25 7B139-25	7B138-35 7B139-35	7B138-55 7B139-55
Maximum Access Time (ns)		15	25	35	55
Maximum Operating Current (mA)	Commercial	260	220	210	210
	Military/Industrial		280	250	250
Maximum Standby Current for I _{SB1} (mA)	Commercial	110	95	90	90
	Military/Industrial		100	95	95

Electrical Characteristics Over the Operating Range^[5] (continued)

Parameter	Description	Test Conditions	7B138-35 7B139-35		7B138-55 7B139-55		Unit	
			Min.	Max.	Min.	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 4.0 mA		0.4		0.4	V	
V _{IH}	Input HIGH Voltage		2.2		2.2		V	
V _{IL}	Input LOW Voltage			0.8		0.8	V	
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	μA	
I _{OZ}	Output Leakage Current	Output Disabled, GND ≤ V _O ≤ V _{CC}	-10	+10	-10	+10	μA	
I _{CC}	Operating Current	V _{CC} = Max., I _{OUT} = 0 mA, Outputs Disabled	Com'l		210		210	mA
			Mil/Ind		250		250	
I _{SB1}	Standby Current (Both Ports TTL Levels)	C _{EL} and C _{ER} ≥ V _{IH} , f = f _{MAX} ^[6]	Com'l		90		90	mA
			Mil/Ind		95		95	
I _{SB2}	Standby Current (One Port TTL Level)	C _{EL} and C _{ER} ≥ V _{IH} , f = f _{MAX} ^[6]	Com'l		135		135	mA
			Mil/Ind		160		160	
I _{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports C _{EL} and C _{ER} ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0 ^[6]	Com'l		15		15	mA
			Mil/Ind		30		30	
I _{SB4}	Standby Current (One Port CMOS Level)	One Port C _{EL} or C _{ER} ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, Active Port Outputs, f = f _{MAX} ^[6]	Com'l		130		130	mA
			Mil/Ind		140		140	

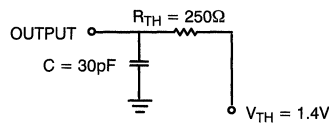
Capacitance^[7]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz,	10	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.0V	15	pF

AC Test Loads and Waveforms


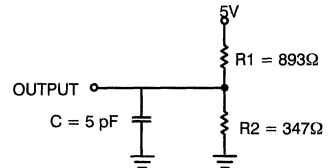
(a) Normal Load (Load 1)

B138-3



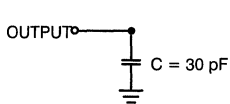
(b) Thévenin Equivalent (Load 1)

B138-4



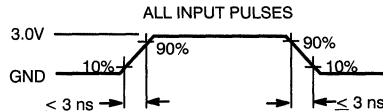
(c) Three-State Delay (Load 3)

B138-5



Load (Load 2)

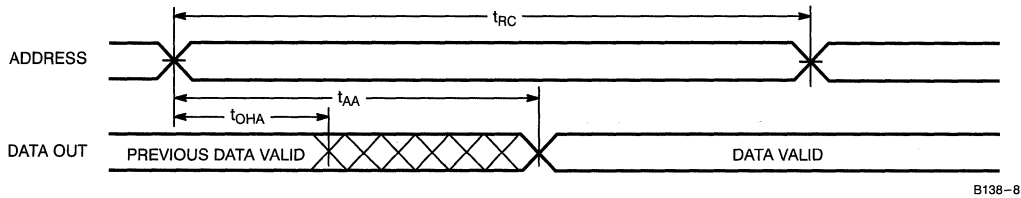
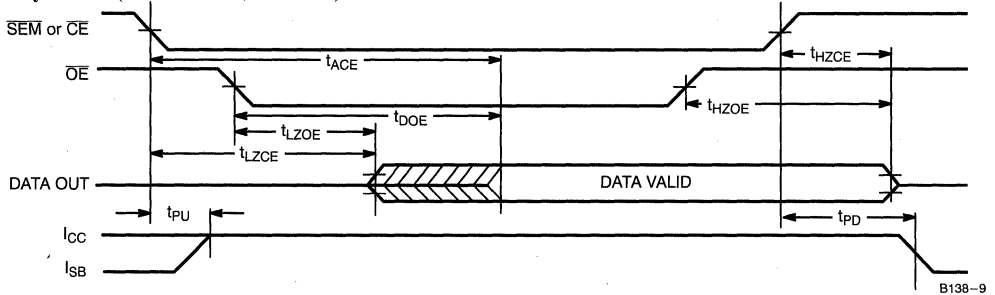
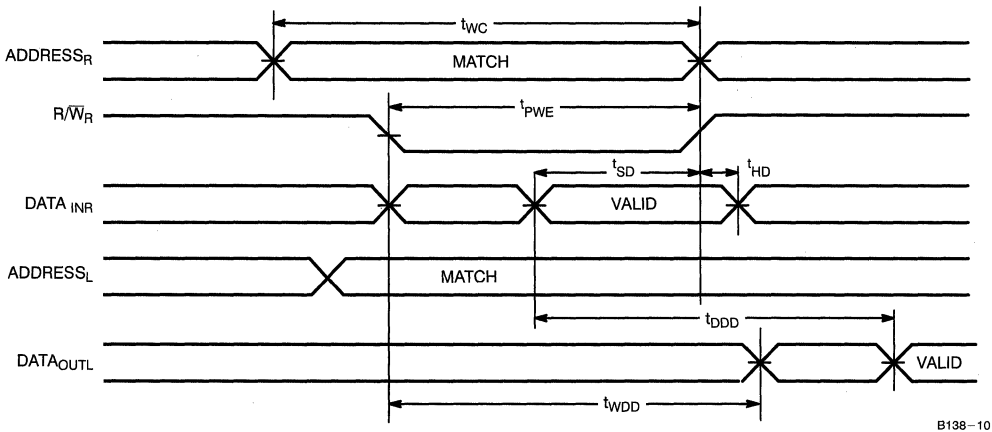
B138-6



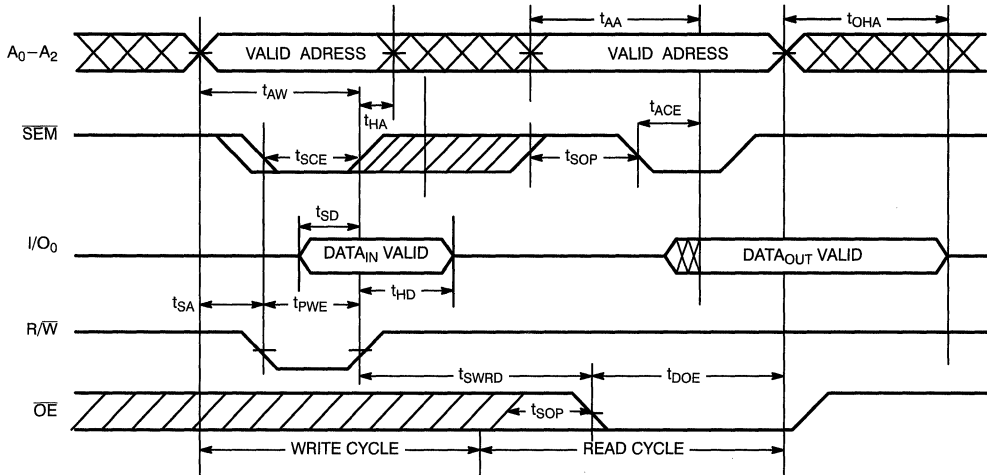
B138-7

Note:

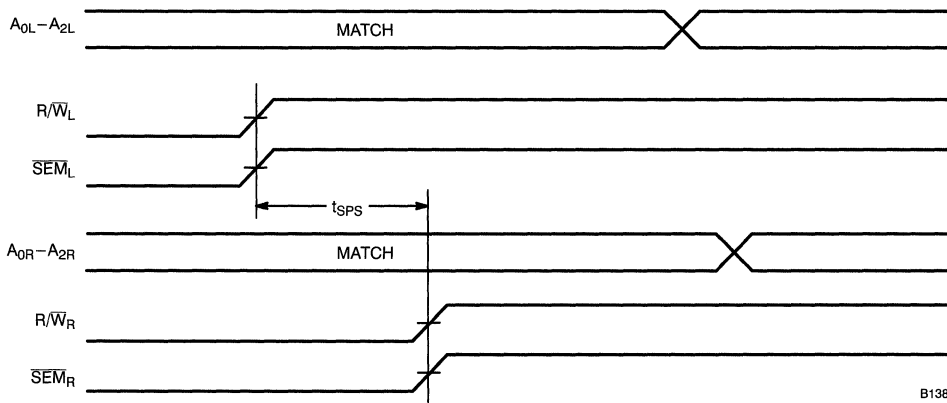
7. Tested initially and after any design or process changes that may affect these parameters.

Switching Waveforms
Read Cycle No. 1 (Either Port Address Access)^[14, 15]

Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access)^[14, 16, 17]

Read Timing with Port-to-Port Delay ($M/\overline{S} = L$)^[18, 19]

Notes:

- 14. R/\overline{W} is HIGH for read cycle.
- 15. Device is continuously selected $\overline{CE} = \text{LOW}$ and $\overline{OE} = \text{LOW}$. This waveform cannot be used for semaphore reads.
- 16. Address valid prior to or coincident with \overline{CE} transition LOW.
- 17. $\overline{CE}_L = L, \overline{SEM} = H$ when accessing RAM. $\overline{CE} = H, \overline{SEM} = L$ when accessing semaphores.
- 18. $BUSY = \text{HIGH}$ for the writing port.
- 19. $\overline{CE}_L = \overline{CE}_R = \text{LOW}$.

Switching Waveforms (continued)
Semaphore Read After Write Timing, Either Side^[24]


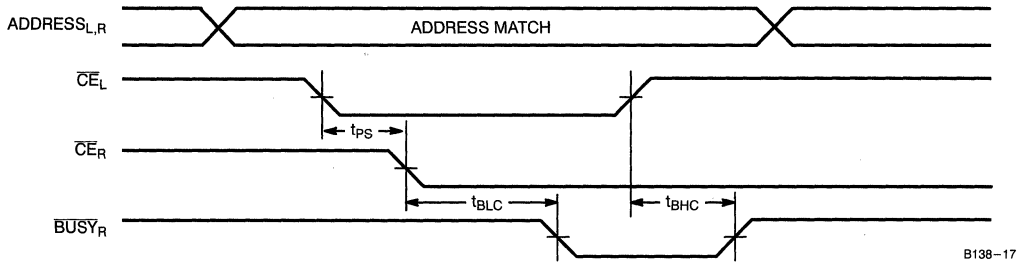
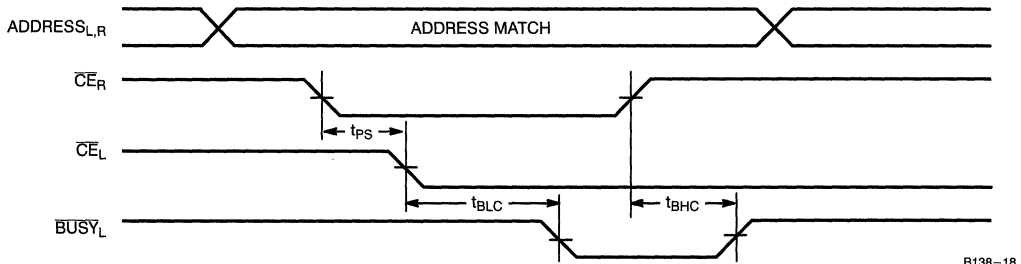
B138-13

Timing Diagram of Semaphore Contention^[25, 26, 27]


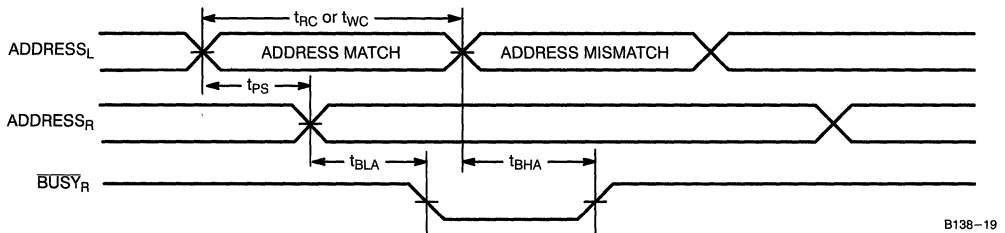
B138-14

Notes:

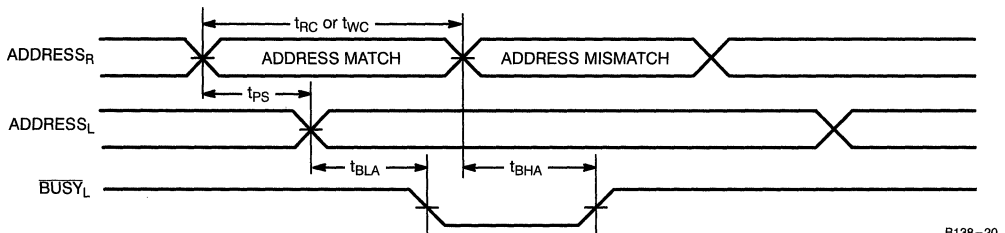
24. $\overline{CE} = \text{HIGH}$ for the duration of the above timing (both write and read cycle).
25. $I/O_{0R} = I/O_{0L} = \text{LOW}$ (request semaphore); $\overline{CE}_R = \overline{CE}_L = \text{HIGH}$
26. Semaphores are reset (available to both ports) at cycle start.
27. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Switching Waveforms (continued)
Busy Timing Diagram No. 1 (\overline{CE} Arbitration)^[28]
 \overline{CE}_L Valid First:

 \overline{CE}_R Valid First:

Busy Timing Diagram No. 2 (Address Arbitration)^[28]

Left Address Valid First:



Right Address Valid First:


Note:

28. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $BUSY$ will be asserted.

Architecture

The CY7B138/9 consists of an array of 4K words of 8/9 bits each of dual-port RAM cells, I/O and address lines, and control signals (\overline{CE} , \overline{OE} , R/W). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a \overline{BUSB} pin is provided on each port. Two interrupt (\overline{INT}) pins can be utilized for port-to-port communication. Two semaphore (\overline{SEM}) control pins are used for allocating shared resources. With the M/S pin, the CY7B138/9 can function as a master (\overline{BUSB} pins are outputs) or as a slave (\overline{BUSB} pins are inputs). The CY7B138/9 has an automatic power-down feature controlled by \overline{CE} . Each port is provided with its own output enable control (\overline{OE}), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/W in order to guarantee a valid write. A write operation is controlled by either the \overline{OE} pin (see Write Cycle No. 1 waveform) or the R/W pin (see Write Cycle No. 2 waveform). Data can be written to the device t_{HZOE} after the \overline{OE} is deasserted or t_{HZWF} after the falling edge of R/W. Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the \overline{OE} and \overline{CE} pins. Data will be available t_{ACE} after \overline{CE} or t_{DOE} after \overline{OE} is asserted. If the user of the CY7B138/9 wishes to access a semaphore flag, then the \overline{SEM} pin must be asserted instead of the \overline{CE} pin.

Interrupts

The interrupt flag (\overline{INT}) permits communications between ports. When the left port writes to location FFF, the right port's interrupt flag (\overline{INT}_R) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag (\overline{INT}_L) is accomplished when the right port writes to location FFE. This flag is cleared when the left port reads location FFE. The message at FFF or FFE is user-defined. See *Table 2* for input requirements for \overline{INT} . \overline{INT}_R and \overline{INT}_L are push-pull outputs and do not require pull-up resistors to operate. \overline{BUSY}_L and \overline{BUSY}_R in master mode are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7B138/9 provides on-chip arbitration to alleviate simultaneous memory location access (contention). If both ports' \overline{CE} s are asserted and an address match occurs within t_{PS} of each other the Busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. \overline{BUSB} will be asserted t_{BLA} after an address match or t_{BLC} after \overline{CE} is taken LOW.

Master/Slave

A M/S pin is provided in order to expand the word width by configuring the device as either a master or a slave. The \overline{BUSB} output of the master is connected to the \overline{BUSB} input of the slave. This will allow the device to interface to a master device with no external components. Writing of slave devices must be delayed until after the \overline{BUSB} input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation. When presented as a HIGH input, the M/S pin allows the device to be used as a master and therefore the \overline{BUSB} line is an output. \overline{BUSB} can then be used to send the arbitration outcome to a slave.

Semaphore Operation

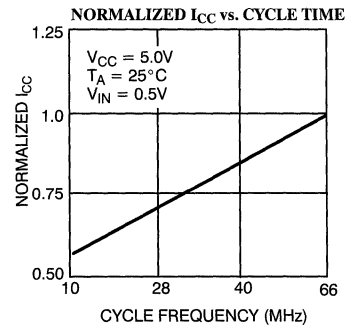
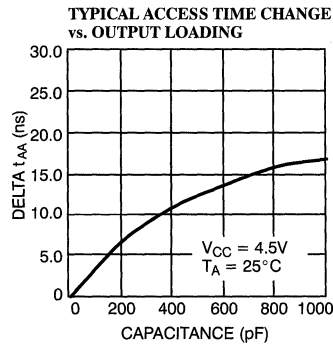
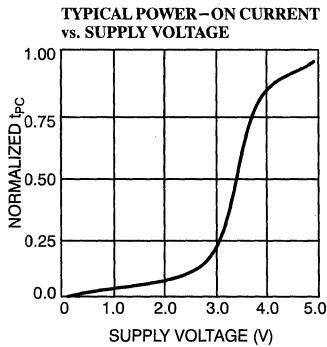
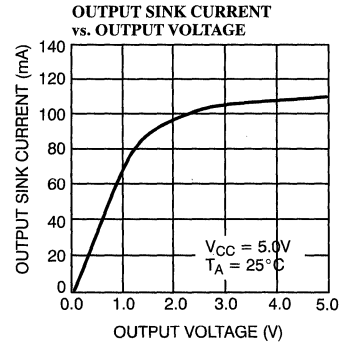
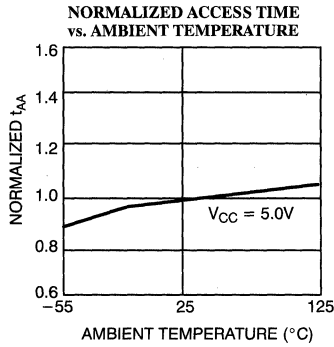
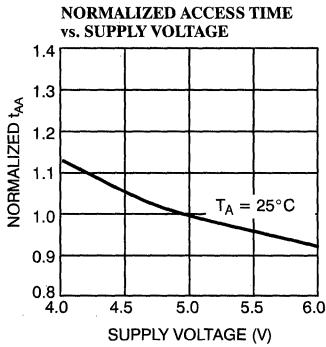
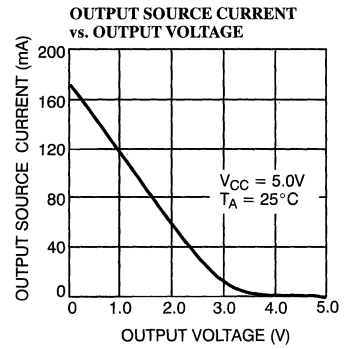
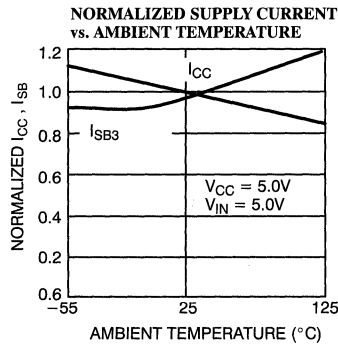
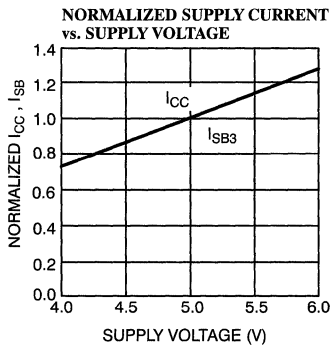
The CY7B138/9 provides eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, \overline{SEM} or \overline{OE} must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control over the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting \overline{SEM} LOW. The \overline{SEM} pin functions as a chip enable for the semaphore latches (\overline{CE} must remain HIGH during \overline{SEM} LOW). A_{0-2} represents the semaphore address. \overline{OE} and R/W are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O₀ is used. If a zero is written to the left port of an unused semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{PS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. All semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Typical DC and AC Characteristics


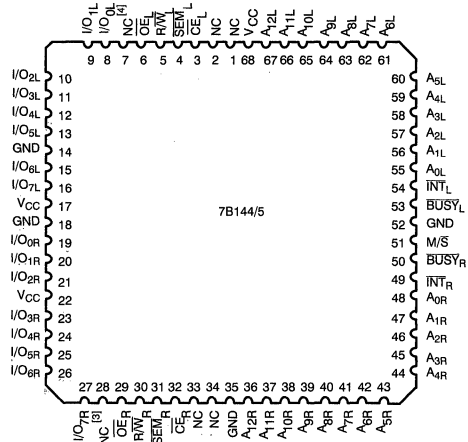
**MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics**

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3
I _{SB3}	1, 2, 3
I _{SB4}	1, 2, 3

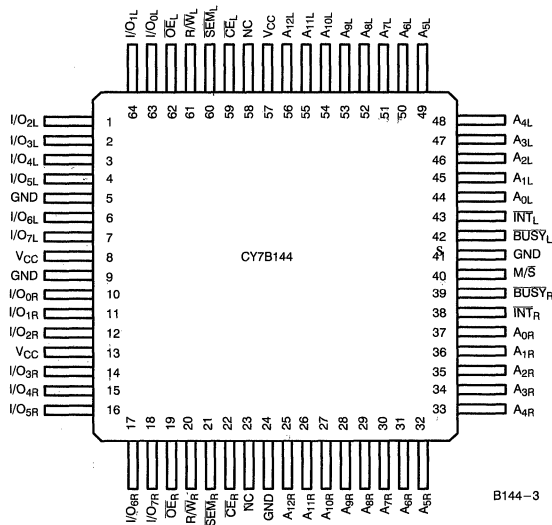
Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11
BUSY/INTERRUPT TIMING	
t _{BLA}	7, 8, 9, 10, 11
t _{BHA}	7, 8, 9, 10, 11
t _{BLC}	7, 8, 9, 10, 11
t _{BHC}	7, 8, 9, 10, 11
t _{PS}	7, 8, 9, 10, 11
t _{INS}	7, 8, 9, 10, 11
t _{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t _{WB}	7, 8, 9, 10, 11
t _{WH}	7, 8, 9, 10, 11
t _{BDD}	7, 8, 9, 10, 11
t _{DDD}	7, 8, 9, 10, 11
t _{WDD}	7, 8, 9, 10, 11

Document #: 38-00162-G

Pin Configurations
68-Pin LCC/PLCC
Top View


B144-2

64-Pin TQFP
Top View


B144-3

Notes:

3. I/O_{8R} on the CY7B145.
4. I/O_{8L} on the CY7B145.



Selection Guide

		7B144-15 7B145-15	7B144-25 7B145-25	7B144-35 7B145-35	7B144-55 7B145-55
Maximum Access Time (ns)		15	25	35	55
Maximum Operating Current (mA)	Commercial	260	220	210	210
	Military		280	250	
Maximum Standby Current for I _{SB1} (mA)	Commercial	110	95	90	90
	Military		100	95	

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied -55°C to +125°C
 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Voltage Applied to Outputs in High Z State -0.5V to +7.0V
 DC Input Voltage^[5] -0.5V to +7.0V
 Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Military ^[6]	-55°C to +125°C	5V ± 10%

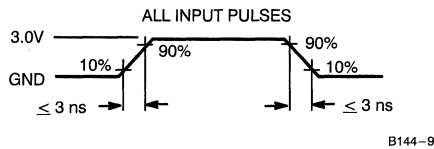
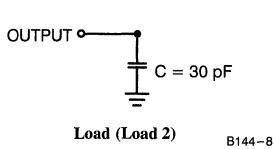
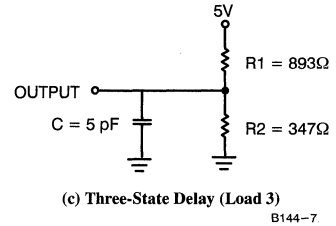
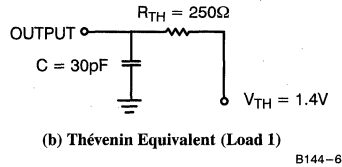
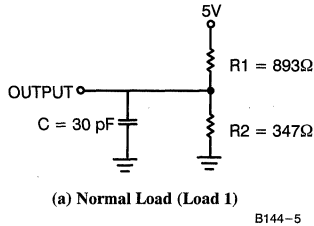
Notes:

5. Pulse width < 20 ns.

6. T_A is the “instant on” case temperature.

Capacitance^[9]

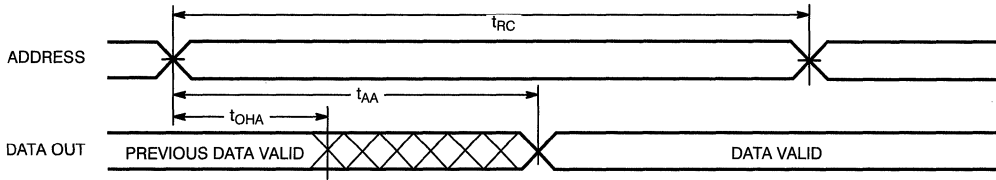
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{V}$	10	pF
C_{OUT}	Output Capacitance		15	pF

AC Test Loads and Waveforms

Switching Characteristics Over the Operating Range^[7, 10]

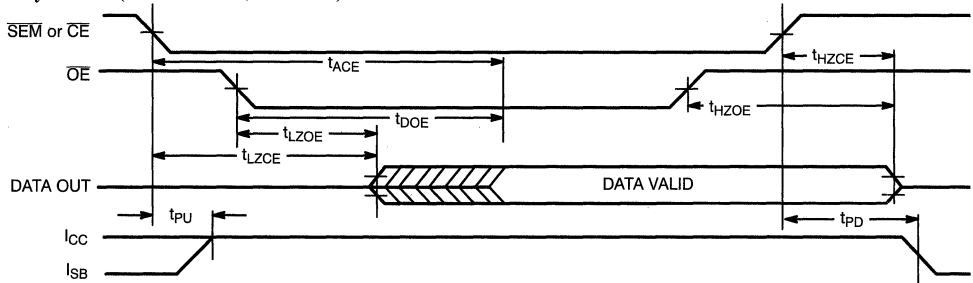
Parameter	Description	7B144-15 7B145-15		7B144-25 7B145-25		7B144-35 7B145-35		7B144-55 7B145-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15		25		35		55		ns
t_{AA}	Address to Data Valid		15		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		ns
t_{ACE}	\overline{CE} LOW to Data Valid		15		25		35		55	ns
t_{DOE}	\overline{OE} LOW to Data Valid		10		15		20		25	ns
$t_{LZOE}^{[11, 12]}$	\overline{OE} Low to Low Z	3		3		3		3		ns
$t_{HZOE}^{[11, 12]}$	\overline{OE} HIGH to High Z		10		15		20		25	ns
$t_{LZCE}^{[11, 12]}$	\overline{CE} LOW to Low Z	3		3		3		3		ns
$t_{HZCE}^{[11, 12]}$	\overline{CE} HIGH to High Z		10		15		20		25	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		15		25		35		55	ns

Notes:

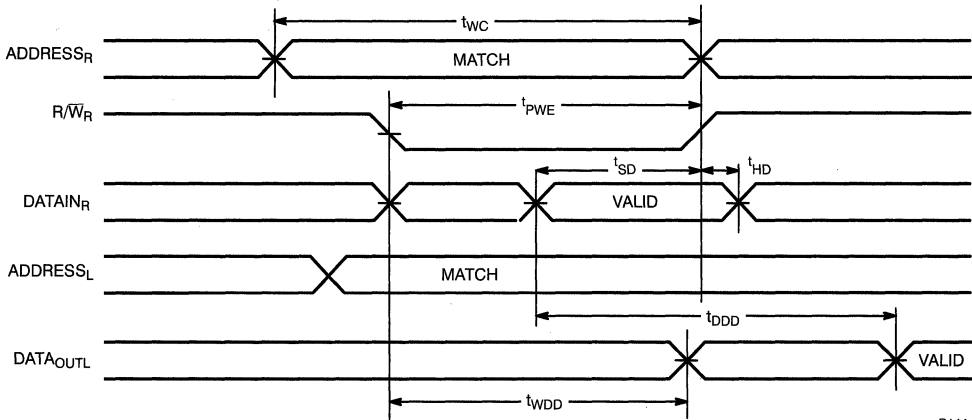
- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE} .
- Test conditions used are Load 3.

Switching Waveforms
Read Cycle No. 1 (Either Port Address Access)^[15, 16]


B144-10

Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access)^[15, 17, 18]


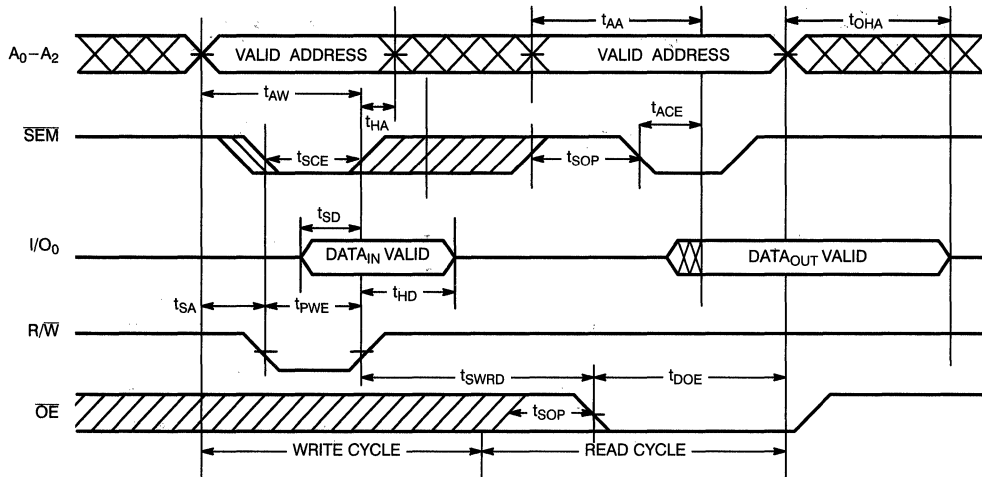
B144-11

Read Timing with Port-to-Port Delay ($M/\overline{S} = L$)^[19, 20]


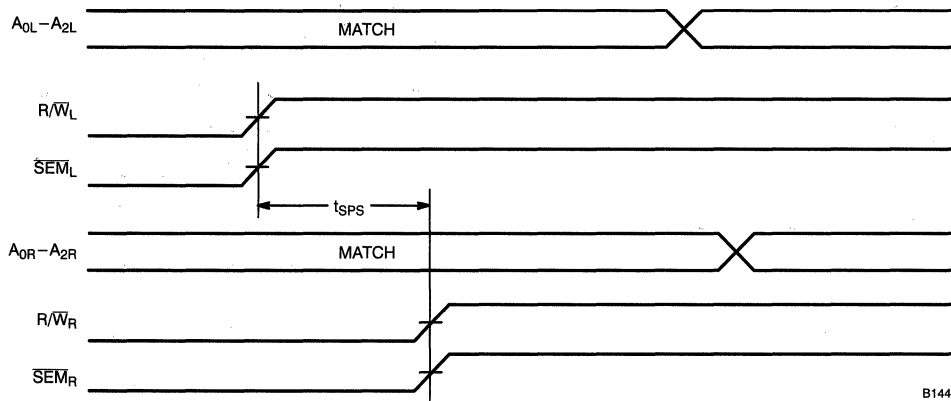
B144-12

Notes:

15. R/\overline{W} is HIGH for read cycle.
16. Device is continuously selected $\overline{CE} = \text{LOW}$ and $\overline{OE} = \text{LOW}$. This waveform cannot be used for semaphore reads.
17. Address valid prior to or coincident with \overline{CE} transition LOW.
18. $\overline{CE}_L = L$, $\overline{SEM} = H$ when accessing RAM. $\overline{CE} = H$, $\overline{SEM} = L$ when accessing semaphores.
19. $\overline{BUSY} = \text{HIGH}$ for the writing port.
20. $\overline{CE}_L = \overline{CE}_R = \text{LOW}$.

Switching Waveforms (continued)
Semaphore Read After Write Timing, Either Side^[25]


B144-15

Semaphore Contention^[26, 27, 28]


B144-16

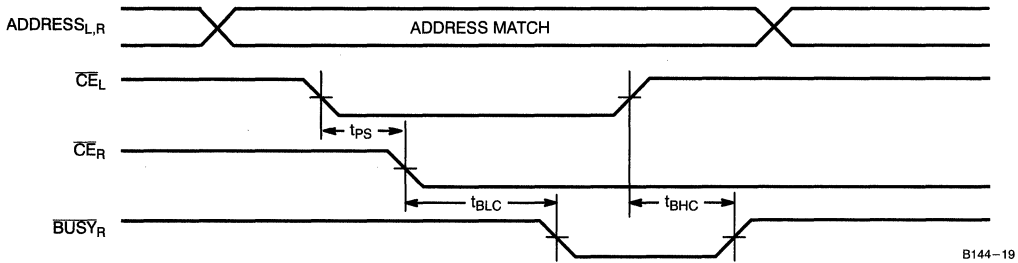
Notes:

 25. $\overline{CE} = \text{HIGH}$ for the duration of the above timing (both write and read cycle).

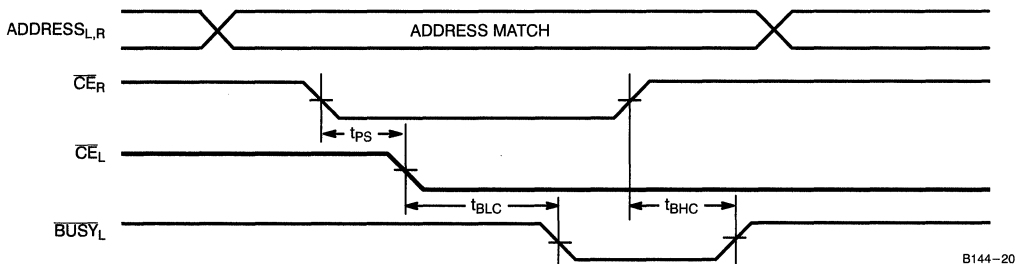
 26. $I/O_{0R} = I/O_{0L} = \text{LOW}$ (request semaphore); $\overline{CE}_R = \overline{CE}_L = \text{HIGH}$

27. Semaphores are reset (available to both ports) at cycle start.

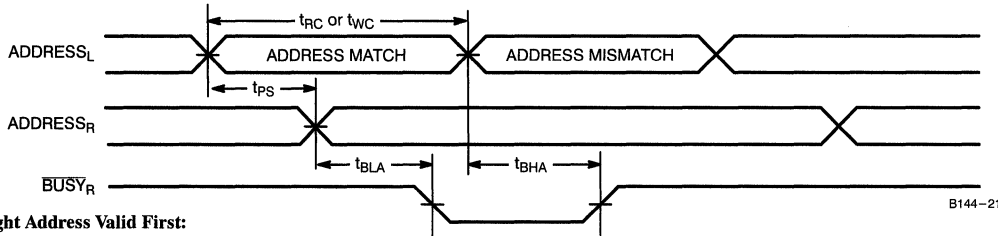
 28. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Switching Waveforms (continued)
Busy Timing Diagram No. 1 (\overline{CE} Arbitration)^[29]
 \overline{CE}_L Valid First:


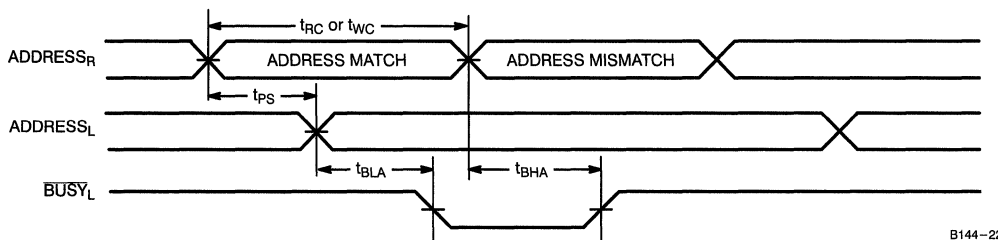
B144-19

 \overline{CE}_R Valid First:


B144-20

Busy Timing Diagram No. 2 (Address Arbitration)^[29]
Left Address Valid First:


B144-21

Right Address Valid First:


B144-22

Note:

29. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $BUSY$ will be asserted.
 30. t_{HA} depends on which enable pin (\overline{CE}_L or R/\overline{WL}) is deasserted first.

31. t_{INS} or t_{INR} depends on which enable pin (\overline{CE}_L or R/\overline{WL}) is asserted last.

Architecture

The CY7B144/5 consists of an array of 8K words of 8/9 bits each of dual-port RAM cells, I/O and address lines, and control signals (\overline{CE} , \overline{OE} , R/\overline{W}). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $BUSY$ pin is provided on each port. Two interrupt (\overline{INT}) pins can be utilized for port-to-port communication. Two semaphore (\overline{SEM}) control pins are used for allocating shared resources. With the M/\overline{S} pin, the CY7B144/5 can function as a Master ($BUSY$ pins are outputs) or as a slave ($BUSY$ pins are inputs). The CY7B144/5 has an automatic power-down feature controlled by \overline{CE} . Each port is provided with its own output enable control (\overline{OE}), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/\overline{W} in order to guarantee a valid write. A write operation is controlled by either the \overline{OE} pin (see Write Cycle No.1 waveform) or the R/\overline{W} pin (see Write Cycle No.2 waveform). Data can be written to the device t_{HZOE} after the \overline{OE} is deasserted or t_{HZWF} after the falling edge of R/\overline{W} . Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the \overline{OE} and \overline{CE} pins. Data will be available t_{ACE} after \overline{CE} or t_{DOE} after \overline{OE} are asserted. If the user of the CY7B144/5 wishes to access a semaphore flag, then the \overline{SEM} pin must be asserted instead of the \overline{CE} pin.

Interrupts

The interrupt flag (\overline{INT}) permits communications between ports. When the left port writes to location 1FFF, the right port's interrupt flag (\overline{INT}_R) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag (\overline{INT}_L) is accomplished when the right port writes to location 1FFE. This flag is cleared when the left port reads location 1FFE. The message at 1FFF or 1FFE is user-defined. See *Table 2* for input requirements for \overline{INT} . \overline{INT}_R and \overline{INT}_L are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7B144/5 provides on-chip arbitration to alleviate simultaneous memory location access (contention). If both ports' \overline{CE} s are asserted and an address match occurs within t_{PS} of each other the Busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. $BUSY$ will be asserted t_{BLA} after an address match or t_{BLC} after \overline{CE} is taken LOW. $BUSY_L$ and $BUSY_R$ in master mode are push-pull outputs and do not require pull-up resistors to operate.

Master/Slave

An M/\overline{S} pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $BUSY$ output of the master is connected to the $BUSY$ input of the slave. This will allow the device to interface to a master device with no external components. Writing of slave devices must be delayed until after the $BUSY$ input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation. When presented a HIGH input, the M/\overline{S} pin allows the device to be used as a master and therefore the $BUSY$ line is an output. $BUSY$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

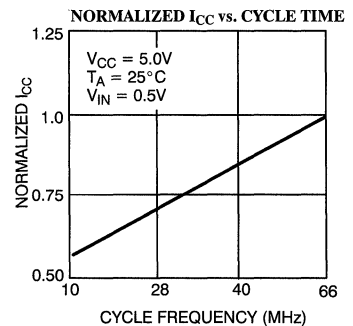
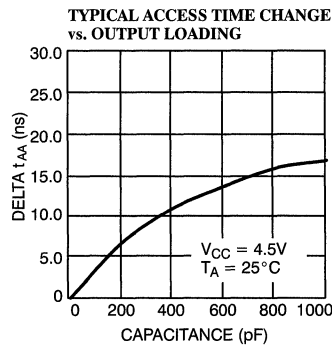
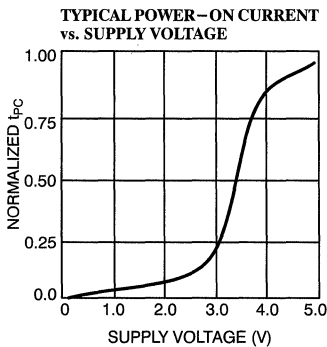
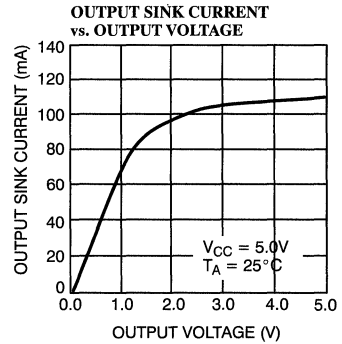
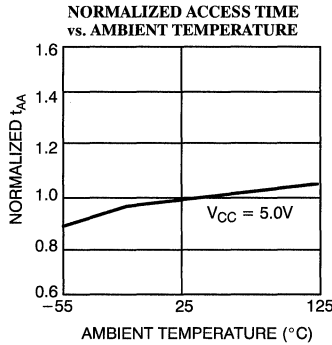
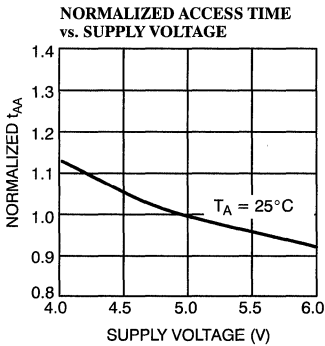
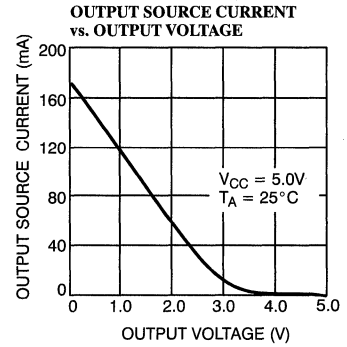
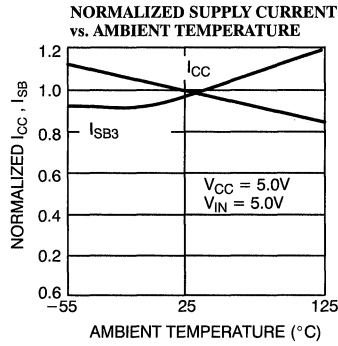
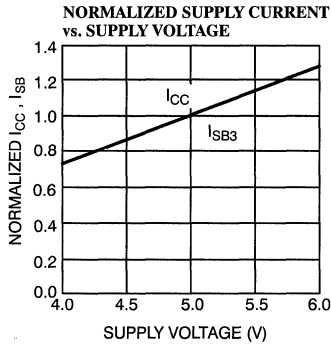
The CY7B144/5 provides eight semaphore latches which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a 0 to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, \overline{SEM} or \overline{OE} must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a 0), it assumes control over the shared resource, otherwise (reads a 1) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a 1), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a 1 is written to cancel its request.

Semaphores are accessed by asserting \overline{SEM} LOW. The \overline{SEM} pin functions as a chip enable for the semaphore latches (\overline{CE} must remain HIGH during \overline{SEM} LOW). A_{0-2} represents the semaphore address. \overline{OE} and R/\overline{W} are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O₀ is used. If a 0 is written to the left port of an unused semaphore, a 1 will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing 0 (the left port in this case). If the left port now relinquishes control by writing a 1 to the semaphore, the semaphore will be set to 1 for both sides. However, if the right port had requested the semaphore (written a 0) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{PS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. All Semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Typical DC and AC Characteristics


**MILITARY SPECIFICATIONS
Group A Subgroup Testing**
DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3
I _{SB3}	1, 2, 3
I _{SB4}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11
BUSY/INTERRUPT TIMING	
t _{BLA}	7, 8, 9, 10, 11
t _{BHA}	7, 8, 9, 10, 11
t _{BLC}	7, 8, 9, 10, 11
t _{BHC}	7, 8, 9, 10, 11
t _{PS}	7, 8, 9, 10, 11
t _{INS}	7, 8, 9, 10, 11
t _{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t _{WB}	7, 8, 9, 10, 11
t _{WH}	7, 8, 9, 10, 11
t _{BDD}	7, 8, 9, 10, 11
t _{DDD}	7, 8, 9, 10, 11
t _{WDD}	7, 8, 9, 10, 11

Document #: 38-00163-G

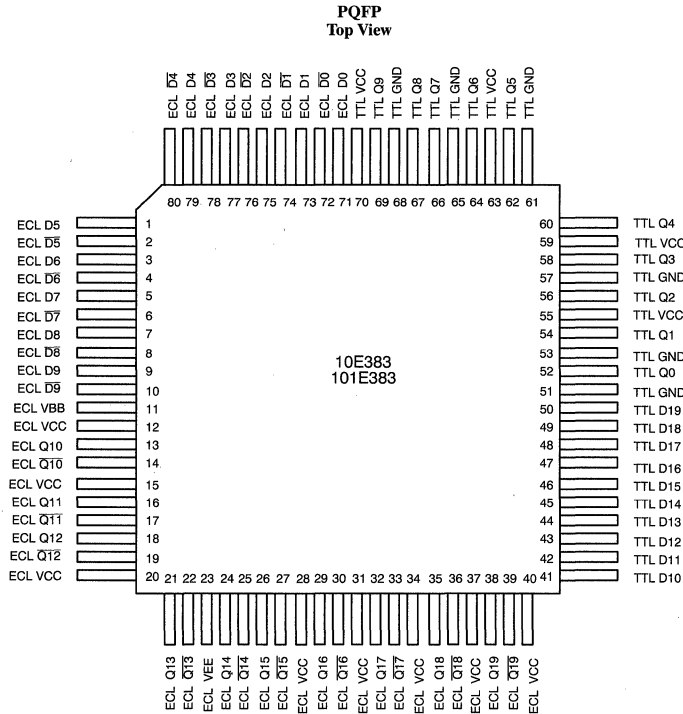


Section Contents

Data Communications Products

Page Number

Device	Description	
CY10E383	ECL/TTL/ECL Translator and High-Speed Bus Driver	7-1
CY101E383	ECL/TTL/ECL Translator and High-Speed Bus Driver	7-1
CY7B923	HOTLink™ Transmitter	7-8
CY7B933	HOTLink Receiver	7-8
CY7B951	SST™ SONET/SDH Serial Transceiver	7-35
CY7C971	100BASE-T4/10BASE-T Fast Ethernet Transceiver (CAT 3)	7-43
CY7B972	100BASE-TX/10BASE-T Fast Ethernet Transceiver	7-66
CY7B8392	Ethernet Coax Transceiver Interface	7-67
CY9266-T	HOTLink Evaluation Board	7-73
CY9266-C	HOTLink Evaluation Board	7-73
CY9266-F	HOTLink Evaluation Board	7-73

Pin Configurations (continued)

Selection Guide

	10E383-2 101E383-2	10E383-3 101E383-3
Maximum Propagation Delay Time (ns) (TTL to ECL)	2.5	3
Maximum Propagation Delay Time (ns) (ECL to TTL)	3.5	4
Maximum Operating Current (mA) Sum of I_{EE} and I_{CC}	270	270

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
TTL Supply Voltage to Ground Potential	-0.5V to +7.0V
TTL DC Input Voltage	-3.0V to +7.0V
ECL Supply Voltage V_{EE} to ECL V_{CC}	-7.0V to +0.5V
ECL Input Voltage	V_{EE} to +0.5V
ECL Output Current	-50 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V
Latch-Up Current	>200 mA

Operating Range

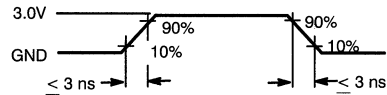
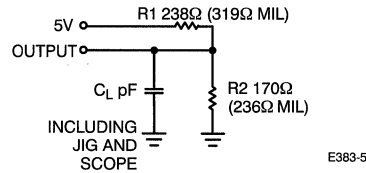
Range	I/O	Version	Ambient Temperature	ECL V_{EE}	TTL V_{CC}
Commercial	10K 10KH	10E	0°C to +75°C	-5.2V ± 5%	5V ± 5%
Commercial	100K	101E	0°C to +85°C	-4.2V to -5.46V	5V ± 5%
Military	10K 10KH	10E	-55°C to +125°C case	-5.2V ± 5%	5V ± 5%

TTL Electrical Characteristics Over the Operating Range^[2]

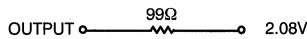
Parameter	Description	Test Conditions	10E383 101E383		Unit
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -3.2 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Max., I _{OL} = 16.0 mA		0.5	V
V _{IH}	Input HIGH Voltage ^[6]		2.0		V
V _{IL}	Input LOW Voltage ^[5]			0.8	V
V _{CD}	Input Clamp Diode Voltage	I _{IN} = -10 mA	-1.5		V
I _{OS} ^[7]	Output Short-Circuit Current	V _{CC} = Max., V _{OUT} = 0.5V ^[8]	-180	-40	mA
I _{IX}	Input Load Current ^[9]	GND ≤ V _I ≤ V _{CC}	-250	+20	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f max.		90	mA

Capacitance^[7]

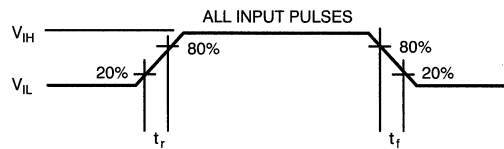
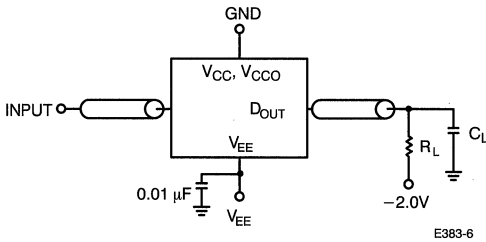
Parameter	Description	Max.	Unit
C _{IN}	Input Capacitance	4	pF
C _{OUT}	Output Capacitance	5	pF

TTL AC Test Load and Waveform^[10]


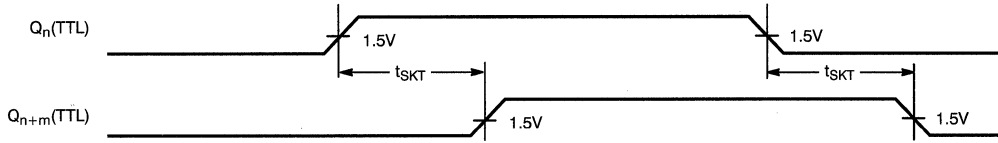
Equivalent to: THÉVENIN EQUIVALENT (Commercial)



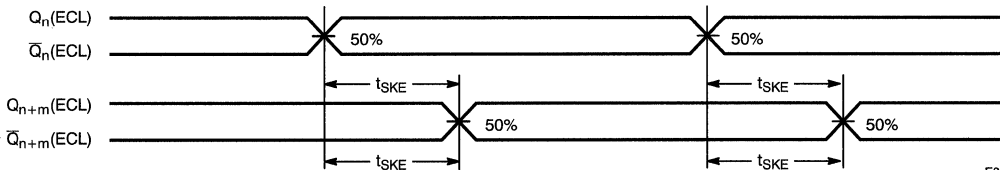
THÉVENIN EQUIVALENT (Military)


ECL AC Test Load and Waveform^[11, 12, 13, 14, 15, 16]

Notes:

- See AC Test Load and Waveform for test conditions.
- Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute. Military grade is specified as case temperature.
- Max. I_{BB} = -1 mA.
- The internal gain of the CY101/10E383 guarantees that the output voltage will not change for common mode signals to ±1V. Therefore, input C_{MRR} is infinite within the common mode range.
- These are absolute values with respect to device ground.
- Characterized initially and after any design or process changes that may affect these parameters.
- Not more than one output should be tested at a time. Duration of the short should not be more than one second.
- I/O pin leakage is the worst case of I_{IX} (where X = H or L).
- TTL test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH}, and C_L = 10 pF.
- V_{IL} = V_{IL} Min., V_{IH} = V_{IH} Max. on 10KH version.
- V_{IL} = -1.7V, V_{IH} = -0.9V on 101E version.
- ECL R_L = 50Ω, C_L < 5 pF (includes fixture and stray capacitance).
- All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
- t_r = t_f = 0.7 ns
- All timing measurements are made from the 50% point of all waveforms.

Switching Waveforms (continued)
**Skew Test (t_{SKT})
TTL Q_n -to-TTL Q_{n+m}**


E383-10

**Skew Test (t_{SKE})
ECL Q_n, \bar{Q}_n -to-ECL Q_{n+m}, \bar{Q}_{n+m}**


E383-11

ECL-to-TTL Truth Table

Inputs		Outputs
ECL D_n	ECL \bar{D}_n	TTL Q_n
Open ^[17]	Open ^[17]	L
L	H	L
H	L	H

Table 1. CY101E383 Nominal Voltages Applied in 100K System

Supply Pin	Single-Supply System	Dual-Supply System
TTL V_{CC}	+5.0V	+5.0V
TTL GND	0.0V	0.0V
ECL V_{CC}	+5.0V	0.0V
ECL V_{EE}	0.0V	-4.5V

TTL-to-ECL Truth Table

Inputs	Outputs	
TTL D_n	ECL Q_n	ECL \bar{Q}_n
L	L	H
H	H	L

Table 2. CY101E383 Nominal Voltages Applied in 101K System

Supply Pin	Single-Supply System	Dual-Supply System
TTL V_{CC}	+5.0V	+5.0V
TTL GND	0.0V	0.0V
ECL V_{CC}	+5.0V	0.0V
ECL V_{EE}	0.0V	-5.2V

Nominal Voltages

The CY101/10E383 can be used in dual $\pm 5V$ or single +5V supply systems. The supply pins should be connected as shown in *Tables 1* and *2*. This connection technique involves shifting up all ECL supply pins by 5V. When operating in single-supply systems, the ECL termination voltage level must also be shifted up by adding 5V. For example, if the termination is 50 ohms to -2V in a dual-supply system, the single +5V system should have 50 ohms to +3V. If the termination is a thevenin type, then the resistor tied to ground is now at +5V and the resistor tied to -5V is now at ground potential. Consideration should be given to the power supply so that adequate bypassing is made to isolate the ECL output switching noise from the supply. Having separate TTL and ECL +5V supply lines will help to reduce the noise. *Table 3* shows the CY10E383 nominal voltages applied in a 10K system.

Table 3. CY10E383 Nominal Voltages Applied in 10K System

Supply Pin	Single-Supply System	Dual-Supply System
TTL V_{CC}	+5.0V	+5.0V
TTL GND	0.0V	0.0V
ECL V_{CC}	+5.0V	0.0V
ECL V_{EE}	0.0V	-5.2V

Note:

17. The ECL inputs will pull to a known logic level if left open.

Transmitter/Receiver
Features

- Fibre Channel compliant
- IBM ESCON® compliant
- ATM-compliant
- 8B/10B-coded or 10-bit unencoded
- 160- to 330-Mbps data rate
- TTL synchronous I/O
- No external PLL components
- Triple PECL 100K serial outputs
- Dual PECL 100K serial inputs
- Low power: 350 mW (Tx), 650 mW (Rx)
- Compatible with fiber optic modules, coaxial cable, and twisted pair media
- Built-In Self-Test
- Single +5V supply
- 28-pin SOIC/PLCC/LCC
- 0.8µ BiCMOS

Functional Description

The CY7B923 HOTLink™ Transmitter and CY7B933 HOTLink Receiver are point-to-point communications building blocks that transfer data over high-speed serial links (fiber, coax, and twisted pair) at 160 to 330 Mbits/second. Figure 1 illustrates typical connections to host systems or controllers.

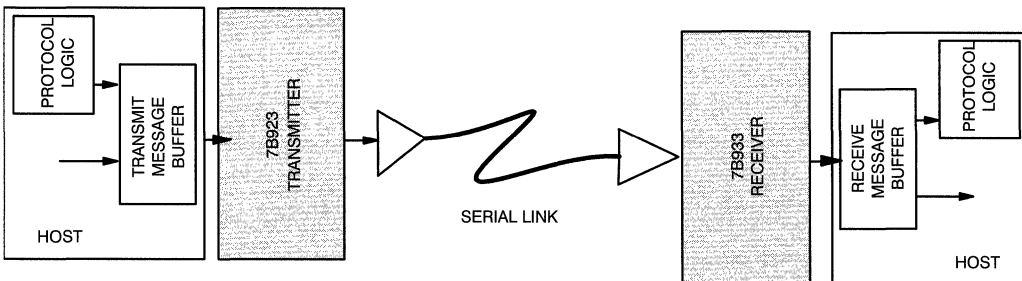
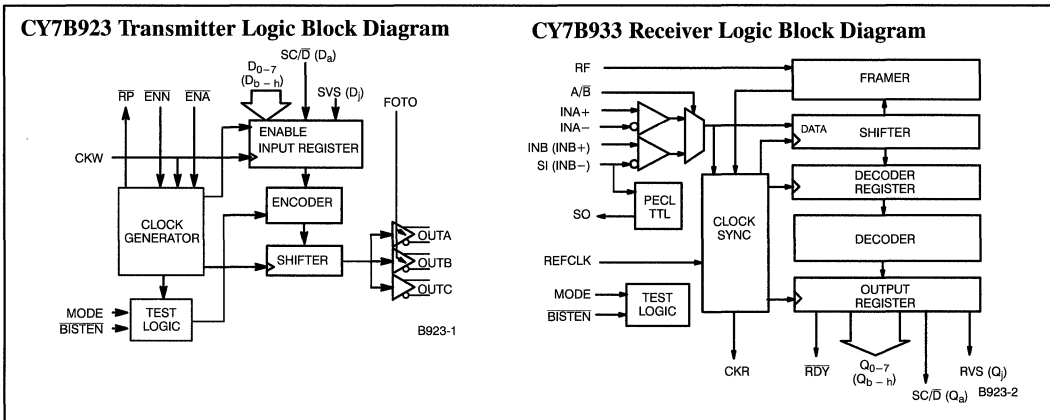
Eight bits of user data or protocol information are loaded into the HOTLink transmitter and are encoded. Serial data is shifted out of the three differential positive ECL (PECL) serial ports at the bit rate (which is 10 times the byte rate).

The HOTLink receiver accepts the serial bit stream at its differential line receiver inputs and, using a completely integrated PLL Clock Synchronizer, recovers the timing information necessary for data reconstruction. The bit stream is deserialized,

decoded, and checked for transmission errors. Recovered bytes are presented in parallel to the receiving host along with a byte rate clock.

The 8B/10B encoder/decoder can be disabled in systems that already encode or scramble the transmitted data. I/O signals are available to create a seamless interface with both asynchronous FIFOs (i.e., CY7C42X) and clocked FIFOs (i.e., CY7C44X). A Built-In Self-Test pattern generator and checker allows testing of the transmitter, receiver, and the connecting link as a part of a system diagnostic check.

HOTLink devices are ideal for a variety of applications where a parallel interface can be replaced with a high-speed point-to-point serial link. Applications include interconnecting workstations, servers, mass storage, and video transmission equipment.


Figure 1. HOTLink System Connections

B923-3

HOTLink is a trademark of Cypress Semiconductor Corporation.
 ESCON is a registered trademark of IBM.

Pin Descriptions
CY7B923 HOTLink Transmitter

Name	I/O	Description
D ₀₋₇ (D _{b-h})	TTL In	Parallel Data Input. Data is clocked into the Transmitter on the rising edge of CKW if EN \bar{A} is LOW (or on the next rising CKW with ENN LOW). If EN \bar{A} and ENN are HIGH, a Null character (K28.5) is sent. When MODE is HIGH, D _{0,1,...,7} become D _{b,c,...,h} respectively.
SC/ \bar{D} (D _a)	TTL In	Special Character/Data Select. A HIGH on SC/ \bar{D} when CKW rises causes the transmitter to encode the pattern on D ₀₋₇ as a control code (Special Character), while a LOW causes the data to be coded using the 8B/10B data alphabet. When MODE is HIGH, SC/ \bar{D} (D _a) acts as D _a input. SC/ \bar{D} has the same timing as D ₀₋₇ .
SVS (D _j)	TTL In	Send Violation Symbol. If SVS is HIGH when CKW rises, a Violation symbol is encoded and sent while the data on the parallel inputs is ignored. If SVS is LOW, the state of D ₀₋₇ and SC/ \bar{D} determines the code sent. In normal or test mode, this pin overrides the BIST generator and forces the transmission of a Violation code. When MODE is HIGH (placing the transmitter in unencoded mode), SVS (D _j) acts as the D _j input. SVS has the same timing as D ₀₋₇ .
EN \bar{A}	TTL In	Enable Parallel Data. If EN \bar{A} is LOW on the rising edge of CKW, the data is loaded, encoded, and sent. If EN \bar{A} and ENN are HIGH, the data inputs are ignored and the Transmitter will insert a Null character (K28.5) to fill the space between user data. EN \bar{A} may be held HIGH/LOW continuously or it may be pulsed with each data byte to be sent. If EN \bar{A} is being used for data control, ENN will normally be strapped HIGH, but can be used for BIST function control.
ENN	TTL In	Enable Next Parallel Data. If ENN is LOW, the data appearing on D ₀₋₇ at the next rising edge of CKW is loaded, encoded, and sent. If EN \bar{A} and ENN are HIGH, the data appearing on D ₀₋₇ at the next rising edge of CKW will be ignored and the Transmitter will insert a Null character to fill the space between user data. ENN may be held HIGH/LOW continuously or it may be pulsed with each data byte sent. If ENN is being used for data control, EN \bar{A} will normally be strapped HIGH, but can be used for BIST function control.
CKW	TTL In	Clock Write. CKW is both the clock frequency reference for the multiplying PLL that generates the high-speed transmit clock, and the byte rate write signal that synchronizes the parallel data input. CKW must be connected to a crystal controlled time base that runs within the specified frequency range of the Transmitter and Receiver.
FOTO	TTL In	Fiber Optic Transmitter Off. FOTO determines the function of two of the three PECL transmitter output pairs. If FOTO is LOW, the data encoded by the Transmitter will appear at the outputs continuously. If FOTO is HIGH, OUTA \pm and OUTB \pm are forced to their "logic zero" state (OUT+ = LOW and OUT- = HIGH), causing a fiber optic transmit module to extinguish its light output. OUTC is unaffected by the level on FOTO, and can be used as a loop-back signal source for board-level diagnostic testing.
OUT A \pm OUT B \pm OUT C \pm	PECL Out	Differential Serial Data Outputs. These PECL 100K outputs (+5V referenced) are capable of driving terminated transmission lines or commercial fiber optic transmitter modules. Unused pairs of outputs can be wired to V _{CC} to reduce power if the output is not required. OUTA \pm and OUTB \pm are controlled by the level on FOTO, and will remain at their "logical zero" states when FOTO is asserted. OUTC \pm is unaffected by the level on FOTO. (OUTA+ and OUTB+ are used as a differential test clock input while in Test mode, i.e., MODE=UNCONNECTED or forced to V _{CC} /2.)
MODE	3-Level In	Encoder Mode Select. The level on MODE determines the encoding method to be used. When wired to GND, MODE selects 8B/10B encoding. When wired to V _{CC} , data inputs bypass the encoder and the bit pattern on D _{a-j} goes directly to the shifter. When left floating (internal resistors hold the input at V _{CC} /2) the internal bit-clock generator is disabled and OUTA+/OUTB+ become the differential bit clock to be used for factory test. In typical applications MODE is wired to V _{CC} or GND.
BISTEN	TTL In	Built-In Self-Test Enable. When BISTEN is LOW and EN \bar{A} and ENN are HIGH, the transmitter sends an alternating 1-0 pattern (D10.2 or D21.5). When either EN \bar{A} or ENN is set LOW and BISTEN is LOW, the transmitter begins a repeating test sequence that allows the Transmitter and Receiver to work together to test the function of the entire link. In normal use this input is held HIGH or wired to V _{CC} . The BIST generator is a free-running pattern generator that need not be initialized, but if required, the BIST sequence can be initialized by momentarily asserting SVS while BISTEN is LOW. BISTEN has the same timing as D ₀₋₇ .
RP	TTL Out	Read Pulse. RP is a 60% LOW duty-cycle byte-rate pulse train suitable for the read pulse in CY7C42X FIFOs. The frequency on RP is the same as CKW when enabled by EN \bar{A} , and duty cycle is independent of the CKW duty cycle. Pulse widths are set by logic internal to the transmitter. In BIST mode, RP will remain HIGH for all but the last byte of a test loop. RP will pulse LOW one byte time per BIST loop.
V _{CCN}		Power for output drivers.
V _{CCQ}		Power for internal circuitry.
GND		Ground.

CY7B923 HOTLink Transmitter Block Diagram Description

Input Register

The Input register holds the data to be processed by the HOTLink transmitter and allows the input timing to be made consistent with standard FIFOs. The Input register is clocked by CKW and loaded with information on the D₀₋₇, SC/D, and SVS pins. Two enable inputs (EN_A and EN_N) allow the user to choose when data is loaded in the register. Asserting EN_A (Enable, active LOW) causes the inputs to be loaded in the register on the rising edge of CKW. If EN_N (Enable Next, active LOW) is asserted when CKW rises, the data present on the inputs on the next rising edge of CKW will be loaded into the Input register. If neither EN_A nor EN_N are asserted LOW on the rising edge of CKW, then a SYNC (K28.5) character is sent. These two inputs allow proper timing and function for compatibility with either asynchronous FIFOs or clocked FIFOs without external logic, as shown in Figure 5.

In BIST mode, the Input register becomes the signature pattern generator by logically converting the parallel Input register into a Linear Feedback Shift Register (LFSR). When enabled, this LFSR will generate a 511-byte sequence that includes all Data and Special Character codes, including the explicit violation symbols. This pattern provides a predictable but pseudo-random sequence that can be matched to an identical LFSR in the Receiver.

Encoder

The Encoder transforms the input data held by the Input register into a form more suitable for transmission on a serial interface link. The code used is specified by ANSI X3.230 (Fibre Channel) and the IBM ESCON channel (code tables are at the end of this datasheet). The eight D₀₋₇ data inputs are converted to either a Data symbol or a Special Character, depending upon the state of the SC/D input. If SC/D is HIGH, the data inputs represent a control code and are encoded using the Special Character code table. If SC/D is LOW, the data inputs are converted using the Data code table. If a byte time passes with the inputs disabled, the Encoder will output a Special Character Comma K28.5 (or SYNC) that will maintain link synchronization. SVS input forces the transmission of a specified Violation symbol to allow the user to check error handling system logic in the controller or for proprietary applications.

The 8B/10B coding function of the Encoder can be bypassed for systems that include an external coder or scrambler function as part of the controller. This bypass is controlled by setting the MODE select pin HIGH. When in bypass mode, D_{a-1} (note that bit order is specified in the Fibre Channel 8B/10B code) become the ten inputs to the Shifter, with D_a being the first bit to be shifted out.

Shifter

The Shifter accepts parallel data from the Encoder once each byte time and shifts it to the serial interface output buffers using a PLL multiplied bit clock that runs at ten (10) times the byte clock rate. Timing for the parallel transfer is controlled by the counter included in the Clock Generator and is not affected by signal levels or timing at the input pins.

OutA, OutB, OutC

The serial interface PECL output buffers (ECL100K referenced to +5v) are the drivers for the serial media. They are all connected to the Shifter and contain the same serial data. Two of the output pairs (OUTA_± and OUTB_±) are controllable by the FOTO input and can be disabled by the system controller to force a logical zero (i.e., "light off") at the outputs. The third output pair (OUTC_±) is

not affected by FOTO and will supply a continuous data stream suitable for loop-back testing of the subsystem.

OUTA_± and OUTB_± will respond to FOTO input changes within a few bit times. However, since FOTO is not synchronized with the transmitter data stream, the outputs will be forced off or turned on at arbitrary points in a transmitted byte. This function is intended to augment an external laser safety controller and as an aid for Receiver PLL testing.

In wire-based systems, control of the outputs may not be required, and FOTO can be strapped LOW. The three outputs are intended to add system and architectural flexibility by offering identical serial bit streams with separate interfaces for redundant connections or for multiple destinations. Unneeded outputs can be wired to V_{CC} to disable and power down the unused output circuitry.

Clock Generator

The clock generator is an embedded phase-locked loop (PLL) that takes a byte-rate reference clock (CKW) and multiplies it by ten (10) to create a bit rate clock for driving the serial shifter. The byte rate reference comes from CKW, the rising edge of which clocks data into the Input register. This clock must be a crystal referenced pulse stream that has a frequency between the minimum and maximum specified for the HOTLink Transmitter/Receiver pair. Signals controlled by this block form the bit clock and the timing signals that control internal data transfers between the Input register and the Shifter.

The read pulse (RP) is derived from the feedback counter used in the PLL multiplier. It is a byte-rate pulse stream with the proper phase and pulse widths to allow transfer of data from an asynchronous FIFO. Pulse width is independent of CKW duty cycle, since proper phase and duty cycle is maintained by the PLL. The RP pulse stream will insure correct data transfers between asynchronous FIFOs and the transmitter input latch with no external logic.

Test Logic

Test logic includes the initialization and control for the Built-In Self-Test (BIST) generator, the multiplexer for Test mode clock distribution, and control logic to properly select the data encoding. Test logic is discussed in more detail in the CY7B923 HOTLink Transmitter Operating Mode Description.

CY7B933 HOTLink Receiver Block Diagram Description

Serial Data Inputs

Two pairs of differential line receivers are the inputs for the serial data stream. INA_± or INB_± can be selected with the A/B input. INA_± is selected with A/B HIGH and INB_± is selected with A/B LOW. The threshold of A/B is compatible with the ECL 100K signals from PECL fiber optic interface modules. TTL logic elements can be used to select the A or B inputs by adding a resistor pull-up to the TTL driver connected to A/B. The differential threshold of INA_± and INB_± will accommodate wire interconnect with filtering losses or transmission line attenuation greater than 20 db (V_{DIFF} ≥ 50mv) or can be directly connected to fiber optic interface modules (any ECL logic family, not limited to ECL 100K). The common mode tolerance will accommodate a wide range of signal termination voltages. The highest HIGH input that can be tolerated is V_{IN} = V_{CC}, and the lowest LOW input that can be interpreted correctly is V_{IN} = GND + 2.0V.

PECL-TTL Translator

The function of the INB(INB+) input and the SI(INB-) input is defined by the connections on the SO output pin. If the PECL/TTL translator function is not required, the SO output is wired to

CY7B923/CY7B933 Electrical Characteristics Over the Operating Range^[1]

Parameter	Description	Test Conditions		Min.	Max.	Unit	
TTL OUTs, CY7B923: RP; CY7B933: Q₀₋₇, SC/D, RVS, RDV, CKR, SO							
V _{OHT}	Output HIGH Voltage	I _{OH} = - 2 mA		2.4		V	
V _{OLT}	Output LOW Voltage	I _{OL} = 4 mA			0.45	V	
I _{OST}	Output Short Circuit Current	V _{OUT} = 0V ^[2]		-15	-90	mA	
TTL INs, CY7B923: D₀₋₇, SC/D, SVS, ENA, ENN, CKW, FOTO, BISTEN; CY7B933: RE, REFCLK, BISTEN							
V _{IHT}	Input HIGH Voltage			Com'l & Mil	2.0	V _{CC}	V
				Mil (CKW and FOTO, only)	2.2	V _{CC}	V
V _{ILT}	Input LOW Voltage			- 0.5	0.8	V	
I _{IHT}	Input HIGH Current	V _{IN} = V _{CC}		- 10	+10	μA	
I _{ILT}	Input LOW Current	V _{IN} = 0.0V			- 500	μA	
Transmitter PECL-Compatible Output Pins: OUTA+, OUTA-, OUTB+, OUTB-, OUTC+, OUTC-							
V _{OHE}	Output HIGH Voltage (V _{CC} referenced)	Load = 50 Ω to V _{CC} - 2V	Com'l	V _{CC} -1.03	V _{CC} -0.83	V	
			Mil	V _{CC} -1.05	V _{CC} -0.83	V	
V _{OLE}	Output LOW Voltage (V _{CC} referenced)	Load = 50 Ω to V _{CC} - 2V	Com'l	V _{CC} -1.86	V _{CC} -1.62	V	
			Mil	V _{CC} -1.96	V _{CC} -1.62	V	
V _{ODIF}	Output Differential Voltage (OUT+) - (OUT-)	Load = 50 ohms to V _{CC} - 2V		0.6		V	
Receiver PECL-Compatible Input Pins: A/B, SI, INB							
V _{IHE}	Input HIGH Voltage			Com'l	V _{CC} -1.165	V _{CC}	V
				Mil	V _{CC} -1.14	V _{CC}	V
V _{ILE}	Input LOW Voltage			Com'l	2.0	V _{CC} -1.475	V
				Mil	2.0	V _{CC} -1.50	V
I _{IHE} ^[3]	Input HIGH Current	V _{IN} = V _{IHE} Max.			+500	μA	
I _{ILE} ^[3]	Input LOW Current	V _{IN} = V _{ILE} Min.		+0.5		μA	
Differential Line Receiver Input Pins: INA+, INA-, INB+, INB-							
V _{DIFF}	Input Differential Voltage (IN+) - (IN-)			50		mV	
V _{IHH}	Highest Input HIGH Voltage				V _{CC}	V	
V _{ILL}	Lowest Input LOW Voltage			2.0		V	
I _{IHH}	Input HIGH Current	V _{IN} = V _{IHH} Max.			750	μA	
I _{ILL} ^[4]	Input LOW Current	V _{IN} = V _{ILL} Min.		-200		μA	
Miscellaneous				Typ.	Max.		
I _{CCT} ^[5]	Transmitter Power Supply Current	Freq. = Max.	Com'l	65	85	mA	
			Mil	75	95	mA	
I _{CCR} ^[6]	Receiver Power Supply Current	Freq. = Max.	Com'l	120	155	mA	
			Mil	135	160	mA	

Notes:

- See the last page of this specification for Group A subgroup testing information.
- Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
- Applies to A/B only.
- Input currents are always positive at all voltages above V_{CC}/2.
- Maximum I_{CCT} is measured with V_{CC} = Max., one PECL output pair loaded with 50 ohms to V_{CC} - 2.0V, and other PECL outputs tied to V_{CC}. Typical I_{CCT} is measured with V_{CC} = 5.0V, T_A = 25°C, one output pair loaded with 50 ohms to V_{CC} - 2.0V, others tied to V_{CC}, BISTEN = LOW. I_{CCT} includes current into V_{CC0} (pin 9 and pin 22) only. Current into V_{CCN} is determined by PECL load currents, typically 30 mA with 50 ohms to V_{CC} - 2.0V. Each additional enabled PECL pair adds 5 mA to I_{CCT} and an additional load current to V_{CCN} as described. When calculating the contribution of PECL load currents to chip power dissipation, the output load current should be multiplied by 1V instead of V_{CC}.
- Maximum I_{CCR} is measured with V_{CC} = Max., RF = LOW, and outputs unloaded. Typical I_{CCR} is measured with V_{CC} = 5.0V, T_A = 25°C, RF = LOW, BISTEN = LOW, and outputs unloaded. I_{CCR} includes current into V_{CC0} (pins 21 and 24). Current into V_{CCN} (pin 9) is determined by the total TTL output buffer quiescent current plus the sum of all the load currents for each output pin. The total buffer quiescent current is 10mA max., and max. TTL load current for each output pin can be calculated as follows:

$$\frac{I_{CCN}}{TTLpin} = \left[\frac{0.95 + (V_{CCN} - 5) * 0.3}{R_L} + C_L * \left(\frac{V_{CCN}}{2} + 1.5 \right) * F_{pin} \right] * 1.1$$
 Where R_L=equivalent load resistance, C_L=capacitive load, and F_{pin}=frequency in MHz of data on pin. A derating factor of 1.1 has been included to account for worst process corner and temperature condition.

Receiver Switching Characteristics Over the Operating Range^[1]

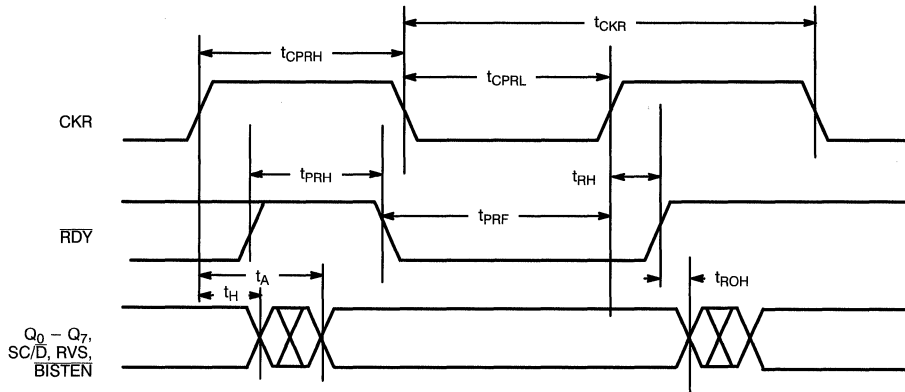
Parameter	Description	7B933		Unit
		Min.	Max.	
t _{CKR}	Read Clock Period (No Serial Data Input), REFCLK as Reference ^[15]	-1	+1	%
t _B	Bit Time ^[16]	3.03	6.25	ns
t _{CPRH}	Read Clock Pulse HIGH	5t _B -3		ns
t _{CPRL}	Read Clock Pulse LOW	5t _B -3		ns
t _{RH}	RDY Hold Time	t _B -3		ns
t _{PRF}	RDY Pulse Fall to CKR Rise	5t _B -3		ns
t _{PRH}	RDY Pulse Width HIGH	4t _B -3		ns
t _A	Data Access Time ^[17, 18]	2t _B -2	2t _B +4	ns
t _{ROH}	Data Hold Time ^[17, 18]	t _B -3		ns
t _H	Data Hold Time from CKR Rise ^[17, 18]	2t _B -3		ns
t _{CKX}	REFCLK Clock Period Referenced to CKW of Transmitter ^[19]	-0.1	+0.1	%
t _{CPXH}	REFCLK Clock Pulse HIGH	6.5		ns
t _{CPXL}	REFCLK Clock Pulse LOW	6.5		ns
t _{DS}	Propagation Delay SI to SO (note PECL and TTL thresholds) ^[20]		20	ns
t _{SA}	Static Alignment ^[7, 21]		100	ps
t _{EFW}	Error Free Window ^[7, 22]	0.9t _B		

Notes:

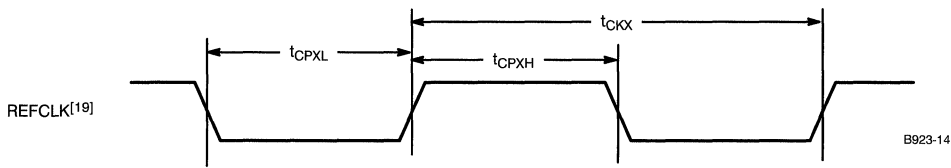
15. The period of t_{CKR} will match the period of the transmitter CKW when the receiver is receiving serial data. When data is interrupted, CKR may drift to one of the range limits above.
16. Receiver t_B is calculated as t_{CKR}/10 if no data is being received, or t_{CKW}/10 if data is being received. See note 9.
17. Data includes Q₀₋₇, SC/D, and RVS.
18. t_A, t_{ROH}, and t_H specifications are only valid if all outputs (CKR, RDY, Q₀₋₇, SC/D, and RVS) are loaded with similar DC and AC loads.
19. REFCLK has no phase or frequency relationship with CKR and only acts as a centering reference to reduce clock synchronization time.

REFCLK must be within 0.1% of the transmitter CKW frequency, necessitating a ±500-PPM crystal.

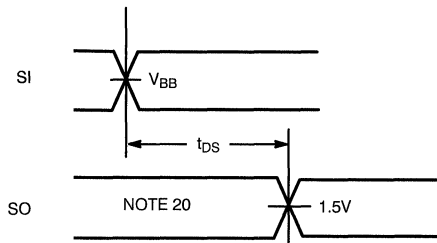
20. The PECL switching threshold is the midpoint between the PECL-V_{OH} and V_{OL} specification (approximately V_{CC} - 1.35V). The TTL switching threshold is 1.5V.
21. Static alignment is a measure of the alignment of the Receiver sampling point to the center of a bit. Static alignment is measured by sliding one bit edge in 3,000 nominal transitions until a byte error occurs.
22. Error Free Window is a measure of the time window between bit centers where a transition may occur without causing a bit sampling error. EFW is measured over the operating range, input jitter < 50% Dj.

Switching Waveforms for the CY7B933 HOTLink Receiver


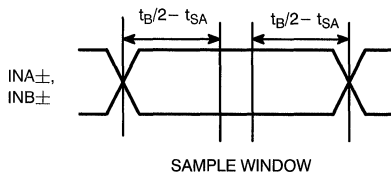
B923-13



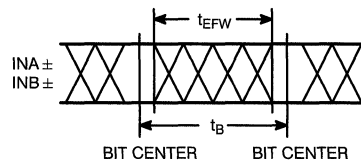
B923-14



B923-15

Static Alignment


B923-16

Error-Free Window


B923-17

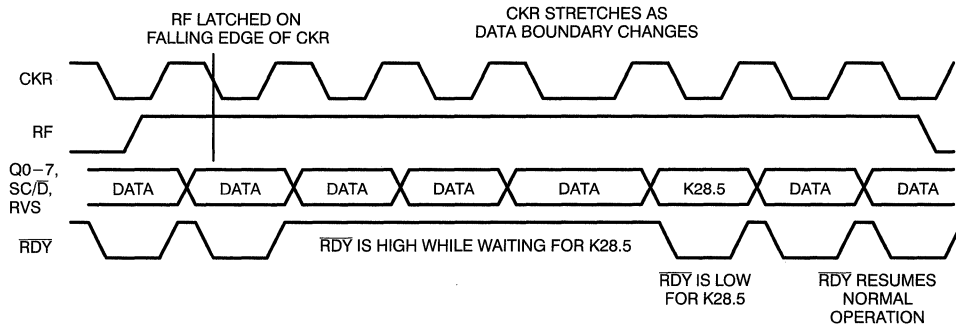


Figure 4. CY7B933 Framing Operation in Encoded Mode

B923-20

When the RF pin is asserted HIGH, $\overline{\text{RDY}}$ leaves its normal mode of operation and is asserted HIGH while the framer searches the data stream for a K28.5 character. After the framer has synchronized to a K28.5 character, the Receiver will assert the $\overline{\text{RDY}}$ pin LOW when the K28.5 character is present at the parallel output. The $\overline{\text{RDY}}$ pin will then resume its normal operation as dictated by the MODE and BISTEN pins.

The normal operation of the $\overline{\text{RDY}}$ pin in encoded mode is to signal when parallel data is present at the output pins by pulsing LOW with a 60% LOW/40% HIGH duty cycle. $\overline{\text{RDY}}$ does not pulse LOW in a field of K28.5 characters; however, $\overline{\text{RDY}}$ does pulse LOW for the last K28.5 character in the field or for any single K28.5. In unencoded mode, the normal operation of the $\overline{\text{RDY}}$ pin is to signal when any K28.5 is at the parallel output pins.

The Transmitter and Receiver parallel interface timing and functionality can be made to match the timing and functionality of either an asynchronous FIFO or a clocked FIFO by appropriately connecting signals (See Figure 5). Proper operation of the FIFO interface depends upon various FIFO-specific access and response specifications.

The HOTLink Transmitter and Receiver serial interface provides a seamless interface to various types of media. A minimal number of external components are needed to properly terminate transmission lines and provide PECL loads. For proper power supply decoupling, a single 0.01 μF for each device is all that is required to bypass the V_{CC} and GND pins. Figure 6 illustrates a HOTLink Transmitter and Receiver interface to fiber optic and copper media. More information on interfacing HOTLink to various media can be found in the *HOTLink Design Considerations* application note.

CY7B923 HOTLink Transmitter Operating Mode Description

In normal operation, the Transmitter can operate in either of two modes. The Encoded mode allows a user to send and receive eight (8) bit data and control information without first converting it to transmission characters. The Bypass mode is used for systems in which the encoding and decoding is performed in an external protocol controller.

In either mode, data is loaded into the Input register of the Transmitter on the rising edge of CKW. The input timing and functional response of the Transmitter input can be made to match the timing

and functionality of either an asynchronous FIFO or a clocked FIFO by an appropriate connection of input signals (See Figure 5). Proper operation of the FIFO interface depends upon various FIFO-specific access and response specifications.

Encoded Mode Operation

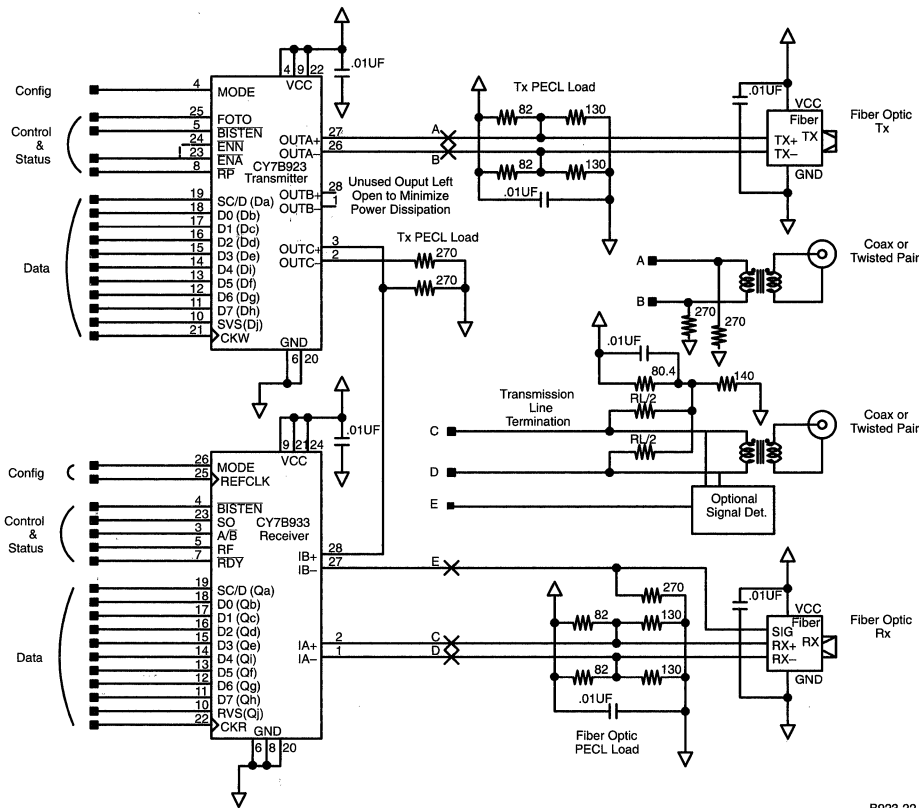
In Encoded mode the input data is interpreted as eight bits of data ($D_0 - D_7$), a context control bit (SC/D), and a system diagnostic input bit (SVS). If the context of the data is to be normal message data, the SC/D input should be LOW, and the data should be encoded using the valid data character set described in the Valid Data Characters section of this datasheet. If the context of the data is to be control or protocol information, the SC/D input will be HIGH, and the data will be encoded using the valid special character set described in the Valid Special Character Codes and Sequences section. Special characters include all protocol characters necessary to encode packets for Fibre Channel, ESCON, proprietary systems, and diagnostic purposes.

The diagnostic characters and sequences available as Special Characters include those for Fibre Channel link testing, as well as codes to be used for testing system response to link errors and timing. A Violation symbol can be explicitly sent as part of a user data packet (i.e., send C0.7; $D_{7-0} = 111\ 00000$ and $\text{SC}/\overline{\text{D}} = 1$), or it can be sent in response to an external system using the SVS input. This will allow system diagnostic logic to evaluate the errors in an unambiguous manner, and will not require any modification to the transmission interface to force transmission errors for testing purposes.

Bypass Mode Operation

In Bypass mode the input data is interpreted as ten (10) bits (D_{b-h}), SC/D (D_a), and SVS (D_j) of pre-encoded transmission data to be serialized and sent over the link. This data can use any encoding method suitable to the designer. The only restrictions upon the data encoding method is that it contain suitable transition density for the Receiver PLL data synchronizer (one per 10 bit byte), and that it be compatible with the transmission media.

Data loaded into the Input register on the rising edge of CKW will be loaded into the Shifter on the subsequent rising edges of CKW. It will then be shifted to the outputs one bit at a time using the internal clock generated by the clock generator. The first bit of the transmission character (D_a) will appear at the output ($\text{OUTA}\pm$, $\text{OUTB}\pm$, and $\text{OUTC}\pm$) after the next CKW edge.


Figure 6. HOTLink Connection Diagram

B923-22

Deterministic Jitter (D_j) < 35 ps (peak-peak). Typically measured while sending a continuous K28.5 (C5.0).

Random Jitter (R_j) < 175 ps (peak-peak). Typically measured while sending a continuous K28.7 (C7.0).

Transmitter Test Mode Description

The CY7B923 Transmitter offers two types of test mode operation, BIST mode and Test mode. In a normal system application, the Built-In Self-Test (BIST) mode can be used to check the functionality of the Transmitter, the Receiver, and the link connecting them. This mode is available with minimal impact on user system logic, and can be used as part of the normal system diagnostics. Typical connections and timing are shown in Figure 7.

BIST Mode

BIST mode functions as follows:

1. Set $\overline{\text{BISTEN}}$ LOW to begin test pattern generation. Transmitter begins sending bit rate ...1010...
2. Set either $\overline{\text{ENA}}$ or $\overline{\text{ENN}}$ LOW to begin test pattern sequence generation (use of the Enable pin not being used for normal FIFO or system interface can minimize logic delays between the controller and transmitter).

3. Allow the Transmitter to run through several BIST loops or until the Receiver test is complete. $\overline{\text{RP}}$ will pulse LOW once per BIST loop, and can be used by an external counter to monitor the number of test pattern loops.

4. When testing is completed, set $\overline{\text{BISTEN}}$ HIGH and $\overline{\text{ENA}}$ and $\overline{\text{ENN}}$ HIGH and resume normal function.

Note: It may be advisable to send violation characters to test the RVS output in the Receiver. This can be done by explicitly sending a violation with the SVS input, or allowing the transmitter BIST loop to run while the Receiver runs in normal mode. The BIST loop includes deliberate violation symbols and will adequately test the RVS function.

BIST mode is intended to check the entire function of the Transmitter (except the Transmitter input pins and the bypass function in the Encoder), the serial link, and the Receiver. It augments normal factory ATE testing and provides the designer with a rigorous test mechanism to check the link transmission system without requiring any significant system overhead.

While in Bypass mode, the BIST logic will function in the same way as in the Encoded mode. $\text{MODE} = \text{HIGH}$ and $\overline{\text{BISTEN}} = \text{LOW}$ causes the Transmitter to switch to Encoded mode and begin sending the BIST pattern, as if $\text{MODE} = \text{LOW}$. When $\overline{\text{BISTEN}}$ returns

initialized to match an ATE test pattern using the following technique:

1. With the MODE pin either HIGH or LOW, stop CKW and bit-clock.
2. Force the MODE pin to MID (open or $V_{CC}/2$) while the clocks are stopped.
3. Start the bit-clock and let it run for at least 2 cycles.
4. Start the CKW clock at the bit-clock/10 rate.

Test mode is intended to allow logical, DC, and AC testing of the Transmitter without requiring that the tester check output data patterns at the bit rate, or accommodate the PLL lock, tracking, and frequency range characteristics that are required when the HOTLink part operates in its normal mode. To use OutA+/OutB+ as the test clock input, the FOTO input is held HIGH while in Test mode. This forces the two outputs to go to an “PECL LOW,” which can be ignored while the test system creates a differential input signal at some higher voltage.

CY7B933 HOTLink Receiver Operating Mode Description

In normal user operation, the Receiver can operate in either of two modes. The Encoded mode allows a user system to send and receive 8-bit data and control information without first converting it to transmission characters. The Bypass mode is used for systems in which the encoding and decoding is performed by an external protocol controller.

In either mode, serial data is received at one of the differential line receiver inputs and routed to the Shifter and the Clock Synchronization. The PLL in the Clock Synchronizer aligns the internally generated bit rate clock with the incoming data stream and clocks the data into the shifter. At the end of a byte time (ten bit times), the data accumulated in the shifter is transferred to the Decode register.

To properly align the incoming bit stream to the intended byte boundaries, the bit counter in the Clock Synchronizer must be initialized. The Framing logic block checks the incoming bit stream for the unique pattern that defines the byte boundaries. This combinatorial logic filter looks for the X3.230 symbol defined as “Special Character Comma” (K28.5). Once K28.5 is found, the free running bit counter in the Clock Synchronizer block is synchronously reset to its initial state, thus “framing” the data to the correct byte boundaries.

Since noise-induced errors can cause the incoming data to be corrupted, and since many combinations of error and legal data can create an alias K28.5, an option is included to disable resynchronization of the bit counter. The Framing will be inhibited when the RF input is held LOW. When RF rises, \overline{RDY} will be inhibited until a K28.5 has been detected, and \overline{RDY} will resume its normal function. Data will continue to flow through the Receiver while \overline{RDY} is inhibited.

Encoded Mode Operation

In Encoded mode the serial input data is decoded into eight bits of data ($Q_0 - Q_7$), a context control bit (SC/\overline{D}), and a system diagnostic output bit (RVS). If the pattern in the Decode register is found in the Valid Data Characters table, the context of the data is decoded as normal message data and the SC/\overline{D} output will be LOW. If the incoming bit pattern is found in the Valid Special Character Codes and Sequences table, it is interpreted as “control” or “protocol information,” and the SC/\overline{D} output will be HIGH. Special characters include all protocol characters defined for use in packets for Fibre Channel, ESCON, and other proprietary and diagnostic purposes.

The Violation symbol that can be explicitly sent as part of a user data packet (i.e., Transmitter sending C0.7; $D_{7-0} = 111\ 00000$ and $SC/\overline{D} = 1$; or SVS = 1) will be decoded and indicated in exactly the same way as a noise-induced error in the transmission link. This function will allow system diagnostics to evaluate the error in an unambiguous manner, and will not require any modification to the receiver data interface for error-testing purposes.

Bypass Mode Operation

In Bypass mode the serial input data is not decoded, and is transferred directly from the Decode register to the Output register's 10 bits ($Q_{(a-j)}$). It is assumed that the data has been pre-encoded prior to transmission, and will be decoded in subsequent logic external to HOTLink. This data can use any encoding method suitable to the designer. The only restrictions upon the data encoding method is that it contain suitable transition density for the Receiver PLL data synchronizer (one per 10 bit byte) and that it be compatible with the transmission media.

The framer function in Bypass mode is identical to Encoded mode, so a K28.5 pattern can still be used to re-frame the serial bit stream.

Parallel Output Function

The 10 outputs (Q_{0-7} , SC/\overline{D} , and RVS) all transition simultaneously, and are aligned with \overline{RDY} and CKR with timing allowances to interface directly with either an asynchronous FIFO or a clocked FIFO. Typical FIFO connections are shown in Figure 5.

Data outputs can be clocked into the system using either the rising or falling edge of CKR, or the rising or falling edge of \overline{RDY} . If CKR is used, \overline{RDY} can be used as an enable for the receiving logic. A LOW pulse on \overline{RDY} shows that new data has been received and is ready to be delivered. The signal on \overline{RDY} is a 60%–LOW duty cycle byte-rate pulse train suitable for the write pulse in asynchronous FIFOs such as the CY7C42X, or the enable write input on Clocked FIFOs such as the CY7C44X. HIGH on \overline{RDY} shows that the received data appearing at the outputs is the null character (normally inserted by the transmitter as a pad between data inputs) and should be ignored.

When the Transmitter is disabled it will continuously send pad characters (K28.5). To assure that the receive FIFO will not be overfilled with these dummy bytes, the \overline{RDY} pulse output is inhibited during fill strings. Data at the Q_{0-7} outputs will reflect the correct received data, but will not appear to change, since a string of K28.5s all are decoded as $Q_{7-0} = 000\ 00101$ and $SC/\overline{D} = 1$ (C5.0). When new data appears (not K28.5), the \overline{RDY} output will resume normal function. The “last” K28.5 will be accompanied by a normal \overline{RDY} pulse.

Fill characters are defined as any K28.5 followed by another K28.5. All fill characters will not cause \overline{RDY} to pulse. Any K28.5 followed by any other character (including violation or illegal characters) will be interpreted as usable data and will cause \overline{RDY} to pulse.

As noted above, \overline{RDY} can also be used as an indication of correct framing of received data. While the Receiver is awaiting receipt of a K28.5 with RF HIGH, the \overline{RDY} outputs will be inhibited. When \overline{RDY} resumes, the received data will be properly framed and will be decoded correctly. In Bypass mode with RF HIGH, \overline{RDY} will pulse once for each K28.5 received. For more information on the \overline{RDY} pin, consult the “HOTLink CY7B933 \overline{RDY} Pin Description” application note.

range characteristics that are required when the part operates in its normal mode.

X3.230 Codes and Notation Conventions

Information to be transmitted over a serial link is encoded eight bits at a time into a 10-bit Transmission Character and then sent serially, bit by bit. Information received over a serial link is collected ten bits at a time, and those Transmission Characters that are used for data (Data Characters) are decoded into the correct eight-bit codes. The 10-bit Transmission Code supports all 256 8-bit combinations. Some of the remaining Transmission Characters (Special Characters) are used for functions other than data transmission.

The primary rationale for use of a Transmission Code is to improve the transmission characteristics of a serial link. The encoding defined by the Transmission Code ensures that sufficient transitions are present in the serial bit stream to make clock recovery possible at the Receiver. Such encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, some Special Characters of the Transmission Code selected by Fibre Channel Standard consist of a distinct and easily recognizable bit pattern (the Special Character Comma) that assists a Receiver in achieving word alignment on the incoming bit stream.

Notation Conventions

The documentation for the 8B/10B Transmission Code uses letter notation for the bits in an 8-bit byte. Fibre Channel Standard notation uses a bit notation of A, B, C, D, E, F, G, H for the 8-bit byte for the raw 8-bit data, and the letters a, b, c, d, e, i, f, g, h, j for encoded 10-bit data. There is a correspondence between bit A and bit a, B and b, C and c, D and d, E and e, F and f, G and g, and H and h. Bits i and j are derived, respectively, from (A,B,C,D,E) and (F,G,H).

The bit labeled A in the description of the 8B/10B Transmission Code corresponds to bit 0 in the numbering scheme of the FC-2 specification, B corresponds to bit 1, as shown below.

FC-2 bit designation—	7	6	5	4	3	2	1	0
HOTLink D/Q designation—	7	6	5	4	3	2	1	0
8B/10B bit designation—	H	G	F	E	D	C	B	A

To clarify this correspondence, the following example shows the conversion from an FC-2 Valid Data Byte to a Transmission Character (using 8B/10B Transmission Code notation)

```

FC-2 45
      Bits: 7654 3210
            0100 0101
  
```

Converted to 8B/10B notation (note carefully that the order of bits is reversed):

```

Data Byte Name  D5.2
      Bits: ABCDE FGH
            10100 010
  
```

Translated to a transmission Character in the 8B/10B Transmission Code:

```

Bits: abcdei fghj
      101001 0101
  
```

Each valid Transmission Character of the 8B/10B Transmission Code has been given a name using the following convention: *cxxy*, where *c* is used to show whether the Transmission Character is a Data Character (*c* is set to D, and the SC/D pin is LOW) or a Special Character (*c* is set to K, and the SC/D pin is HIGH). When *c* is set to D, *xx* is the decimal value of the binary number composed of the bits E, D, C, B, and A in that order, and the *y* is the decimal value of the binary number composed of the bits H, G, and F in that

order. When *c* is set to K, *xx* and *y* are derived by comparing the encoded bit patterns of the Special Character to those patterns derived from encoded Valid Data bytes and selecting the names of the patterns most similar to the encoded bit patterns of the Special Character.

Under the above conventions, the Transmission Character used for the examples above, is referred to by the name D5.2. The Special Character K29.7 is so named because the first six bits (abcdei) of this character make up a bit pattern similar to that resulting from the encoding of the unencoded 11101 pattern (29), and because the second four bits (fghj) make up a bit pattern similar to that resulting from the encoding of the unencoded 111 pattern (7).

Note: This definition of the 10-bit Transmission Code is based on (and is in basic agreement with) the following references, which describe the same 10-bit transmission code.

A.X. Widmer and P.A. Franaszek. "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code" *IBM Journal of Research and Development*, 27, No. 5: 440–451 (September, 1983).

U.S. Patent 4,488,739. Peter A. Franaszek and Albert X. Widmer. "Byte-Oriented DC Balanced (0.4) 8B/10B Partitioned Block Transmission Code" (December 4, 1984).

Fibre Channel Physical and Signaling Interface (dpANSI X3.230–199X ANSI FC–PH Standard).

IBM Enterprise Systems Architecture/390 ESCON I/O Interface (document number SA22–7202).

8B/10B Transmission Code

The following information describes how the tables shall be used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). It also specifies the ordering rules to be followed when transmitting the bits within a character and the characters within the higher-level constructs specified by the standard.

Transmission Order

Within the definition of the 8B/10B Transmission Code, the bit positions of the Transmission Characters are labeled a, b, c, d, e, i, f, g, h, j. Bit "a" shall be transmitted first followed by bits b, c, d, e, i, f, g, h, and j in that order. (Note that bit i shall be transmitted between bit e and bit f, rather than in alphabetical order.)

Valid and Invalid Transmission Characters

The following tables define the valid Data Characters and valid Special Characters (K characters), respectively. The tables are used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). In the tables, each Valid-Data-byte or Special-Character-code entry has two columns that represent two (not necessarily different) Transmission Characters. The two columns correspond to the current value of the running disparity ("Current RD—" or "Current RD+"). Running disparity is a binary parameter with either the value negative (–) or the value positive (+).

After powering on, the Transmitter may assume either a positive or negative value for its initial running disparity. Upon transmission of any Transmission Character, the transmitter will select the proper version of the Transmission Character based on the current running disparity value, and the Transmitter shall calculate a new value for its running disparity based on the contents of the transmitted character. Special Character codes C1.7 and C2.7 can be used to force the transmission of a specific Special Character with a specific running disparity as required for some special sequences in X3.230.



Valid Data Characters (SC/D = LOW)

Data Byte Name	Bits		Current RD-		Current RD+	
	HGF	EDCBA	abcdei	fg hj	abcdei	fg hj
D0.0	000	00000	100111	0100	011000	1011
D1.0	000	00001	011101	0100	100010	1011
D2.0	000	00010	101101	0100	010010	1011
D3.0	000	00011	110001	1011	110001	0100
D4.0	000	00100	110101	0100	001010	1011
D5.0	000	00101	101001	1011	101001	0100
D6.0	000	00110	011001	1011	011001	0100
D7.0	000	00111	111000	1011	000111	0100
D8.0	000	01000	111001	0100	000110	1011
D9.0	000	01001	100101	1011	100101	0100
D10.0	000	01010	010101	1011	010101	0100
D11.0	000	01011	110100	1011	110100	0100
D12.0	000	01100	001101	1011	001101	0100
D13.0	000	01101	101100	1011	101100	0100
D14.0	000	01110	011100	1011	011100	0100
D15.0	000	01111	010111	0100	101000	1011
D16.0	000	10000	011011	0100	100100	1011
D17.0	000	10001	100011	1011	100011	0100
D18.0	000	10010	010011	1011	010011	0100
D19.0	000	10011	110010	1011	110010	0100
D20.0	000	10100	001011	1011	001011	0100
D21.0	000	10101	101010	1011	101010	0100
D22.0	000	10110	011010	1011	011010	0100
D23.0	000	10111	111010	0100	000101	1011
D24.0	000	11000	110011	0100	001100	1011
D25.0	000	11001	100110	1011	100110	0100
D26.0	000	11010	010110	1011	010110	0100
D27.0	000	11011	110110	0100	001001	1011
D28.0	000	11100	001110	1011	001110	0100
D29.0	000	11101	101110	0100	010001	1011
D30.0	000	11110	011110	0100	100001	1011
D31.0	000	11111	101011	0100	010100	1011

Data Byte Name	Bits		Current RD-		Current RD+	
	HGF	EDCBA	abcdei	fg hj	abcdei	fg hj
D0.1	001	00000	100111	1001	011000	1001
D1.1	001	00001	011101	1001	100010	1001
D2.1	001	00010	101101	1001	010010	1001
D3.1	001	00011	110001	1001	110001	1001
D4.1	001	00100	110101	1001	001010	1001
D5.1	001	00101	101001	1001	101001	1001
D6.1	001	00110	011001	1001	011001	1001
D7.1	001	00111	111000	1001	000111	1001
D8.1	001	01000	111001	1001	000110	1001
D9.1	001	01001	100101	1001	100101	1001
D10.1	001	01010	010101	1001	010101	1001
D11.1	001	01011	110100	1001	110100	1001
D12.1	001	01100	001101	1001	001101	1001
D13.1	001	01101	101100	1001	101100	1001
D14.1	001	01110	011100	1001	011100	1001
D15.1	001	01111	010111	1001	101000	1001
D16.1	001	10000	011011	1001	100100	1001
D17.1	001	10001	100011	1001	100011	1001
D18.1	001	10010	010011	1001	010011	1001
D19.1	001	10011	110010	1001	110010	1001
D20.1	001	10100	001011	1001	001011	1001
D21.1	001	10101	101010	1001	101010	1001
D22.1	001	10110	011010	1001	011010	1001
D23.1	001	10111	111010	1001	000101	1001
D24.1	001	11000	110011	1001	001100	1001
D25.1	001	11001	100110	1001	100110	1001
D26.1	001	11010	010110	1001	010110	1001
D27.1	001	11011	110110	1001	001001	1001
D28.1	001	11100	001110	1001	001110	1001
D29.1	001	11101	101110	1001	010001	1001
D30.1	001	11110	011110	1001	100001	1001
D31.1	001	11111	101011	1001	010100	1001



Valid Data Characters (SC/D = LOW) (continued)

Data Byte Name	Bits		Current RD-		Current RD+		Data Byte Name	Bits		Current RD-		Current RD+	
	HGF	EDCBA	abcdei	fg hj	abcdei	fg hj		HGF	EDCBA	abcdei	fg hj	abcdei	fg hj
D0.4	100	00000	100111	0010	011000	1101	D0.5	101	00000	100111	1010	011000	1010
D1.4	100	00001	011101	0010	100010	1101	D1.5	101	00001	011101	1010	100010	1010
D2.4	100	00010	101101	0010	010010	1101	D2.5	101	00010	101101	1010	010010	1010
D3.4	100	00011	110001	1101	110001	0010	D3.5	101	00011	110001	1010	110001	1010
D4.4	100	00100	110101	0010	001010	1101	D4.5	101	00100	110101	1010	001010	1010
D5.4	100	00101	101001	1101	101001	0010	D5.5	101	00101	101001	1010	101001	1010
D6.4	100	00110	011001	1101	011001	0010	D6.5	101	00110	011001	1010	011001	1010
D7.4	100	00111	111000	1101	000111	0010	D7.5	101	00111	111000	1010	000111	1010
D8.4	100	01000	111001	0010	000110	1101	D8.5	101	01000	111001	1010	000110	1010
D9.4	100	01001	100101	1101	100101	0010	D9.5	101	01001	100101	1010	100101	1010
D10.4	100	01010	010101	1101	010101	0010	D10.5	101	01010	010101	1010	010101	1010
D11.4	100	01011	110100	1101	110100	0010	D11.5	101	01011	110100	1010	110100	1010
D12.4	100	01100	001101	1101	001101	0010	D12.5	101	01100	001101	1010	001101	1010
D13.4	100	01101	101100	1101	101100	0010	D13.5	101	01101	101100	1010	101100	1010
D14.4	100	01110	011100	1101	011100	0010	D14.5	101	01110	011100	1010	011100	1010
D15.4	100	01111	010111	0010	101000	1101	D15.5	101	01111	010111	1010	101000	1010
D16.4	100	10000	011011	0010	100100	1101	D16.5	101	10000	011011	1010	100100	1010
D17.4	100	10001	100011	1101	100011	0010	D17.5	101	10001	100011	1010	100011	1010
D18.4	100	10010	010011	1101	010011	0010	D18.5	101	10010	010011	1010	010011	1010
D19.4	100	10011	110010	1101	110010	0010	D19.5	101	10011	110010	1010	110010	1010
D20.4	100	10100	001011	1101	001011	0010	D20.5	101	10100	001011	1010	001011	1010
D21.4	100	10101	101010	1101	101010	0010	D21.5	101	10101	101010	1010	101010	1010
D22.4	100	10110	011010	1101	011010	0010	D22.5	101	10110	011010	1010	011010	1010
D23.4	100	10111	111010	0010	000101	1101	D23.5	101	10111	111010	1010	000101	1010
D24.4	100	11000	110011	0010	001100	1101	D24.5	101	11000	110011	1010	001100	1010
D25.4	100	11001	100110	1101	100110	0010	D25.5	101	11001	100110	1010	100110	1010
D26.4	100	11010	010110	1101	010110	0010	D26.5	101	11010	010110	1010	010110	1010
D27.4	100	11011	110110	0010	001001	1101	D27.5	101	11011	110110	1010	001001	1010
D28.4	100	11100	001110	1101	001110	0010	D28.5	101	11100	001110	1010	001110	1010
D29.4	100	11101	101110	0010	010001	1101	D29.5	101	11101	101110	1010	010001	1010
D30.4	100	11110	011110	0010	100001	1101	D30.5	101	11110	011110	1010	100001	1010
D31.4	100	11111	101011	0010	010100	1101	D31.5	101	11111	101011	1010	010100	1010

Valid Special Character Codes and Sequences (SC/D̄ = HIGH)^[23, 24]

S.C. Byte Name	S.C. Code Name		Bits		Current RD-		Current RD+				
			HGF	EDCBA	abcdei	fghj	abcdei	fghj			
K28.0	C0.0	(C00)	000	00000	001111	0100	110000	1011			
K28.1	C1.0	(C01)	000	00001	001111	1001	110000	0110			
K28.2	C2.0	(C02)	000	00010	001111	0101	110000	1010			
K28.3	C3.0	(C03)	000	00011	001111	0011	110000	1100			
K28.4	C4.0	(C04)	000	00100	001111	0010	110000	1101			
K28.5	C5.0	(C05)	000	00101	001111	1010	110000	0101			
K28.6	C6.0	(C06)	000	00110	001111	0110	110000	1001			
K28.7	C7.0	(C07)	000	00111	001111	1000	110000	0111			
K23.7	C8.0	(C08)	000	01000	111010	1000	000101	0111			
K27.7	C9.0	(C09)	000	01001	110110	1000	001001	0111			
K29.7	C10.0	(C0A)	000	01010	101110	1000	010001	0111			
K30.7	C11.0	(C0B)	000	01011	011110	1000	100001	0111			
Idle	C0.1	(C20)	001	00000	-K28.5+, D21.4, D21.5, D21.5, repeat ^[25]						
R_RDY	C1.1	(C21)	001	00001	-K28.5+, D21.4, D10.2, D10.2, repeat ^[26]						
EOF _{xx}	C2.1	(C22)	001	00010	-K28.5, Dn. xxx0 ^[27]		+K28.5, Dn. xxx1 ^[27]				
C-SOF	Follows K28.1 for ESCON Connect-SOF (Rx indication only)			C7.1	(C27)	001	00111	001111	1000	110000	0111
P-SOF	Follows K28.5 for ESCON Passive-SOF (Rx indication only)			C7.2	(C47)	010	00111	001111	1000	110000	0111
Exception	C0.7	(CE0)	111	00000	Code Rule Violation and SVS Tx Pattern		100111	1000 ^[28]	011000	0111 ^[28]	
-K28.5	C1.7	(CE1)	111	00001	001111	1010 ^[29]	001111	1010 ^[29]			
+K28.5	C2.7	(CE2)	111	00010	110000	0101 ^[30]	110000	0101 ^[30]			
Exception	C4.7	(CE4)	111	00100	Running Disparity Violation Pattern		110111	0101 ^[31]	001000	1010 ^[31]	

Notes:

23. All codes not shown are reserved.
24. Notation for Special Character Byte Name is consistent with Fibre Channel and ESCON naming conventions. Special Character Code Name is intended to describe binary information present on I/O pins. Common usage for the name can either be in the form used for describing Data patterns (i.e., C0.0 through C31.7), or in hex notation (i.e., Cnn where nn=the specified value between 00 and FF).
25. C0.1 = Transmit Negative K28.5 (-K28.5+) disregarding Current RD when input is held for only one byte time. If held longer, transmit-

ter begins sending the repeating transmit sequence -K28.5+, D21.4, D21.5, D21.5, (repeat all four bytes)... defined in X3.230 as the primitive signal "Idle word." This Special Character input must be held for four (4) byte times or multiples of four bytes or it will be truncated by the new data.

The receiver will never output this Special Character, since K28.5 is decoded as C5.0, C1.7, or C2.7, and the subsequent bytes are decoded as data.

**MILITARY SPECIFICATIONS
Group A Subgroup Testing**
DC Characteristics

Parameter	Subgroup
VOHT	1, 2, 3
VOLT	1, 2, 3
VOHE	1, 2
VOLE	1, 2, 3
VODIF	1, 2, 3
I _{OST}	1, 2, 3
V _{IHT}	1, 2, 3
V _{ILT}	1, 2, 3
V _{IHE}	1, 2, 3
V _{ILE}	1, 2, 3
I _{IHT}	1, 2, 3
I _{ILT}	1, 2, 3
I _{IHE}	1, 2, 3
I _{ILE}	1, 2, 3
I _{CC}	1, 2, 3
V _{DIFF}	1, 2, 3
V _{IHH}	1, 2, 3
V _{ILL}	1, 2, 3

Switching Characteristics

Parameter	Subgroup
t _{CKW}	9, 10, 11
t _B	9, 10, 11
t _{CPWH}	9, 10, 11
t _{CPWL}	9, 10, 11
t _{SD}	9, 10, 11
t _{HD}	9, 10, 11
t _{SENP}	9, 10, 11
t _{HENP}	9, 10, 11
t _{PDR}	9, 10, 11
t _{PPWH}	9, 10, 11
t _{PDF}	9, 10, 11
t _{RISE}	9, 10, 11
t _{FALL}	9, 10, 11
t _{CKR}	9, 10, 11
t _{CPRH}	9, 10, 11
t _{CPRL}	9, 10, 11
t _{RH}	9, 10, 11
t _{PRF}	9, 10, 11
t _{PRH}	9, 10, 11
t _A	9, 10, 11
t _{ROH}	9, 10, 11
t _{CKX}	9, 10, 11
t _{CPXH}	9, 10, 11
t _{CPXL}	9, 10, 11
t _{DS}	9, 10, 11

Document #: 38-00189-F

Pin Descriptions

Name	I/O	Description
RIN±	Differential In	Receive Input. This line receiver port connects the receive differential serial input data stream to the internal Receive PLL. This PLL will recover the embedd clock (RCLK±) and data (RSER±) information for one of two data rates depending on the state of the MODE pin. These inputs can receive very low amplitude signals and are compatible with all PECL signalling levels. If the RIN± inputs are not being used, connect RIN+ to V _{CC} and RIN- to V _{SS} .
ROUT±	ECL Out	Receive Output. These ECL 100K outputs (+5V referenced) represent the buffered version of the input data stream (RIN±). This output pair can be used for Receiver input data equalization in copper based systems, reducing the system impact of data dependent jitter. All PECL outputs can be powered down by connecting both outputs to V _{CC} or leaving them both unconnected.
RSER±	ECL Out	Recovered Serial Data. These ECL 100K outputs (+5V referenced) represent the recovered data from the input data stream (RIN±). This recovered data is aligned with the recovered clock (RCLK±) with a sampling window compatible with most data processing devices.
RCLK±	ECL Out	Recovered Clock. These ECL 100K outputs (+5V referenced) represent the recovered clock from the input data stream (RIN±). This recovered clock is used to sample the recovered data (RSER±) and has timing compatible with most data processing devices. If both the RSER± and the RCLK± are tied to V _{CC} or left unconnected, the entire Receive PLL will be powered down.
CD	TTL/ECL In	Carrier Detect. This input controls the recovery function of the Receive PLL and can be driven by the carrier detect output from optical modules or from external transition detection circuitry. When this input is at an ECL HIGH, the input data stream (RIN±) is recovered normally by the Receive PLL. When this input is at an ECL LOW, the Receive PLL no longer aligns to RIN±, but instead aligns with the REFCLK×8 frequency. Also, the Link Fault Indicator (LFI) will transition LOW, and the recovered data outputs (RSER) will remain LOW regardless of the signal level on the Receive data-stream inputs (RIN). When the CD input is at a TTL LOW, the internal transitions detection circuitry is disabled.
LFI	TTL Out	Link Fault Indicator. This output indicates the status of the input data stream (RIN±). It is controlled by three functions; the Carrier Detect (CD) input, the internal Transition Detector, and the Out of Lock (OOL) detector. The Transition Detector determines if RIN± contains enough transitions to be accurately recovered by the Receive PLL. The Out of Lock detector determines if RIN± is within the frequency range of the Receive PLL. When CD is HIGH and RIN± has sufficient transitions and is within the frequency range of the Receive PLL, the LFI output will be HIGH. If CD is at an ECL LOW or RIN± does not contain sufficient transitions or RIN± is outside the frequency range of the Receive PLL then the LFI output will be LOW. If CD is at a TTL LOW then the LFI output will only transition LOW when the frequency of RIN± is outside the range of the Receive PLL.
TSER±	Differential In	Transmit Serial Data. This line receiver port connects the transmit differential serial input data stream to the TOUT transmit buffers. Depending on the state of the LOOP pin, this input port can also be set up to supply the serial input data stream to the Receive PLL. These inputs can receive very low amplitude signals and are compatible with all PECL signalling levels. If the TSER± inputs are not being used, connect RIN+ to V _{CC} and RIN- to V _{SS} .
TOUT±	ECL Out	Transmit Output. These ECL 100K outputs (+5V referenced) represent the buffered version of the Transmit data stream (TSER±). This Transmit path is used to take weak input signals and rebuffer them to drive low impedance copper media.
REFCLK±	Diff/TTL In	Reference Clock. This input is the clock frequency reference for the clock and data recovery Receive PLL. REFCLK is multiplied internally by eight and sets the approximate center frequency for the internal Receive PLL to track the incoming bit stream. This input is also multiplied by eight by the frequency multiplier Transmit PLL to produce the bit rate Transmit Clock (TCLK±). REFCLK can be connected to either a differential PECL or single-ended TTL frequency source. When either REFCLK+ or REFCLK- is at a TTL LOW, the opposite REFCLK signal becomes a TTL level input.
TCLK±	ECL Out	Transmit Clock. These ECL 100K outputs (+5V referenced) provide the bit rate frequency source for external Transmit data processing devices. This output is synthesized by the Transmit PLL and is derived by multiplying the REFCLK frequency by eight. When this output is turned off, the entire Transmit PLL is powered down. All PECL outputs can be powered down by connecting both outputs to V _{CC} or leaving them both unconnected.
LOOP	TTL In	Loop Back Select. This input is used to select the input data stream source that the Receive PLL uses for clock and data recovery. When the LOOP input is HIGH, the Receive input data stream (RIN±) is used for clock and data recovery. When LOOP is LOW, the Transmit input data stream (TSER±) is used by the Receive PLL for clock and data recovery.

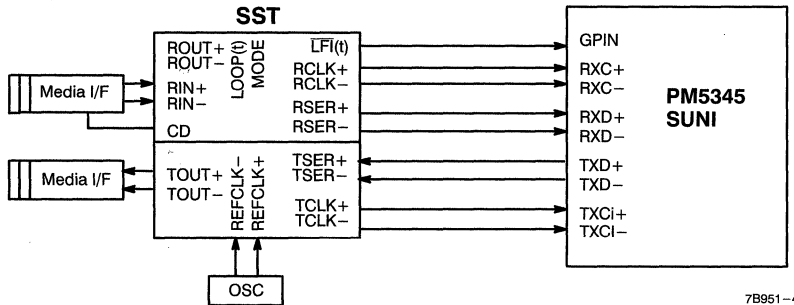


Figure 2. SST to PMC-Sierra PM5345 SUNI Connection Diagram

number of bit times that have passed without a data transition. A bit time is defined as the period of $RCLK\pm$. When 256 bit times have passed without a data transition on $RIN\pm$, \overline{LFI} will transition LOW. The receiver will assume that the serial data stream is invalid and, instead of allowing the $RCLK\pm$ frequency to wander in the absence of data, the PLL will lock to the $REFCLK \times 8$ frequency. This will insure that $RCLK\pm$ is as close to the correct link operating frequency as the $REFCLK$ accuracy. \overline{LFI} will be driven HIGH again and the receiver will recover clock and data from the incoming data stream when the transition detection circuitry determines that at least 64 transitions have been detected within 256 bit-times.

The Transition Detector can be turned off by pulling the CD input to a TTL LOW ($\leq 0.8V$). When CD is pulled to a TTL LOW the \overline{LFI} will only be driven LOW if the incoming data stream frequency is not within 1000 ppm of the $REFCLK \times 8$ frequency. \overline{LFI} LOW in this case will only indicate that the Receiver PLL is Out of Lock (OOL). When this pin is left unconnected, an internal pull-down resistor will pull this input to Ground.

Loop Back Testing

The TTL level \overline{LOOP} pin is used to perform loop-back testing. When \overline{LOOP} is asserted (held LOW) the Transmitter serial input ($TSER\pm$) is used by the Receiver PLL for clock and data recovery. This allows in-system testing to be performed on the entire device except for the differential Transmitter drivers ($TOUT\pm$) and the differential Receiver inputs ($RIN\pm$). For example, an ATM controller can present ATM cells to the input of the ATM cell processor and check to see that these same cells are received. When the \overline{LOOP} input is deasserted (held HIGH) the Receive PLL is once again connected to the Receiver serial inputs ($RIN\pm$).

The \overline{LOOP} feature can also be used in applications where clock and data recovery are to be performed from either of two data streams. In these systems the \overline{LOOP} pin is used to select whether the $TSER\pm$ or the $RIN\pm$ inputs are used by the Receive PLL for clock and data recovery.

Power Down Modes

There are several power-down features on the SST. Any of the differential output drivers can be powered down by either tying both outputs to V_{CC} or by simply leaving them unconnected where internal pull-up resistors will force these outputs to V_{CC} . This will save approximately 4 mA per output pair in addition to the associated output current. If the $TOUT\pm$ or $ROUT\pm$ out-

puts are tied to V_{CC} or left unconnected, the Transmit buffer or Receive buffer path respectively will be turned off. If the $TCLK\pm$ outputs are tied to V_{CC} or left unconnected, the entire Transmit PLL will be powered down.

By leaving both the $RCLK\pm$ and $RSER\pm$ outputs unconnected or tied to V_{CC} , the entire Receive PLL is turned off. Even though the Receive PLL may be turned off, the Link Fault Indicator (\overline{LFI}) will still reflect the state of the Carrier Detect (CD) input. This feature can be used for aggressive power management.

Applications

The SST can be used in SONET/SDH and ATM applications. The operating frequency of the 7B951 is centered around the SONET/SDH STS-1 rate of 51.84 MHz and the SONET/SDH STS-3/STM-1 rate of 155.52 MHz. This device can also be used in data mover and Local Area Network (LAN) applications that operate at these frequencies.

The SST can provide clock and data recovery as well as output buffering for physical layer protocol engines such as the SONET/SDH and ATM processing application shown in Figures 1 and 2 and SONET/SDH overhead termination and 155Mb/s serial to parallel conversion as shown in Figure 3.

Figure 1 shows the SST in an ATM system that uses the PMC-Sierra SUNI device. The SST will recover clock and data from the input serial data stream and pass it to the PM5345 SUNI. The SUNI device will perform serial to parallel conversion, SONET/SDH overhead processing and ATM cell processing and then pass ATM cells to an ATM packet reassembly engine. On the Transmit side, a segmentation engine will divide long packets of data such as Ethernet packets into 53 byte cells and pass them to the SUNI. The SUNI device will then perform ATM cell processing, such as header generation, SONET/SDH overhead processing and parallel to serial conversion. This serial data will then be passed to the SST which will buffer this data stream and pass it along to the transmission media.

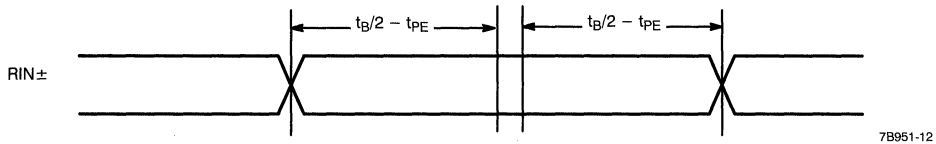
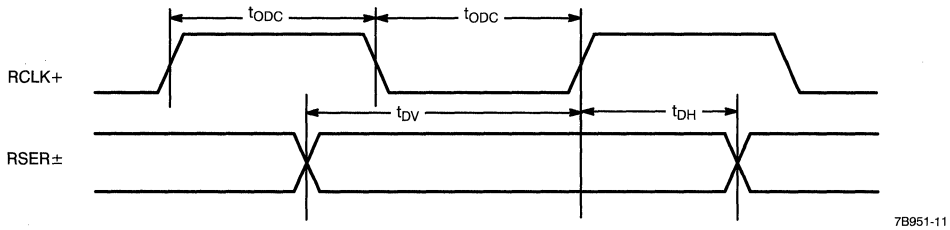
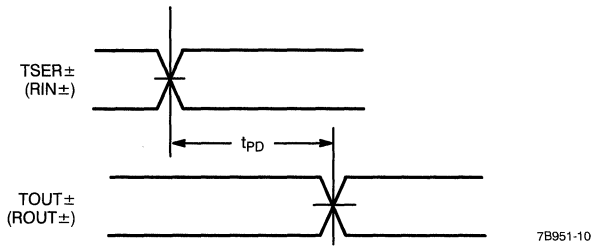
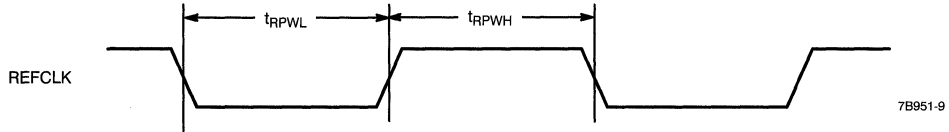
The SST provides the necessary clock and data recovery function to the PM5345. These differential PECL clock and data signals interface directly with the $RXD\pm$ and $RXC\pm$ inputs of the SUNI device as show in Figure 2. In addition, the SST provides transmit data output buffering for direct drive of cable transmission media. Lastly, the SST provides a bit rate reference clock to the SUNI transmitter by multiplying a local clock by eight allowing an inexpensive crystal oscillator to be used for the local reference.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit	
TTL Compatible Input Pins (LOOP, REFCLK+, REFCLK-)						
V _{IHT}	Input HIGH Voltage		2.0	V _{CC}	V	
V _{ILT}	Input LOW Voltage		-0.5	0.8	V	
I _{IHT}	Input HIGH Current	REFCLK	V _{IN} =V _{CC}	+0.5	+200	μA
		LOOP	V _{IN} =V _{CC}	-10	+10	μA
I _{ILT}	Input LOW Current	REFCLK	V _{IN} =0.0V	-50	+50	μA
		LOOP	V _{IN} =0.0V	-500		μA
TTL Compatible Output Pins (LF1)						
V _{OHT}	Output HIGH Voltage	I _{OH} =-2 mA	2.4		V	
V _{OLT}	Output LOW Voltage	I _{OL} =4 mA		0.45	V	
I _{OST}	Output Short Circuit Current	V _{OUT} =0V ^[2]	-15	-90	mA	
ECL Compatible Input Pins (REFCLK+/-, CD, TSER+/-, RIN+/-)						
I _{IHE}	ECL Input HIGH Current		V _{IN} =V _{IHE(MAX)}		+250	μA
		TSER/RIN	V _{IN} =V _{IHE(MAX)}		+750	μA
I _{ILE} ^[3]	ECL Input LOW Current		V _{IN} =V _{I(L)E(MIN)}	+0.5		μA
		TSER/RIN	V _{IN} =V _{I(L)E(MIN)}	-200		μA
V _{IDIFF}	Input Differential Voltage	TSER/RIN		50	1200	mV
		REFCLK		100	1200	mV
V _{IHE}	Input High Voltage	TSER/RIN			V _{CC}	V
		REFCLK		3.0	V _{CC}	V
		CD		V _{CC} - 1.165	V _{CC}	V
V _{I(L)E}	Input LOW Voltage			2.0		V
		REFCLK		2.5		V
		CD (ECL)		2.5	V _{CC} - 1.475	V
		CD (Disable)		-0.5	0.8	V
ECL Compatible Output Pins (ROUT+/-, RCLK+/-, RSER+/-, TOUT+/-, TCLK+/-)						
V _{OHE}	ECL Output HIGH Voltage	Commercial		V _{CC} - 1.03	V _{CC} - 0.83	V
		Industrial ^[4]		V _{CC} - 1.08	V _{CC} - 0.83	V
V _{OLE}	ECL Output LOW Voltage	T > 0°C		V _{CC} - 1.86	V _{CC} - 1.62	V
V _{ODIFF}	Output Differential Voltage		0.6		V	
Three-Level Input Pins (MODE)						
V _{IHH}	Three-Level Input HIGH			V _{CC} - 1.0	V _{CC}	V
V _{I(M)M}	Three-Level Input MID			V _{CC} /2 - 0.5	V _{CC} /2 + 0.5	V
V _{I(L)L}	Three-Level Input LOW			0.0	1.0	V
Operating Current^[5]						
I _{CCS}	Static Operating Current				30	mA
I _{CCR}	Receiver Operating Current				50	mA
I _{CCT}	Transmitter Operating Current				13	mA
I _{CCE}	ECL Pair Operating Current				7.0	mA
I _{CC5}	Additional Current at 51.84 MHz				7.0	mA
I _{CCO}	Additional Current LF1=LOW				3	mA

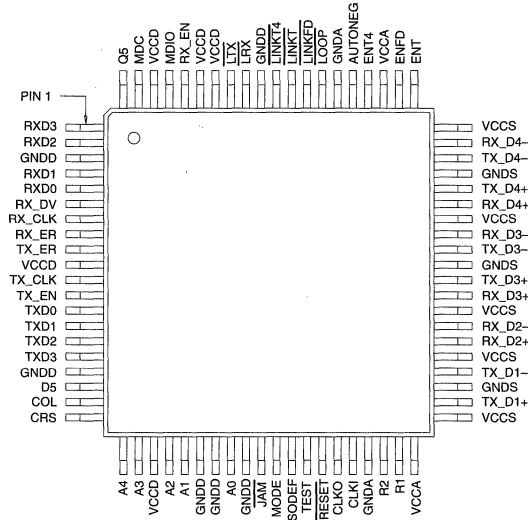
Capacitance^[6]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f ₀ = 1 MHz, V _{CC} = 5.0V	10	pF

Switching Waveforms for the CY7B951 SONET/SDH Serial Transceiver

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7B951-SC	S13	24-Lead (300-Mil) Molded SOIC	Commercial
	CY7B951-SI	S13	24-Lead (300-Mil) Molded SOIC	Industrial

Document #: 38-00358-C

Pin Configuration
**80-Lead Plastic Quad Flatpack
(Top View)**


7C971-2

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-3.0V to +7.0V

Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Pin Descriptions (continued)
Media Dependent Interface

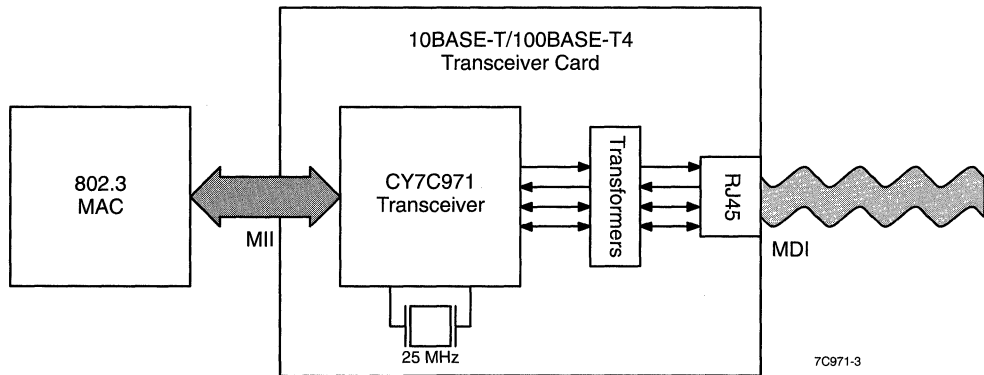
Name	I/O	Description
TX_D1+ TX_D1-	Differential Output	Transmit Data. TX_D1± are differential line drivers for data transmission. In 10BASE-T mode TX_D1± transmit Manchester encoded data with a nominal period of 100 ns. In 100BASE-T4 mode TX_D1± transmit 8B6T ternary symbols with a nominal period of 40 ns. TX_D1± also participate in the Link Integrity function.
RX_D2+ RX_D2-	Differential Input	Receive Data. RX_D2± are differential line receivers for data reception. In 100-Mb/s mode, RX_D2± receives 8B6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, RX_D2± receives Manchester encoded bits with a nominal period of 100ns. RX_D2± also participates in the Link Integrity function.
TX_D3+ TX_D3-	Differential Output	Transmit Data. TX_D3± are differential line drivers for data transmission. In 100-Mb/s mode, TX_D3± transmits 6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, TX_D3± are not used.
RX_D3+ RX_D3-	Differential Input	Receive Data. RX_D3± are differential line receivers used for data reception. In 100-Mb/s mode, RX_D3± receives 6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, RX_D3± are not used.
TX_D4+ TX_D4-	Differential Output	Transmit Data. TX_D4± are differential line drivers used for data transmission. In 100-Mb/s mode, TX_D4± transmits 6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, TX_D4± are not used.
RX_D4+ RX_D4-	Differential Input	Receive Data. RX_D4± are differential line receivers used for data reception. In 100-Mb/s mode, RX_D4± receives 6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, RX_D4± are not used.

Physical Media Attachment Interface

Name	I/O	Description
MODE	Input (TTL)	Mode. When MODE is tied HIGH, the transceiver is in normal mode. Received and transmitted data will move through the PMA and the PCS sublayers. Asserting MODE LOW exposes the 100BASE-T4 PMA service interface and disables 10BASE-T. The PCS is bypassed and the binary coded 6T serial data is presented at the MII and PMA interface pins.
D5	Input (TTL)	PMA Input Data. D5 is an input signal to the PMA transmit sublayer when MODE is asserted LOW.
Q5	Output (TTL, Three State)	PMA Output Data. Q5 is an output signal from the PMA receive sublayer when MODE is asserted LOW. Q5 is high-impedance when RX_EN is HIGH.

Control and Status

Name	I/O	Description
RESET	Input (TTL)	Reset. When RESET is asserted LOW, the PHY is placed in the reset state and the transmit and receive functions are disabled. The MII registers are placed in their default states.
AUTONEG	Input (TTL)	Auto-Negotiation Enable. When asserted HIGH, Auto-Negotiation capability is enabled by setting the Status Register bit 1.3. Auto-Negotiation is controlled through the MII management registers. When asserted LOW, Auto-Negotiation capability is disabled. AUTONEG is sampled on the rising edge of RESET.
ENT4	Input (TTL)	Enable 100BASE-T4. ENT4 enables 100BASE-T4 operation by setting the Status Register bit 1.15. When ENT4 is HIGH, bit 1.15 is forced HIGH, enabling 100BASE-T4 operation. When ENT4 is LOW, bit 1.15 is forced LOW, disabling 100BASE-T4. ENT4 is latched on the rising edge of RESET.
ENT	Input (TTL)	Enable 10BASE-T. ENT enables 10BASE-T operation by setting the Status Register bit 1.11. When ENT is HIGH, bit 1.11 is forced HIGH, enabling 10BASE-T operation. When ENT4 is LOW, bit 1.11 is forced LOW, disabling 10BASE-T. ENT is latched on the rising edge of RESET.
ENTFD	Input (TTL)	Enable 10BASE-T Full Duplex. ENT4 enables 10BASE-T Full Duplex operation by setting the Status Register bit 1.12. When ENTFD is HIGH, bit 1.12 is forced HIGH, enabling 10BASE-T Full Duplex operation. When ENTFD is LOW, bit 1.12 is forced LOW, disabling 10BASE-T Full Duplex. ENTFD is latched on the rising edge of RESET.
ISODEF	Input (TTL)	Isolate Default. ISODEF determines the default state of Isolate Bit 0.10 in the Control Register. When ISODEF is HIGH, the default value for 0.10 is 1. When ISODEF is LOW, the default value for 0.10 is 0. ISODEF is latched on the rising edge of RESET.
LOOP	Input (TTL)	Loopback Enable. When asserted LOW, the transmitter bit stream is looped back to the receiver for diagnostic testing. When LOOP is HIGH, the Loopback function is controlled by the Loopback bit in the control register.


Figure 1. Transceiver Card Block Diagram

CY7C971 Description

100BASE-T4

The CY7C971 provides a physical layer interface (PHY) for dual speed IEEE 802.3 100BASE-T4 and 10BASE-T CSMA/CD local area networks. 100BASE-T4 offers increased performance over existing 10BASE-T networks while maintaining compatibility with the existing Ethernet Media Access Control (MAC) specification. The 100BASE-T4 PHY interfaces to 4 pairs of category 3, 4, or 5 cable. The 100BASE-T4 PHY is comprised of the Physical Coding Sublayer (PCS), Physical Media Attachment (PMA), Media Independent Interface (MII), and Media Dependent Interface (MDI). A typical 100BASE-T4 transceiver card application is shown in *Figure 1*.

Transmitter

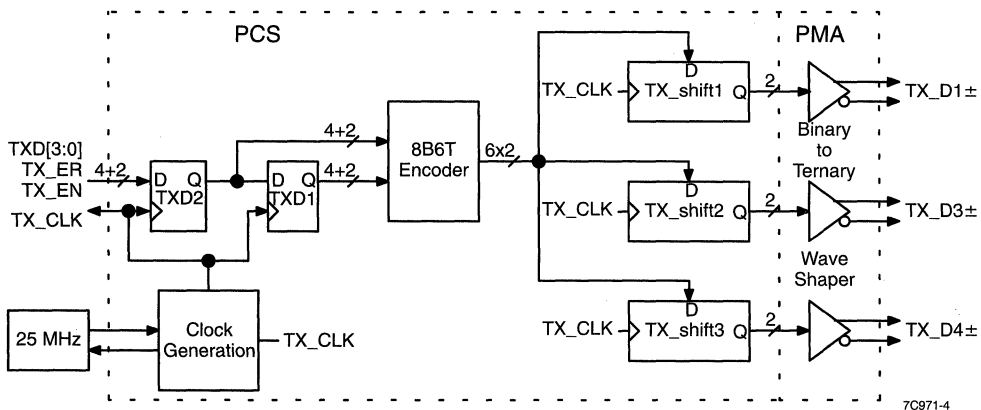
The transmitter is comprised of the Physical Coding Sublayer (PCS) and the Physical Media Attachment (PMA). *Figure 2* shows a block diagram of the T4 transmitter.

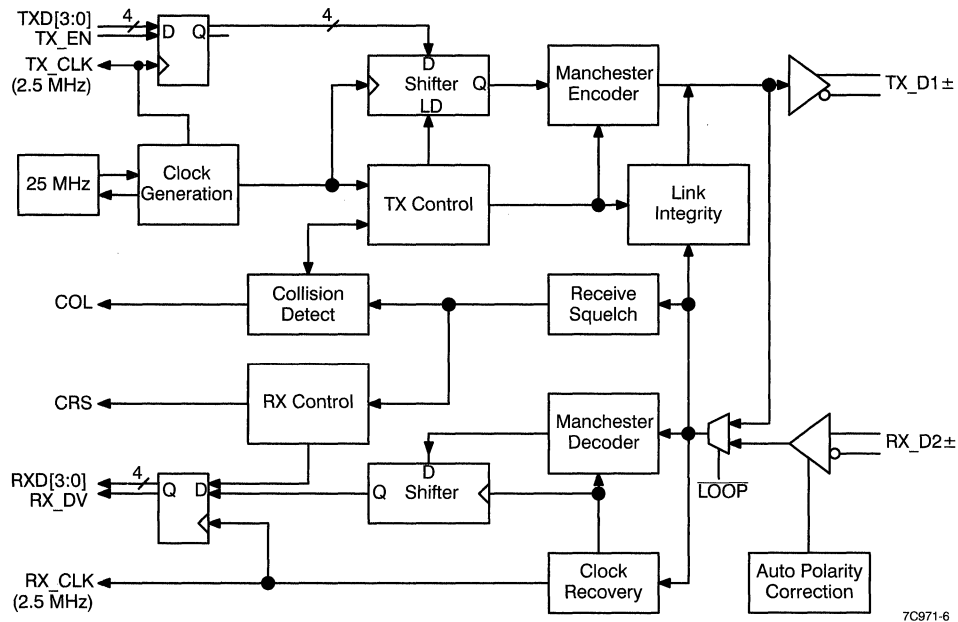
Transmit Physical Coding Sublayer (PCS)

The PCS takes nibble-wide data from the MII and accumulates them into 8-bit octets in the TXD1 and TXD2 registers. The octets are then encoded using the 8B6T ternary code according to the 802.3 standard. The encoded 8B6T code groups are then loaded in binary form to the shift registers.

Three shift registers convert the parallel 8B6T code groups to serial form. When the transmitter is active, a shift register is loaded on every other TX_CLK cycle. The first 8B6T code group of the frame is loaded into TX_shift1. The second group is loaded into TX_shift2 and the third into TX_shift3. The 4th group will be loaded into TX_shift1. This sequence continues until all of the 8B6T code groups comprising the frame have been transmitted.

At the start of the transmit frame, TX_shift2 and TX_shift3 will be loaded with a pad sequence aligned with first 8B6T code group in TX_shift1. The pad sequence aids the receiver with clock recovery and pair alignment. The preamble is generated automatically and follows the pad sequence.


Figure 2. T4 Transmitter Block Diagram


Figure 4. 10BASE-T Transmitter & Receiver Block Diagram

Full Duplex

The CY7C971 supports Full Duplex operation in 10BASE-T mode. 10BASE-T Full Duplex operation is automatically selected if Auto-Negotiation established 10BASE-T Full Duplex as the highest common operating mode. The 10BASE-T Full Duplex operation can also be selected manually by disabling Auto-Negotiation and clearing the Speed Selection (0.13) bit and setting the Duplex Mode Bit (0.8) in the MII Control Register. 10BASE-T Full Duplex mode cannot be enabled through Auto-Negotiation or manually unless the ENTDFD pin is HIGH. The LINKFD pin indicates when 10BASE-T Full Duplex is the selected mode of operation and the 10BASE-T transceiver is in the Link Pass State. During full duplex operation, the collision pin (COL) is LOW.

Auto-Polarity Correction

The Auto-Polarity Correction function monitors the received signal polarity on RX_D2± and inverts the received signal internally if its polarity is inverted. Auto-Polarity Correction is active during Auto-Negotiation and normal operation.

Media Independent Interface (MII)

The MII provides a connection between the PHY and the MAC and between the PHY and the station management (STA) entity. The MII is capable of supporting 100- and 10-Mb/s operation.

Data transfer is accomplished over nibble-wide dedicated transmit and receive channels. When TX_EN is asserted HIGH, data on TXD[3:0] channel is latched into the PHY on the rising edge of TX_CLK and passed to the PCS. If TX_ER is asserted HIGH, an 8B6T code violation word will be sent in place of the transmit data.

TX_CLK provides a continuous clock that is sourced from the PHY.

When recovered data is available from the PCS, the RX_DV signal is asserted HIGH simultaneously with the first Start of Frame Delimiter (SFD) nibble on RXD[3:0]. The RX_DV signal remains HIGH continuously through the final recovered nibble of the frame. If an error is detected in the frame by the PHY, the RX_ER signal is driven HIGH synchronously with RX_CLK.

RX_CLK is a continuous clock that provides a timing reference for the transfer of RXD[3:0], RX_DV, and RX_ER from the PHY to the MAC. RX_CLK is sourced from the PHY. While RX_DV is deasserted, RX_CLK will run at the PHY's nominal frequency. When RX_DV is asserted, the frequency and phase of RX_CLK is recovered from the received data. During the transition from nominal to recovered frequency, the period of RX_CLK may extend by up to one cycle. RX_CLK stretching prevents logic failures from occurring in downstream logic while the clock makes its transition.

When a carrier is detected, the CRS signal is asserted HIGH. A collision is signaled by asserting COL HIGH. CRS is asserted throughout a collision condition.

Access to the management facilities are provided through the MII with the MDC and MDIO pins. These pins provide a serial interface to the management control and status registers. The MDC signal is driven to the PHY from the management station (STA) as a timing reference for transfer of information on the MDIO signal. The MDIO signal is a bidirectional signal between the PHY and the STA. Control information is driven by the STA to the PHY. Status information is driven from the PHY to the STA.

Table 2. MII Status Register Definition

Status Register (Register 1)					
Bit(s)	Name	Setting	R/W	Default	Description
1.15 ^[4]	100BASE-T4	1 = 100BASE-T4 Able 0 = 100BASE-T4 Able	RO	1,0	When set, this bit indicates that the PHY is 100BASE-T4 capable.
1.14	100BASE-TX Full Duplex	0 = 100BASE-TX Full Duplex Not Supported	RO	0	This bit is always set to zero.
1.13	100BASE-TX Half Duplex	0 = 100BASE-TX Half Duplex Not Supported	RO	0	This bit is always set to zero.
1.12 ^[5]	10BASE-T Full Duplex	1 = 10BASE-T Full Duplex Able 0 = 10BASE-T Full Duplex Able	RO	1,0	When set, this bit indicates that the PHY is 10BASE-T full duplex capable.
1.11 ^[6]	10BASE-T Half Duplex	1 = 10BASE-T Half Duplex Able 0 = 10BASE-T Half Duplex Able	RO	1,0	When set, this bit indicates that the PHY is 10BASE-T half duplex capable.
1.10:6	Reserved	0 = Default	RO	0	
1.5	Auto-Negotiation Complete	1 = Auto-Negotiation Complete 0 = Auto-Negotiation Incomplete	RO	0	This bit is set when NWAY has completed the auto negotiation process.
1.4	Remote Fault	1 = Remote Fault Condition 0 = No Remote Fault Condition	RO	0	This bit is set when Auto Negotiation detects a remote fault.
1.3 ^[7]	Auto Negotiation Ability	1 = PHY is Able to Perform Auto Negotiation	RO	1,0	PHY supports Auto-Negotiation.
1.2	Link Status	1 = Link Is Up 0 = Link Is Down	RO	0	Link Status indicates that the PHY is in the Link Pass State.
1.1	Jabber Detect	1 = Jabber Condition Detected 0 = No Jabber Condition Detected	RO LH	0	Jabber Detect indicates that a jabber condition has been detected for 10BASE-T.
1.0	Extended Capabilities	1 = Extended Register Capable	RO	1	OUI and Auto-Negotiation Extended Registers 2–7 are present.

Vendor and Product ID Registers

Vendor and Product identification codes are stored in management ID registers 2 and 3. These registers contain the Cypress Semiconductor Corporation unique identifier and the CY7C971 product and revision number. *Table 3* explains the ID registers.

Auto-Negotiation Registers

The Auto-Negotiation process is managed through the Auto-Negotiation registers. Register 4 is the Auto-Negotiation Advertisement register. This register contains the 16-bit code word that is advertised to the remote link partner. Register 5 is the Auto-Negotiation Link Partner Ability register for base and next pages. This register holds the 16-bit code word that the Auto-Negotiation function receives from the remote link partner. Register 6 is the Auto-Negotiation Expansion register and is used to monitor the negotiation process. Register 7 is the Auto-Negotiation Next Page Transmit register. The function of the Auto-Negotiation register bits are defined in *Tables 4* through 7.

Auto-Negotiation

The IEEE Auto-Negotiation function provides remote capability detection and automatic speed selection. Auto-Negotiation is fully compatible with existing 10BASE-T only devices.

Notes:

- 100BASE-T4 Default is set by the ENT4 pin.
- 10BASE-T FD Default is set by the ENTFD pin.

Auto-Negotiation advertises the capabilities of the PHY by transmitting a sequence of fast link pulses (FLPs) that form a standard 16-bit code word. The advertised code word is contained in the Auto-Negotiation Advertisement register (Register 4). Auto-Negotiation receives 16-bit code words and stores them in the Auto-Negotiation Partner Ability register (Register 5). Once the code words have been sent and acknowledged, Auto-Negotiation selects the highest common operating mode as the current mode of operation. The highest common mode of operation is determined by the Priority Resolution Table specified in the Auto-Negotiation standard. When a mode of operation is selected, Auto-Negotiation enables the transition to the selected mode's Link Pass state.

The Auto-Negotiation process is controlled and monitored through the MII management registers. Auto-Negotiation may be disabled in the MII control register or by asserting the AUTONEG pin HIGH.

The Auto-Negotiation is capable of transmitting and receiving code word pages in addition to the base pages. The next page process is controlled through the MII registers.

- 10BASE-T HD Default is set by the ENT pin.
- Auto-Negotiation Default is set by the AUTONEG pin.

Table 5. MII Auto-Negotiation Link Partner Ability Register Definition

Auto-Negotiation Link Partner Ability Register (Register 5)					
Bit(s)	Name	Setting	R/W	Default	Description
5.15	Remote Next Page	1 = Next Page to be Transmitted 0 = No Next Page	RO	0	When set, this bit indicates the remote PHY has a Next Page to send.
5.14	Remote Acknowledge	1 = Remote Acknowledge 0 = No Acknowledge	RO	0	When set, this bit indicates that the remote PHY has acknowledged receipt of a page.
5.13	Remote Fault	1 = Fault Indication 0 = No Fault	RO	0	When set, this bit indicates that a fault has occurred in the remote PHY.
5.12	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
5.11	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
5.10	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
5.9	Technology Ability Field 100BASE-T4	1 = 100BASE-T4 Able 0 = Not 100BASE-T4 Able	RO	0	When set, this bit indicates that the remote PHY has 100BASE-T4 capability.
5.8	Technology Ability Field 100BASE-TX Full Duplex	1 = 100BASE-TX FD Able 0 = Not 100BASE-TX FD Able	RO	0	When set, this bit indicates that the remote PHY has 100BASE-TX FD capability.
5.7	Technology Ability Field 100BASE-TX	1 = 100BASE-TX Able 0 = Not 00Base-TX Able	RO	0	When set, this bit indicates that the remote PHY has 100BASE-TX capability.
5.6	Technology Ability Field 10BASE-T Full Duplex	1 = 10BASE-T FD Able 0 = Not 10BASE-T Able	RO	0	When set, this bit indicates that the remote PHY has 10BASE-T FD capability.
5.5	Technology Ability Field 10BASE-T	1 = 10BASE-T Able 0 = Not 10BASE-T Able	RO	0	When set, this bit indicates that the remote PHY has 10BASE-T capability.
5.4:0	Selector Field	Indicates LAN Type	RO	00h	This field indicates the type of LANs being advertised by the remote PHY.

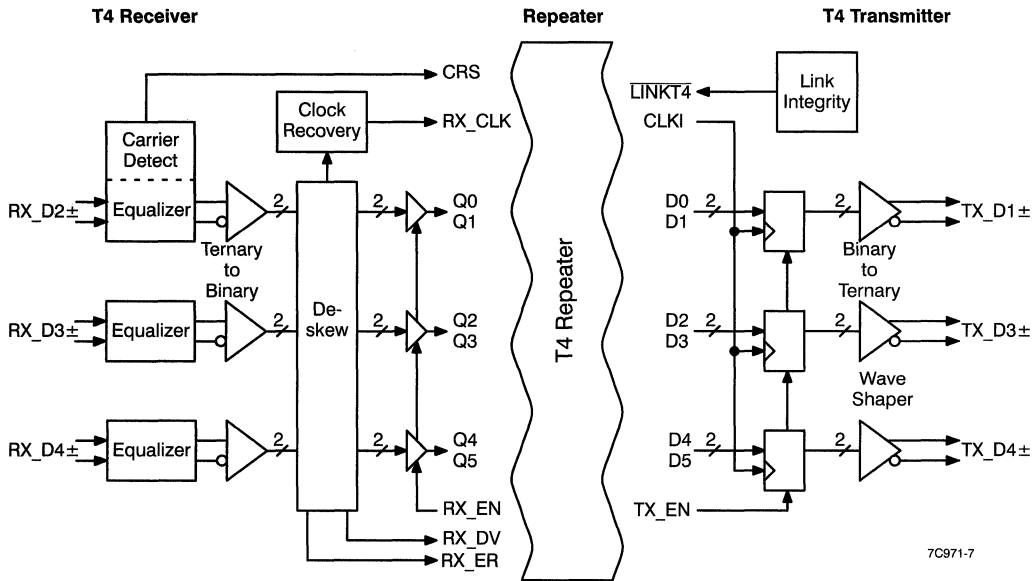


Figure 5. T4 Transmitter & Receiver PMA Interface and Block Diagram (MODE = LOW)

Serial 6T data from the three PMA circuits are transferred over the PMA interface pins in binary form. The Receiver aligns and converts the line signals to their 6T binary representation and drives them to the Q[5:0] pins. The transmitter latches the three 6T symbol streams on its D[5:0] input pins on the rising edge of TX_CLK. The 6T symbols are loaded into the waveshaper DAC and converted to their corresponding ternary waveforms. Table 8 shows the mapping of binary PMA signals to ternary waveforms.

Table 8. PMA Binary to Ternary Map^[11]

PMA Q1-0, Q3-2, Q5-4 D1-0, D3-2, D5-4	Transmitter	Receiver
00	CS0	CS0
10	CS1	CS1
01	CS-1	CS-1
11	CS0	-

Notes:

- 11. CS0 is a waveform which conveys the ternary symbol 0.
- CS1 is a waveform which conveys the ternary symbol 1.
- CS-1 is a waveform which conveys the ternary symbol -1.

The RX_DV signal indicates when the first data symbol after sob is present on the Q0-5 PMA interface pins. RX_DV will remain HIGH throughout the transfer of data symbols across the PMA interface. RX_DV is LOW when there is no carrier present. RX_ER HIGH indicates a pair alignment error. The RX_EN input pin enables the Q0-5, RX_DV, and RX_ER drivers. RX_EN LOW places the drivers in the high-impedance state.

The transmit PMA interface is synchronous to the CLKI input clock signal. The TX_EN HIGH causes data on the PMA D0-5 pins to be loaded into the transmit PMA waveshaper on the rising edge of CLKI. When TX_EN is LOW, the output drivers transmit the CS0 idle symbols.

Applications

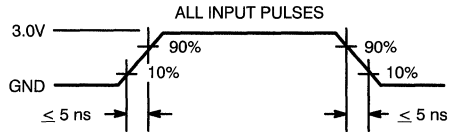
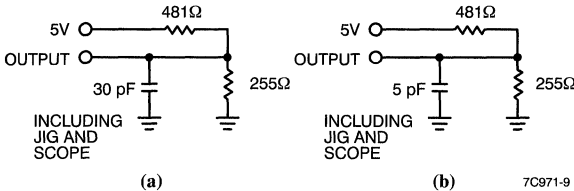
The CY7C971 is a flexible physical-layer device that fits into any Ethernet application including network interface cards, transceiver cards, repeaters, hubs and switches. Figure 6 shows a schematic of the CY7C971 configured for a transceiver card application with an exposed MII port.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
TTL Pins					
V _{OHT}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		V
V _{OLT}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 4.0 mA		0.4	V
V _{IHT}	Input HIGH Voltage		2.0	6.0	V
V _{ILT}	Input LOW Voltage		-3.0	0.8	V
I _{IXT}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	μA
I _{OZT}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-50	+50	μA
I _{OST}	Output Short Circuit Current ^[12]	V _{CC} = Max., V _{OUT} = GND		-350	mA
Open Drain LED Pins					
V _{OLD}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 12.0 mA		0.4	V
Miscellaneous					
I _{CC1}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, 100BASE-T4 transmitting		300	mA
I _{CC2}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, 100BASE-T4 not transmitting		100	mA
I _{SB}	Power-Down Current	Max. V _{CC}		TBD	mA

Capacitance^[13]

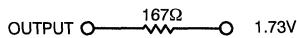
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	5	pF
C _{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms


7C971-9

7C971-10

Equivalent to: THÉVENIN EQUIVALENT


Notes:

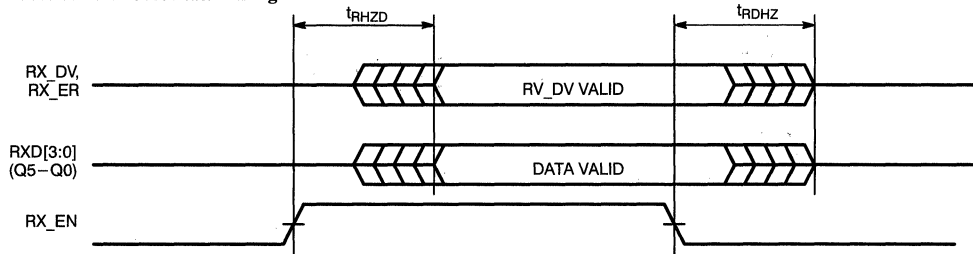
12. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
13. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range (continued)

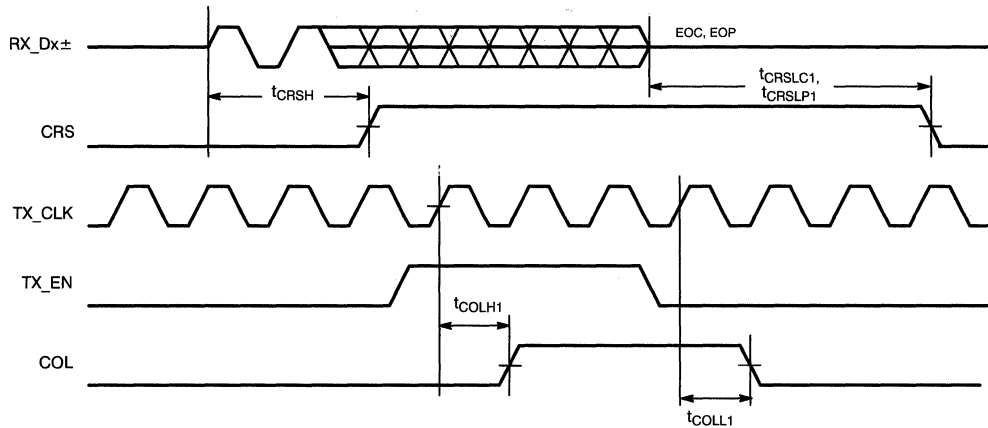
Parameter	Description	Min.	Max.	Unit
10BASE-T CRS and COL				
$t_{CRSH3}^{[23]}$	CRS Assert Latency		500	ns
$t_{CRSL3}^{[24]}$	CRS Deassert Latency		500	ns
Management Timing				
t_{MCPWH}	MDC Pulse Width HIGH	25		ns
t_{MCPWL}	MDC Pulse Width LOW	25		ns
f_M	MDC Frequency		12.5	MHz
t_{MDS}	MDIO Set-Up	10		ns
t_{MDH}	MDIO Hold	0		ns
t_{MDO}	MDIO Valid from Clock		40	ns
t_{MDOH}	MDIO Hold from Clock	0		ns
t_{MDHZ}	MDC to High Impedance		40	ns
t_{MDLZ}	MDC to Low Impedance	0	20	ns
Control and Status Timing				
t_{RL}	Reset Pulse Width LOW	5		μ s
t_{RS}	Control Input Set-Up	100		ns
PMA Interface Timing				
t_{TPMA}	PMA Transmit Latency		40	ns
t_{TDS}	PMA Transmit Data Set Up	10		ns
t_{TDH}	PMA Transmit Data Hold	0		ns
$t_{PMACRSH}$	PMA CRS Assert Latency	110	140	ns
$t_{PMACRSL}$	PMA CRS Deassert Latency		650	ns
$t_{PMADATA}$	PMA Receiver Data Latency		800	ns
Clock Timing				
t_{CPWH}	Reference Clock Pulse Width HIGH	16	24	ns
t_{CPWL}	Reference Clock Pulse Width LOW	16	24	ns
f_C	Reference Clock Frequency	25 – 100 ppm	25 + 100 ppm	MHz

Notes:

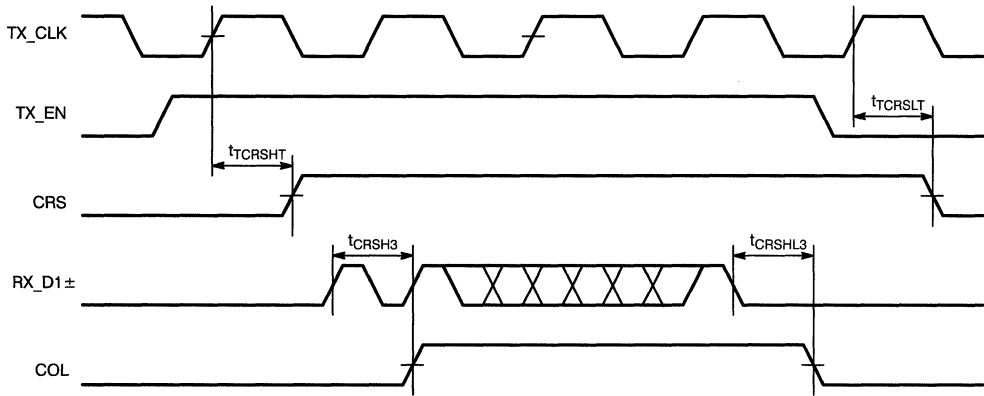
23. t_{CRSH3} is measured from the rising edge of the signal on RX_D2 that meets the 10BASE-T carrier criterion to the rising edge of CRS.
24. t_{CRSL3} is measured from the end of the last data symbol on RX_D2 to the falling edge of CRS.

Switching Waveforms (continued)
MII Receive Port Three State Timing


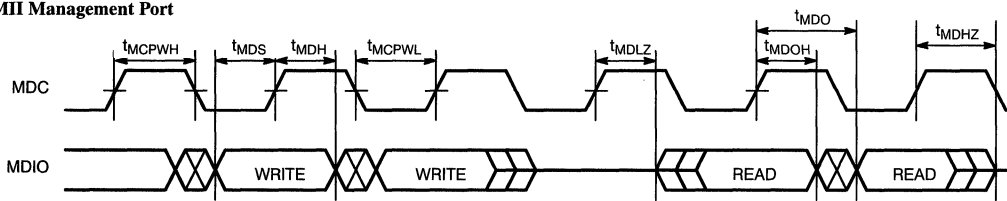
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MII Carrier Sense and Collision (100BASE-T4)


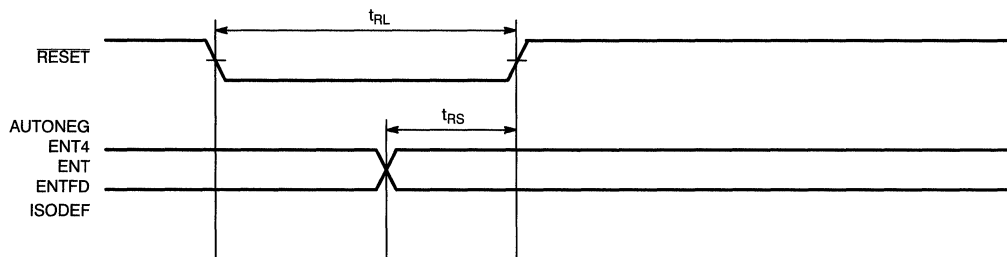
7C971-14

Switching Waveforms (continued)
MII Carrier Sense and Collision (10BASE-T) [29]


7C971-17

MII Management Port


7C971-18

Control and Status Pins


7C971-19

Notes:

29. Switching waveforms show CRS and COL timing for a collision that is started and terminated by activity on the receive path.



100BASE-TX/10BASE-T Fast Ethernet Transceiver

Features

- Complies with IEEE 802.3u standard
- Four Operating Modes:
 - 100BASE-TX
 - 100BASE-TX Full Duplex
 - 10BASE-T
 - 10BASE-T Full Duplex
- Media Independent Interface (MII)
 - Three-state receive port
 - Serial management port
- Auto-Negotiation
- MLT-3 Transmitter/Receiver for 100BASE-TX
- Cat. 5 twisted-pair adaptive equalizer for 100BASE-TX
- PMA interface for repeater applications
- LED status indicators: TX, RX, Link

- Loopback mode for PHY integrity testing
- 80-pin PQFP

Functional Description

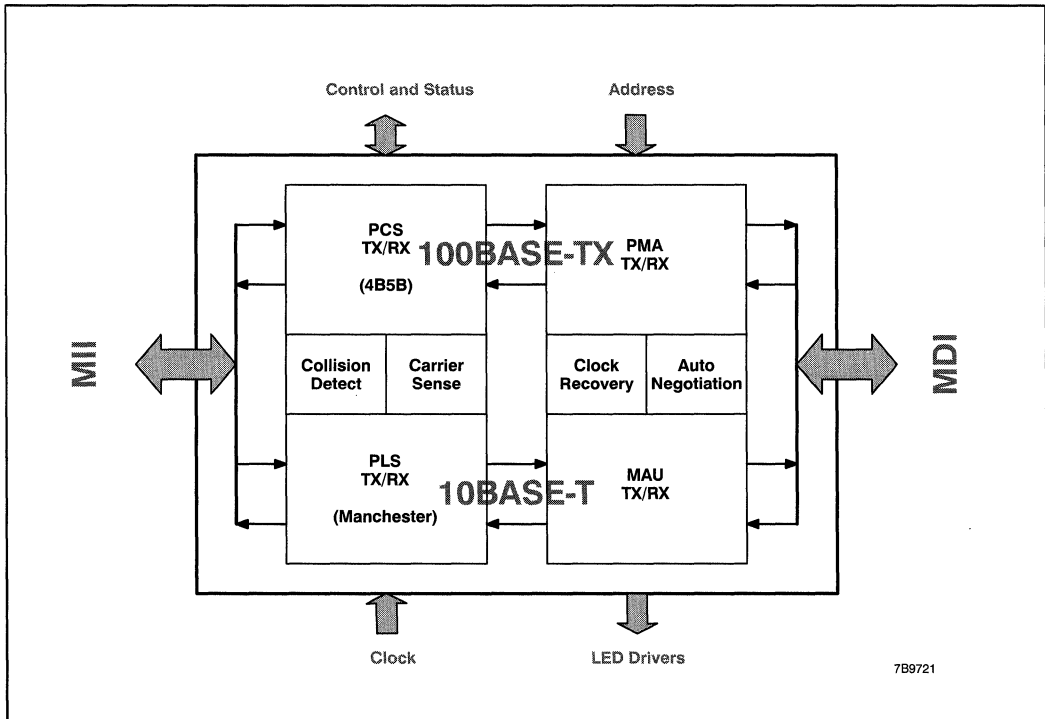
The CY7B972 is a full featured physical layer transceiver (PHY) devices supporting both 100BASE-TX (Fast Ethernet) and 10BASE-T Local Area Network (LAN) standards. The CY7B972 complies with IEEE 802.3 100BASE-TX, 10BASE-T, Auto-Negotiation and MII standards.

The CY7B972 interfaces to two pair of category 5 unshielded twisted-pair cable or fiber. The Media Independent Interface (MII) attaches directly to 802.3 Media Access Control (MAC) layer devices.

The CY7B972 performs the Physical Coding Sublayer (PCS), Physical Media Attachment (PMA), Physical Layer Sig-

naling (PLS), and Media Attachment Unit (MAU) functions defined in the 802.3 standard for 100BASE-X and 10BASE-T. Ethernet frames are transferred from the MAC to the CY7B972 over the MII interface. The data is encoded in the PCS or PLS encoder (4B5B for 100BASE-TX or Manchester for 10BASE-T) and then passed to the PMA or MAU where the serial encoded data is shifted bitwise on to the twisted pair media. Collision and Carrier Detect signals are generated by the CY7B972 and passed to the MAC over the MII.

The CY7B972 PHY uses 802.3 standard Auto-Negotiation to configure the twisted-pair link. The CY7B972 also includes a direct interface to the PMA layer for repeater applications.



7B9721

Pin Description

Pin Number		Pin Name	Description
16-Pin DIP	28-Pin PLCC		
1	2	CD+	AUI Collision Output pins. Differential driver that transmit a 10-MHz signal during collision events, jabber and CD Heartbeat conditions. Also referred to as CI port.
2	3	CD-	
3	4	RX+	AUI Receive Output pins. Differential driver that outputs the signal receive from the line. Also referred to as DI port.
6	12	RX-	
7	13	TX+	AUI Transmit Input pins. Differential receiver that inputs the signal for transmission onto the cable.
8	14	TX-	
9	15	HBE	Heartbeat Enable Pin. When this pin is grounded, the heartbeat is enabled. When the pin is connected to V_{EE} , the heartbeat is disabled.
11	18	RR+	External Resistor. A 1K 1% resistor should be connected between these pins to establish proper internal operation current.
12	19	RR-	
14	26	RXI	Receive Input. This pin is connected directly to the coaxial cable.
15	28	TXO	Transmitter Output. This pin is connected directly (10BASE2 thin wire) or through a diode to the coaxial cable.
16	1	CDS	Collision Detect Sense. Ground sense connection for the collision detect circuit. This pin should be connected separately to the shield to prevent ground drops from altering the receive mode collision detect threshold.
10	16,17	GND	Positive Power Supply Pin.
4,5,13	5-11 20-25	V_{EE}	Negative Power Supply Pin.

CY7B8392 Description
Transmitter

The CY7B8392 transfers Manchester-encoded data from the AUI port of the DTE (TX+ and TX-) to the coaxial cable. The output waveform is wave shaped to meet IEEE 802.3 specifications. For Ethernet compatible applications (10BASE5), an external isolation diode may be added to further reduce the coax load capacitance.

The AUI squelch circuit prevents signals with less than 15 ns pulse width or smaller than 175 mV average dc level from reaching the output driver. The squelch circuit also turns the transmitter off at the end of the packet if the average of the dc level of the signal stays greater than 175 mV for more than 190 ns.

Receiver

The CY7B8392 receiver transfers the serial data from the coaxial cable to the DTE via the balanced differential output (RX+ and RX-). The received signal is amplified and equalized by the on chip equalizer.

The device also contains an internal squelch function that discriminates noise from valid data. A 4-pole Bessel filter is used to extract the DC level of the received signal. If the DC level of the received signal is lower than an internally set squelch threshold, the CY7B8392 receive function will not be activated.

Collision Detection

The collision detection circuit monitors the signal level on the coax cable. This signal voltage level is compared against the collision voltage threshold V_{CD} . When the measured signal level is

Note:

1. BT = Bit Time = 100 ns.

more negative than V_{CD} , a collision condition is declared by the CY7B8392 by sending a 10-MHz signal over the CD+/CD-pair.

Long Cable Application

The IEEE 802.3 standard is designed for 500 meters of Ethernet cable and 185 meters of thin coax cable (RG58A/U). To extend the cable segment to 1000 meters and 300 meters of Ethernet cable and thin coaxial cable respectively, transmit collision detection mode is required. The disadvantage of the transmit collision detection mode is that it will detect collision only when the station is transmitting; it will not be able to detect collision of two far-end stations when it is not transmitting. Note that transmit mode collision detection is not allowed in repeater applications.

Implementation of transmit mode collision detection with CY7B8392 is simple. By connecting an external resistor divider to the CDS pin; R1 to 150 ohms and R2 to 10 Kohms, the device is now in transmit collision detection mode.

The CY7B8392 utilizes a combination receive and transmit mode collision detection. When the device is idle it enters into receive collision detection mode, and when it is transmitting it is in the transmit collision detection mode.

Heartbeat Test Function

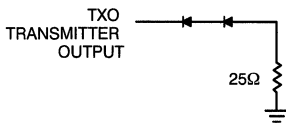
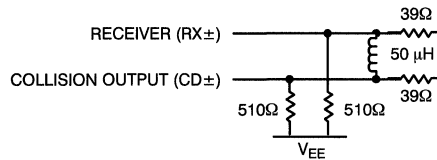
The Heartbeat Test Function is enabled when the HBE pin is tied to ground. When enabled, a 10-MHz collision signal is transmitted to the MAC over the CD+/CD- pair after the transmission of a packet for $10 \pm 5BT^{(1)}$. The Heartbeat function should be disabled by tying the HBE pin to V_{EE} for repeater applications.

Electrical Characteristics Over the Operating Range^[5]

Parameter	Description	Min.	Typ.	Max.	Unit
V _{EE}	Supply Voltage	-8.55	-9.0	-9.45	V
I _{EE1}	(V _{EE} to GND) Non-transmitting		-25	-35	mA
I _{EE2}	(V _{EE} to GND) Transmitting		-70	-80	mA
I _{RXI}	Input Bias Current (RXI pin)	-2		25	μA
I _{TDC}	Transmitter Output DC Current	37	41	45	mA
I _{TAC}	Transmitter AC Current	±28			mA
V _{CD}	Collision Threshold	-1.45	-1.53	-1.62	V
V _{CS}	Carrier Sense Threshold	-0.38	-0.45	-0.52	V
R _{X, C, D}	Differential Output Voltage	±500		±1500	mV
V _{OC}	Common Mode Voltage ^[6]	-1		-3	V
V _{TS}	Transmitter Squelch Threshold ^[7]	-175	-225	-300	mV
R _{RXI}	Shunt Resistance—Non-transmitting	100			KΩ
T _{TXO}	Shunt Resistance—Transmitting	10			KΩ

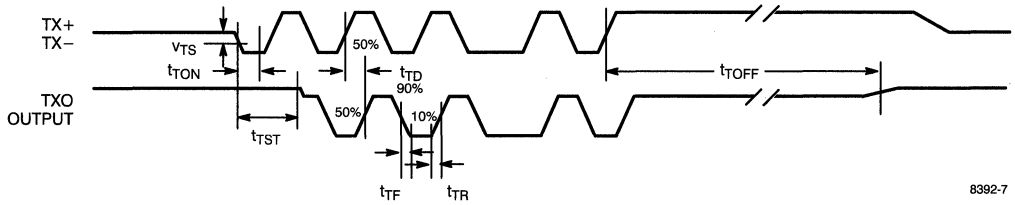
Capacitance

Parameter	Description	Test Conditions	Typ.	Unit
C _X	Input Capacitance		1.5	pF

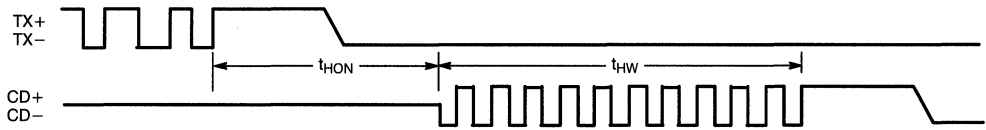
AC Test Loads and Waveforms

(a)

(b) 8392-5

Notes:

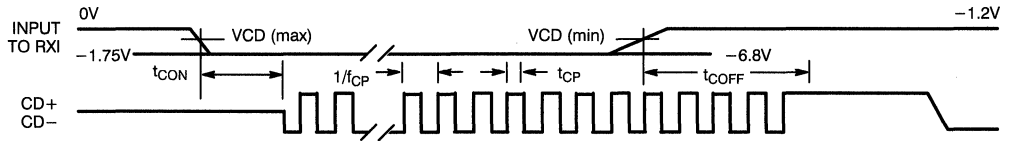
- Testing is done under test load as defined in AC Test Loads and Waveforms.
- During idle, V_{OC} is pulled down to V_{EE} to minimize the power dissipation across the load resistors connected to RX± and CD±.
- For a minimum pulse width of >40 ns.

Switching Waveforms (continued)
Transmit Timing


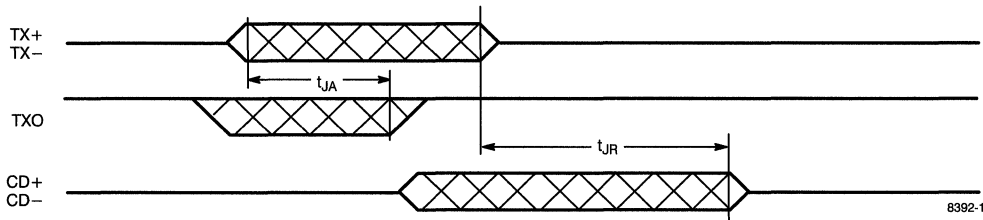
8392-7

Heartbeat Timing


8392-8

Collision Timing


8392-9

Jabber Timing


8392-10

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY7B8392-JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
CY7B8392-PC	P1	16-Lead (300-Mil) Molded DIP	



Functional Description

The HOTLink Evaluation Board (CY9266) is a system development tool that facilitates the design and evaluation of the Cypress HOTLink transmitter (CY7B923) and receiver (CY7B933) devices. The CY9266 Evaluation Board is offered with three serial media interface options: CY9266-C (copper), CY9266-F (fiber), and CY9266-T (twisted pair). The CY9266-C offers a low cost 1/4" coaxial connection, the CY9266-F interfaces with a longwave (1300 nm) LED optical transceiver and SC fiberoptic connector, and the CY9266-T is configured to support shielded twisted pair or twin axial cable that attaches through a 9-pin D-sub connector.

The CY9266 accepts data and control commands from the host via the parallel interface ports (available in three connectors). The 48-pin header connector allows interoperability with the IBM OLC-266 interface. The two 60-pin connectors are functionally equivalent. The vertical pin connector is used for probing and monitoring the appropriate signals, while the edge connector can be connected to a flat ribbon cable as a direct host communication interface.

In a typical point-to-point link, the host downloads parallel data to the CY9266 Evaluation Board. Parallel data can be formatted as pre-encoded 10-bit patterns or 8-bit data/special characters to be encoded by the HOTLink transmitter. The data is then encoded (optionally) and serialized by CY7B923 HOTLink Transmitter. Serial data is then transmitted via coax, twisted pair, or fiber.

In the receive operation, serial data is sent from a remote source (via copper/fiber/twisted pair) and transferred to the CY7B933 HOTLink receiver. The serialized data is converted to parallel and then optionally decoded. Parallel data is transferred to the host system along with various status and synchronizing signals. All I/O operations are performed between the host and the Evaluation Board using simple handshakes.

The CY9266 Evaluation Board can also operate in self-diagnostic mode and indicate errors in the serial transmission stream using a built-in two-digit, seven-segment LED display.

Document #: 38-00236-A

HOTLink is a trademark of Cypress Semiconductor Corporation.
 ESCON is a registered trademark of International Business Machines Corporation.
 IBM OLC-266 is a trademark of International Business Machines Corporation.
 HP HOLC-0266 is a trademark of Hewlett-Packard Corporation.

Typical Applications for the Evaluation Board include:

- HOTLink system development
- Telecommunication
- Remote data acquisition
- Processor-to-disk/peripheral communication
- Backplane extender
- Point-to-point video/image communications
- Point-to-point CPU/server communications
- High-speed data switching (TI Multiplier, etc.)
- Similar in function to IBM OLC-266 (single channel) and HP HOLC-0266™

Specification

Board Dimensions	3.0" x 4.0" (approx., plus media connector)
Two media types:	
CY9266-C	Coax connectors—BNC for transmit, TNC for receive
CY9266-F	Fiber optic module, single row or 4 row modules
CY9266-T	Twisted pair connector, 9-pin D-sub
Power Supply	+5V ± 5%
Maximum Clock Rate	33 MHz
Maximum Data Rate	330 Mbps
Parallel I/O	TTL
Serial I/O	Coax or twisted pair (CY9266-C/T) or Fiber optic with SC connector (CY9266-F)

Ordering Information

Ordering Code	Media Type
CY9266-C	Copper
CY9266-F	Fiber
CY9266-T	Twisted Pair
CY9266-FX	Fiber w/o optic module



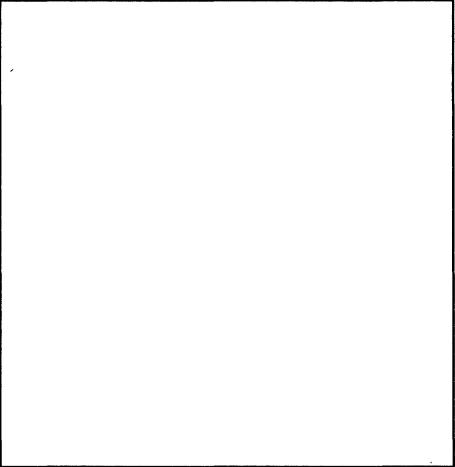
Section Contents

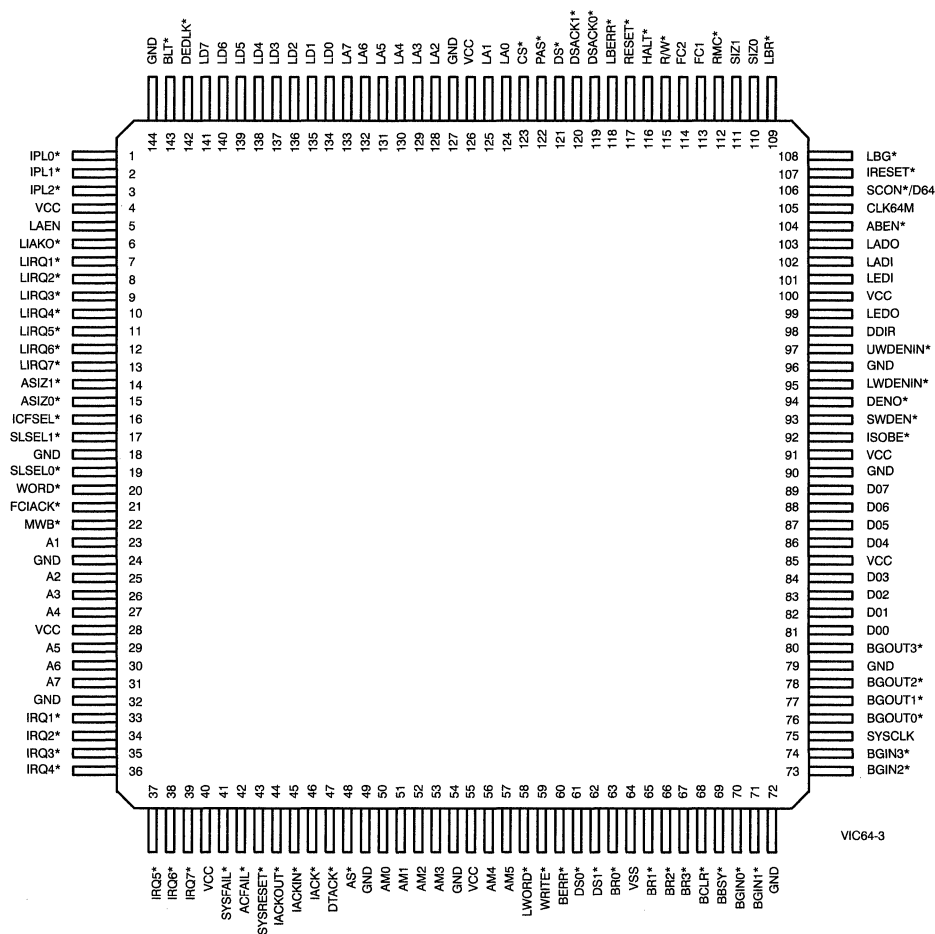
Bus Interface Products

Page Number

Device	Description	
VIC64	VMEbus Interface Controller with D64 Functionality	8-1
VIC068A	VMEbus Interface Controller	8-7
VAC068A	VMEbus Address Controller	8-16
CY7C960	Slave VMEbus Interface Controller Family	8-22
CY7C961	Slave VMEbus Interface Controller Family	8-22
CY7C964	Bus Interface Logic Circuit	8-27

Pin Configurations
**Pin Grid Array (PGA)
Bottom View**

A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
GND	IPL2*	LIACKO*	LIRQ2*	LIRQ5*	ASIZ1	ASIZ0	SLSEL1*	WORD*	FCIACK*	A02	A04	VCC	GND	IRQ4*	1
LD6	BLT*	IPL1*	VCC	LIRQ1*	LIRQ4*	LIRQ6*	ICFSEL*	MWB*	A01	A03	A05	A07	IRQ3*	IRQ7*	2
LD2	LD5	DEDLK*	IPL0*	LAEN	LIRQ3*	LIRQ7*	GND	SLSELO*	GND	A06	IRQ1*	IRQ2*	IRQ6*	ACFAIL*	3
LD1	LD3	LD7	LOCATOR PIN									IRQ5*	VCC	IACKOUT*	4
LA7	LD0	LD4										SYSFAIL*	SYSRESET*	DTACK*	5
LA3	LA5	LA6										IACKIN*	IACK*	AM0	6
LA2	LA4	GND										GND	AS*	AM1	7
LA1	LA0	VCC										GND	AM2	AM3	8
CS*	DSACK1*	DS*										VCC	LWORD*	AM4	9
PAS*	LBERR*	RESET*										BERR*	WRITE*	AM5	10
DSACK0*	R/W*	FC1										BR2*	DS1*	DS0*	11
HALT*	RMC*	LBR*										BBSY*	BR1*	BR0*	12
FC2	SI20	SCON*/D64	CLK64M									LADI	GND	VCC	GND
SI21	IRESET*	LADO	LEDI	DDIR	LWDENIN*	DENO*	D06	D03	D01	GND	BGOUT0*	BGIN3*	BGIN1*	BCLR*	14
LBG*	ABEN*	VCC	LEDO	UWDENIN*	SWDEN*	ISOBE*	D07	D05	D04	D02	BGOUT3*	BGOUT2*	SYSCLK	GND	15

Pin Configurations (continued)
144-Pin Thin Quad Flatpack (TQFP)
Top View


VIC64 Slave Block Transfer

The VIC64 is capable of decoding the address modifier codes to determine that a slave block transfer is desired. In this mode, the VIC64 captures the VMEbus address, and latches it into internal counters. For subsequent cycles, the VIC64 simply increments this counter for each transfer. The local protocol for slave block transfers can be configured in a full handshake mode by toggling both PAS* and DS* and expecting DSACKi* to toggle, or in an accelerated mode in which only DS* toggles and PAS* is asserted throughout the cycle.

For D64 slave block transfers, the SCON*/D64 signal is asserted to indicate a D64 transfer is in progress. External logic is required to de-multiplex the data from the VMEbus address bus for the upper 24 address/data lines. The lower 8 bits are done within the VIC64.

Module-Based DMA Transfers

The VIC64 can act as a DMA controller between two local resources. This mode is similar to that of master block transfers with local DMA, with the exception that the VMEbus is not the source or destination.

VIC64 Interrupt Generation and Handling Facilities

The VIC64 can generate and handle a seven-level prioritized interrupt scheme similar to that used by the Motorola 68K processors. These interrupts include:

- 7 VMEbus interrupts
- 7 local interrupts
- 5 VIC64 error/status interrupts
- 8 interprocessor communication interrupts.

The VIC64 can be configured to act as handler for any of the seven VMEbus interrupts. The VIC64 can generate the seven VMEbus interrupts as well as supplying a user-defined status/ID vector. The local priority level (IPL) for VMEbus interrupts is programmable. When configured as the system controller, the VIC64 drives the IACK* daisy chain.

The local interrupts can be configured with the following:

- User-defined local interrupt priority level (IPL)
- Option for VIC64 to provide the status/ID vector
- Edge or level sensitivity
- Polarity (rising/falling edge, active HIGH/LOW)

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
VIC64-AC	A144	144-Lead Thin Quad Flatpack	Commercial
VIC64-BC	B144	145-Pin Plastic Pin Grid Array	
VIC64-GC	G145	145-Pin Ceramic Pin Grid Array	
VIC64-NC	N160	160-Lead Plastic Quad Flatpack	
VIC64-GI	G145	145-Pin Pin Grid Array	Industrial
VIC64-GM	G145	145-Pin Ceramic Pin Grid Array	Military Temp. Commercial
VIC64-GMB	G145	145-Pin Ceramic Pin Grid Array	MIL-STD-883
VIC64-UMB	U162	160-Lead Ceramic Quad Flatpack	MIL-STD-883
VIC64-UM	U162	160-Lead Ceramic Quad Flatpack	Military Temp. Commercial

Document #: 38-00196-B

The VIC64 is also capable of generating local interrupts on certain error or status conditions. These include:

- ACFAIL* asserted
- SYSFAIL* asserted
- Failed master write-post (BERR* asserted)
- Local DMA completion for block transfers
- Arbitration timeout
- VMEbus interrupter interrupt

The VIC64 can also interrupt on the setting of a module or global switch in the interprocessor communication facilities.

Interprocessor Communication Facilities

The VIC64 includes interprocessor registers and switches that can be written and read through VMEbus accesses. These are the only such registers that are directly accessible from the VMEbus. Included in the interprocessor communication facilities are:

- Four general-purpose 8-bit registers
- Four module switches
- Four global switches
- VIC64 version/revision register (read-only)
- VIC64 reset/halt condition (read-only)
- VIC64 interprocessor communication register semaphores

When set through a VMEbus access, these switches can interrupt a local resource. The VIC64 includes module switches that are intended for a single module, and global switches which are intended to be used as a broadcast.

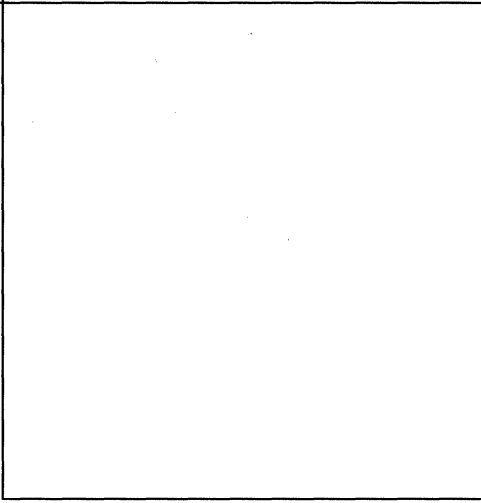
Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	-40°C to +85°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

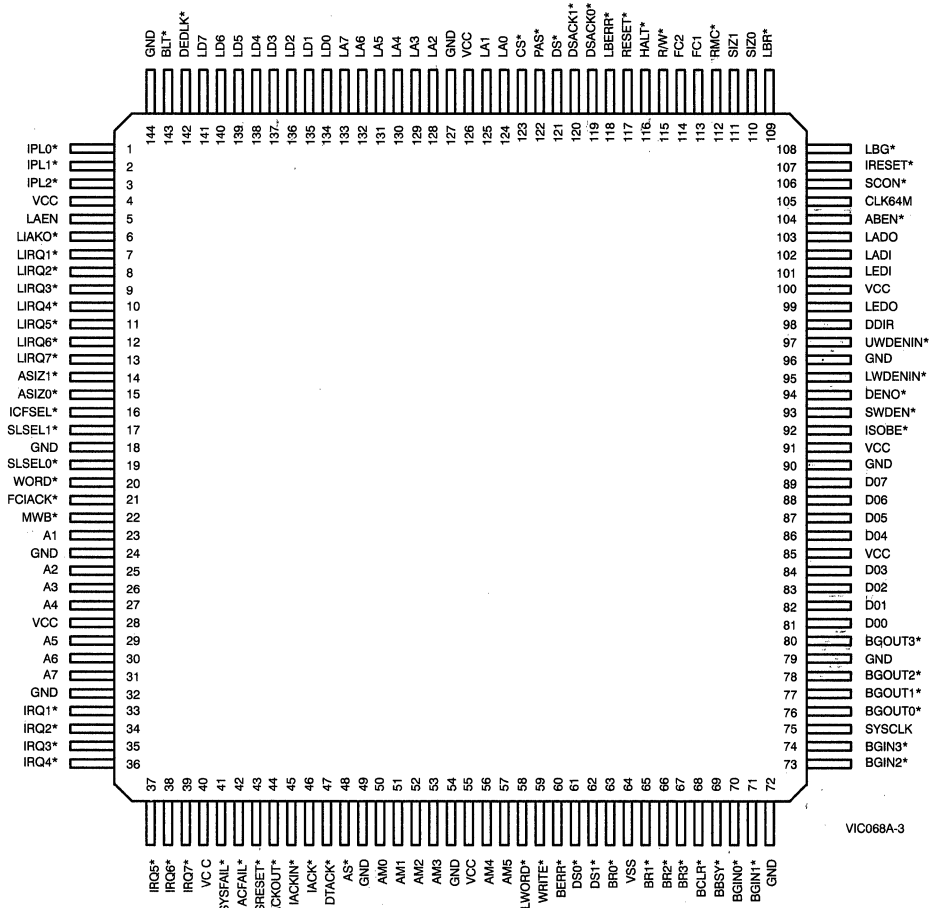
Related Documents

VIC64/CY7C964 Design Notes
VIC068A/VAC068A User's Guide

Pin Configurations
**Pin Grid Array (PGA)
Bottom View**

A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
GND	IPL2*	LIACKO*	LIRQ2*	LIRQ5*	ASIZ1	ASIZ0	SLSEL1*	WORD*	FIACK*	A02	A04	VCC	GND	IRQ4*	1
LD6	BLT*	IPL1*	VCC	LIRQ1*	LIRQ4*	LIRQ6*	ICFSEL*	MWB*	A01	A03	A05	A07	IRQ3*	IRQ7*	2
LD2	LD5	DEDLK*	IPL0*	LAEN	LIRQ3*	LIRQ7*	GND	SLSEL0*	GND	A06	IRQ1*	IRQ2*	IRQ6*	ACFAIL*	3
LD1	LD3	LD7	LOCATOR PIN									IRQ5*	VCC	IACKOUT*	4
LA7	LD0	LD4										SYSFAIL*	SYSRESET*	DTACK*	5
LA3	LA5	LA6										IACKIN*	IACK*	AM0	6
LA2	LA4	GND										GND	AS*	AM1	7
LA1	LA0	VCC										GND	AM2	AM3	8
CS*	DSACK1*	DS*										VCC	LWORD*	AM4	9
PAS*	LBERR*	RESET*										BERR*	WRITE*	AM5	10
DSACK0*	R/W*	FC1										BR2*	DS1*	DS0*	11
HALT*	RMC*	LBR*										BBSY*	BR1*	BR0*	12
FC2	SIZ0	SCON*	CLK64M									LADI	GND	VCC	GND
SIZ1	IRESET*	LADO	LEDI	DDIR	LWDENIN*	DENO*	D06	D03	D01	GND	BGOUT0*	BGIN3*	BGIN1*	BCLR*	14
LBG*	ABEN*	VCC	LEDO	UWDENIN*	SWDEN*	ISOBE*	D07	D05	D04	D02	BGOUT3*	BGOUT2*	SYSCLK	GND	15

VIC068A-1

Pin Configurations (continued)
144-Pin Thin Quad Flatpack (TQFP)
Top View


VIC068A-3

Theory of Operation

The VIC068A is an interface between a local CPU bus and the VMEbus. The local bus interface of the VIC068A emulates Motorola's family of 32-bit CISC processor interfaces. Other processors can easily be adapted to interface to the VIC068A using the appropriate logic.

Resetting the VIC068A

The VIC068A can be reset by any of three distinct reset conditions:

Internal Reset. This reset is the most common means of resetting the VIC068A. It resets select register values and all logic within the device.

System Reset. This reset provides a means of resetting the VIC068A through the VMEbus backplane. The VIC068A may also signal a SYSRESET* by writing a configuration register.

Global Reset. This provides a complete reset of the VIC068A. This reset resets all of the VIC068A's configuration registers. This reset should be used with caution since SYSCLK is not driven while a global reset is in progress.

All three reset options are implemented in a different manner and have different effects on the VIC068A configuration registers.

VIC068A VMEbus System Controller

The VIC068A is capable of operating as the VMEbus system controller. It provides VMEbus arbitration functions, including:

- Priority, round-robin, and single-level arbitration schemes
- Driving IACK* Daisy-Chain
- Driving BGIOUT* Daisy-Chain (All four levels)
- Driving SYSCLK output
- VMEbus arbitration timeout timer

The System controller functions are enabled by the SCON* pin of the VIC068A. When strapped LOW, the VIC068A functions as the VMEbus system controller.

VIC068A VMEbus Master Cycles

The VIC068A is capable of becoming the VMEbus master in response to a request from local resources. In this situation, the local resource requests that a VMEbus transfer is desired. The VIC068A makes a request for the VMEbus. When the VMEbus is granted to the VIC068A, it then performs the transfer and acknowledges the local resource and the cycle is complete. The VIC068A is capable of all four VMEbus request levels. The following release modes are supported:

- Release on request (ROR)
- Release when done (RWD)
- Release on clear (ROC)
- Release under RMC* control
- Bus capture and hold (BCAP)

The VIC068A supports A32, A24, and A16, as well as user-defined address spaces.

Master Write-Posting

The VIC068A is capable of performing master write-posting (bus decoupling). In this situation, the VIC068A acknowledges the local resource *immediately* after the request to the VIC068A is made, thus freeing the local bus. The VIC068A latches the local data to be written and performs the VMEbus transfer without the local resource having to wait for VMEbus arbitration.

Indivisible Cycles

Read-modify-write cycles and indivisible multiple-address cycles (IMACs) are easily performed using the VIC068A. Significant control is allowed to:

- Requesting the VMEbus on the assertion of RMC* independent of MWB* (this prevents any slave access from interrupting local indivisible cycles)
- Stretching the VMEbus AS*
- Making the above behaviors dependent on the local SIZi signals

Deadlock Condition

If a master operation is attempted when a slave operation to the same module is in progress, a deadlock condition has occurred. The VIC068A will signal a deadlock condition by asserting the DEDLK* signal. This should be used by the local resource requesting the VMEbus to try the transfer after the slave access has completed.

Self-Access Condition

If the VIC068A, while it is VMEbus master, has a slave select signaled, a self access is said to have occurred. The VIC068A will issue a BERR*, which in turn will cause a LBERR* to be asserted.

VIC068A VMEbus Slave Cycles

The VIC068A is capable of operating as a VMEbus slave controller. The VIC068A contains a highly programmable environment to allow for a wide variety of slave configurations. The VIC068A allows for:

- D32, D16, or D8 configuration
- A32, A24, A16, or user-defined address spaces
- Programmable block transfer support including:
 - DMA-type block transfer (PAS* and DSACKi* held asserted)
 - non-DMA-type block transfer (toggle PAS* and DSACKi*)
 - No support for block transfer
- Programmable data acquisition delays
- Programmable PAS* and DS* timing
- Restricted slave accesses (supervisory accesses only)

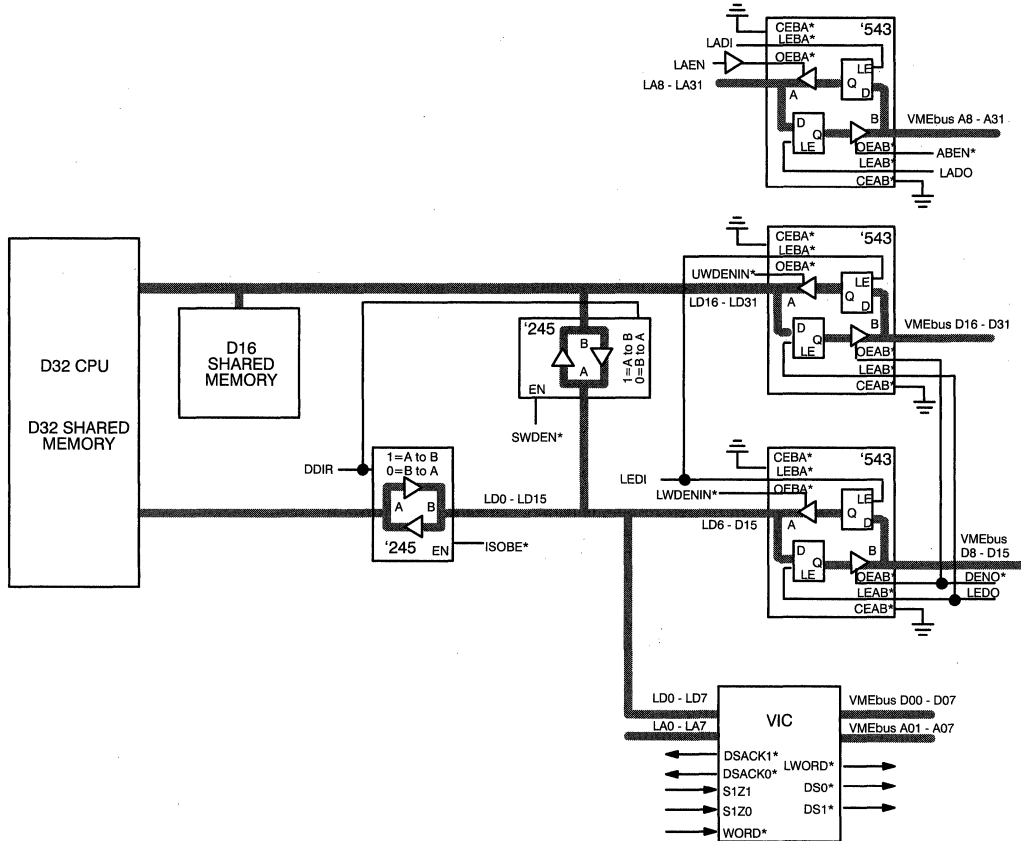
When a slave access is required, the VIC068A will request the local bus. When local bus mastership is obtained, the VIC068A will read or write the data to/from the local resource and assert the DTACK* signal to complete the transfer.

Slave Write-Posting

The VIC068A is capable of performing a slave write-post operation (bus decoupling). When enabled, the VIC068A latches the data to be written and acknowledge the VMEbus (asserts DTACK*) immediately thereafter. This prevents the VMEbus from having to wait for local bus access.

Address Modifier (AM) Codes

The VIC068A encodes and decodes the VMEbus address modifier codes. For VMEbus master accesses, the VIC068A encodes the appropriate AM codes through the VIC068A FCi and ASIZi signals, as well as the block transfer status. For slave accesses, the VIC068A decodes the AM codes and checks the slave select control registers to see if the slave request is to be supported with regard to address spaces, supervisory accesses, and block transfers. The VIC068A also supports user-defined AM codes; that is, the

Buffer Control Signal for Shared Memory Implementation^[1]

Note:

1. This configuration can support Slave Block Transfers and Master and Slave Write-Post Operation. This buffer configuration cannot support block transfers with DMA.

VMEbus Address Controller

Features

- Optional companion part to VIC068A
- Implements master/slave VMEbus interface in conjunction with the VIC068A
- Complete VMEbus and I/O DMA capability for a 32-bit CPU
- Complete local and VMEbus memory map decoding
 - Separate segments on local side available for DRAM, VME subsystem bus (VSB), shared resources, VMEbus, local I/O, and EPROM
 - Separate segments for the VMEbus address decode for slave select 0, slave select 1, and interprocessor communication facilities
 - 64-Kbyte resolution for both local and VMEbus memory maps
- Supports block transfers over 256 byte boundaries
 - Address counters for both VMEbus A(31-8) and local LA(31-8)
 - Supports dual-path mode
 - Supports implementation of VSB interface with DMA capability

- Dual UART channels on board
 - Double-buffered on transmit, quint-buffered on receive
 - Baud rate programmable
- Miscellaneous features
 - Pin grid array or quad flatpack packages
 - Supports unaligned transfers
 - Programmable DSACKi for local I/O
 - Programmable timer and interrupt controller
 - Programmable I/O (PIO)
- See the *VIC068A/VAC068A User's Guide* for more information

Functional Description

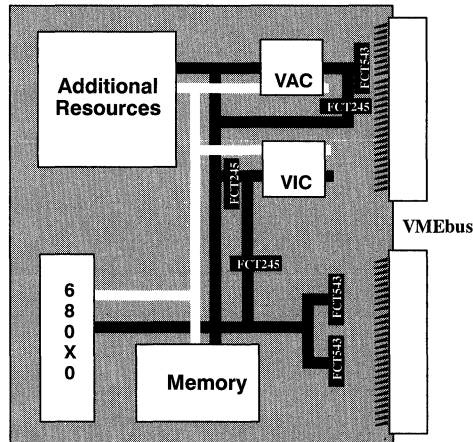
The VMEbus address controller (VAC068A) is a programmable memory map address controller. In conjunction with the VIC068A (VMEbus interface controller), the VAC068A maximizes the VMEbus interface performance of a master/slave module.

The VAC068A contains programmable registers to allow the user to easily define memory maps for both the local and VMEbus address regions. The VAC068A also contains the address counters and handshaking signals to allow easy implementation of block-level transfers over 256-byte boundaries. Additional features include dual internal UART channels, redirection control on the local bus to VSB (VME subsystem bus) or shared resource area, data swapping for unaligned transfers, programmable DSACKi, programmable timer and interrupt controller.

The VAC068A connects directly to the local bus and the VIC068A. VMEbus address lines A8 through A31 are driven directly. The VAC068A output drivers feature patented high-drive outputs and TTL-compatible inputs.

The VAC068A is available in pin grid array (with 122 active signals, 22 power and ground pins, and 1 locator pin) and quad flatpack.

Sample Board Design

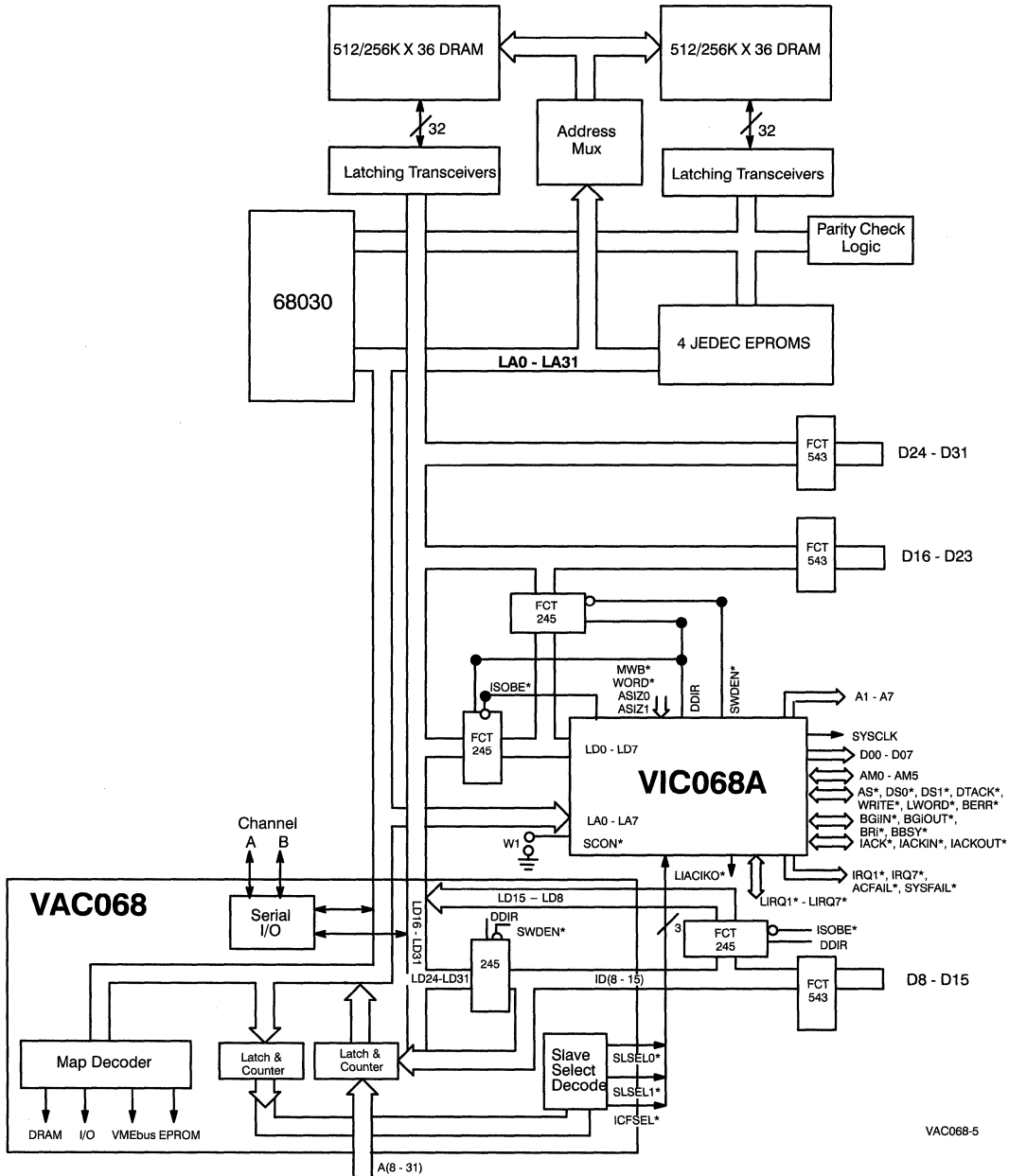


VAC068-1

Pin Configurations
**Pin Grid Array (PGA)
Bottom View**

A	B	C	D	E	F	G	H	J	K	L	M	N	P	R		
A23	PIO13/ IOSEL2*	DDIR	PIO11	LADI	BLT*	REFGT*	ICFSEL*	SLSEL1*	ID8	ID11	ID13	ID14	ASIZ0	FC1	1	
A20	A22	SWDEN*	VAS*	ABEN*	PIO4/ IORD*	VSBSEL*	SLSEL0*	ID10	ID9	ID12	WORD*	FCIACK*	FC0	PAS*	2	
A17	A19	A21	LADO	LDMACK*	GND	LBR*	VCC	GND	GND	ID15	ASIZ1	CPUCLK	LAEN	DSACK1*	3	
A16	A18	GND	LOCATOR PIN	<div style="border: 1px solid black; width: 100%; height: 100%;"></div>									FC2	R/W*	LD19	4
A14	A15	VCC											VCC	DSACK0*	LD21	5
A12	A13	GND											GND	LD16	LD17	6
A10	A11	VCC											LD23	LD18	LD20	7
A08	A09	GND											LD24	LD22	LD25	8
A25	A24	VCC											GND	LD27	LD26	9
A27	A26	GND											VCC	LD29	LD28	10
A29	A28	PIO0/ TXDA											DRAMCS*	LD31	LD30	11
A31	PIO1/ RXDA	PIO5/ IOWR*											GND	EPROMCS*	MWB*	12
A30	PIO3/ RXDB	PIO7	PIO8/ IOSEL4*									GND	LA29	GND	VCC	VCC
PIO2/ TXDB	PIO6/ IOSEL3*	PIO10	CS*	LA31	LA26	LA24	LA22	IOSEL1*	LA17	LA15	LA14	LA12	LA8	RESET*	14	
VCC	PIO9/ IOSEL5*	LA30	PIO12/ SHRCS*	LA28	LA27	LA25	LA23	LA21	LA19	LA20	LA18	LA16	LA10	IOSEL0*	15	

VAC068-3

VIC068A/VAC068A on 68030 Board


VAC068-5

Slave VMEbus Interface Controller Family

Features

- 80 Mbyte per second block transfer rates
- All VME64 transactions provided, including A64/D64, A40/MD32 transfers
- Auto Slot ID
- CR/CSR space
- All standard (rev C) VMEbus transactions implemented
- VMEbus Interrupter
- No local CPU required
- Programmable from VMEbus or serial PROM
- DRAM controller, including refresh

- On-chip DMA controller (CY7C961)
- Local I/O controller
- Flexible VMEbus address scheme
- User-configured VMEbus response
- 64-pin TQFP, 10x10mm (CY7C960)
- 100-pin TQFP, 14x14mm (CY7C961)

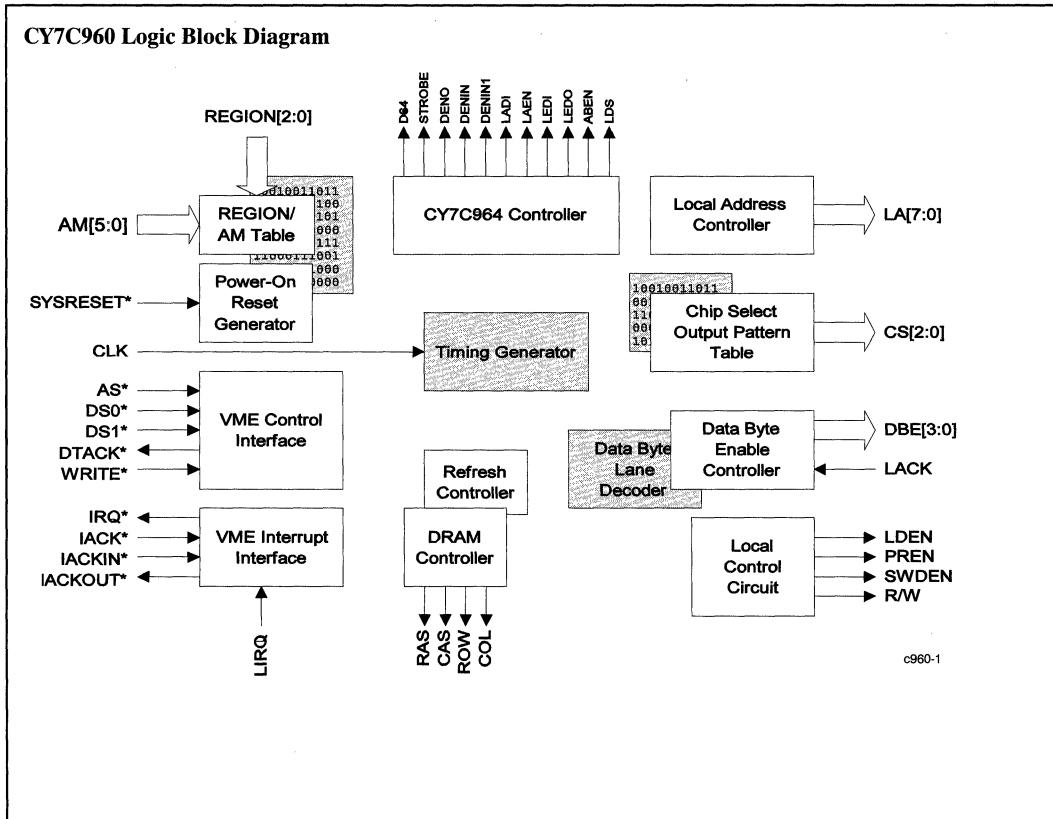
Functional Description

The CY7C960 Slave VMEbus Interface Controller provides the board designer with an integrated, full-featured VME64 interface. This 64-pin device can be programmed to handle every transaction defined in the VME64 specification. The CY7C961 is based upon the CY7C960; additional features include Remote Mas-

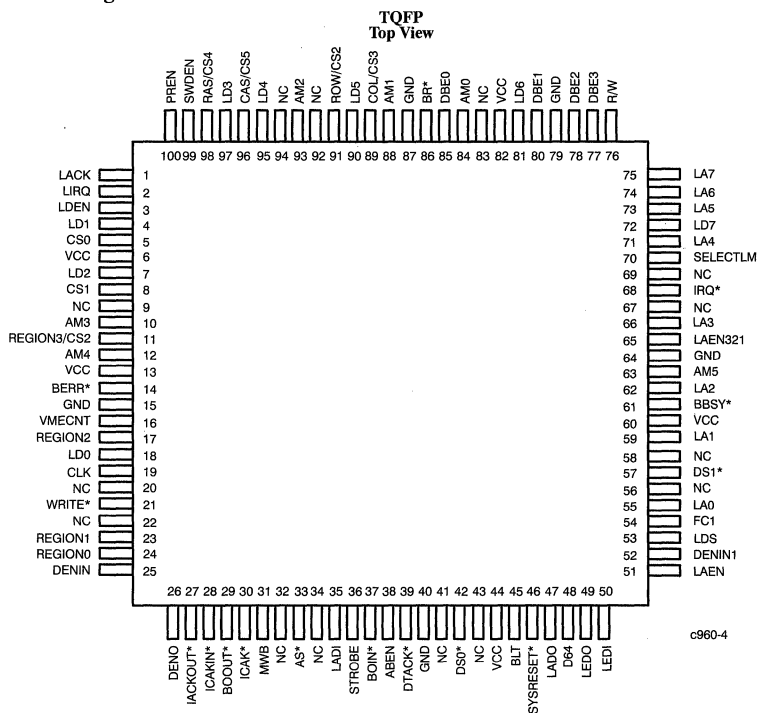
ter capability whereby the CY7C961 can be commanded to move data as a VMEbus master. The CY7C961 is packaged in a 100-pin outline.

The CY7C960 contains all the circuitry needed to control large DRAM arrays and local I/O circuitry without the intervention of a local CPU. There are no registers to read or write, no complex command blocks to be constructed in memory. The CY7C960 simply fetches its own configuration parameters during the power-on reset period. After reset the CY7C960 responds appropriately to VMEbus activity and controls local circuitry transparently.

CY7C960 Logic Block Diagram



c960-1

CY7C961 Pin Configuration

Functional Description (continued)

The CY7C960 controls a bridge between the VMEbus and local DRAM and I/O. Once programmed, the CY7C960 provides activities such as DRAM refresh and local I/O handshaking in a manner that requires no additional local circuitry. The VMEbus control signals are connected directly to the CY7C960. The VMEbus address and data signals are connected to companion address/data transceivers which are controlled by the CY7C960. The CY7C964 VMEbus Interface Logic Circuit is an ideal companion device: the CY7C964 provides a slice of data and address logic that has been optimized for VME64 transactions. In addition to providing the specified drive strength and timing for VME64 transactions, the CY7C964 contains all the circuitry needed to multiplex the address/data bus for multiplexed VMEbus transactions. It contains counters and latches needed during BLT operations. And it also contains address comparators which can be used in the board's Slave Address Decoder. For a 6U or 9U application, four CY7C964 devices are controlled by a single CY7C960. For 3U applications, the CY7C960 controls two CY7C964 devices and an address latch.

The design of the CY7C960 makes it unnecessary to know the details of the VMEbus transaction timing and protocol. The complex VMEbus activities are translated by CY7C960 to simple local cycles involving a few familiar control signals. Similarly, it is not necessary to understand the operation of the companion device, CY7C964: all control sequences for the part are generated

automatically by the CY7C960 in response to VMEbus or local activity. If more information is desired, consult the CY7C964 chapter in the *VIC64 Design Notes* (available separately).

VMEbus transactions supported by the CY7C960 include D8, D16, D32 (incl. UAT), MD32, D64, A16, A24, A32, A40, A64 single-cycle and block-transfer reads and writes, Read-Modify-Write cycles (incl. multiplexed), and Address-only (with or without Handshake). The CY7C960 functions as a VMEbus Interrupter, and supports the new Auto Slot ID standard and CR/CSR space. The CY7C960 also handles LOCK cycles, although full LOCK support is not possible within the constraints of the CY7C960 pinout. Full LOCK support is provided by the CY7C961.

On the local side, no CPU is needed to program the CY7C960, nor to manage transactions. All programmable parameters are initialized through the use of either the VMEbus or a serial PROM. As the CY7C960 incorporates a reliable power-on reset circuit, parameters are self-loaded by the device at power-up or after a system reset. If the VMEbus is used to provide parameters, a VMEbus Master provides the programming information using a protocol, described in the User's Guide, which is compliant with the Auto Slot ID protocol from the new VME64 specification.

To assist in generating the configuration file, a Windows-based program is available which guides the user through the process of

Related Documents*CY7C960 Family User's Guide***Ordering Information**

Ordering Code	Package Name	Package Type	Operating Range
CY7C960-AC	A64	10x10 mm body Plastic Thin Quad Flat Pack	Commercial
CY7C960-NC	N65	14x14 mm body Plastic Quad Flat Pack	

Ordering Code	Package Name	Package Type	Operating Range
CY7C961-NC	A100	14x14 mm body Plastic Thin Quad Flat Pack	Commercial

Document #: 38-00250



FCT Logic Products
Page Number

Parameter Measurement Information		9-1
Device	Description	
CY29FCT52T	8-Bit Registered Transceiver	9-6
CY29FCT520T	Multi-Level Pipeline Register	9-12
CY29FCT818T	Diagnostic Scan Register	9-17
CY54/74FCT138T	1-of-8 Decoder	9-23
CY54/74FCT157T	Quad 2-Input Multiplexer	9-27
CY54/74FCT158T	Quad 2-Input Multiplexer	9-27
CY54/74FCT163T	4-Bit Binary Counter	9-33
CY54/74FCT191T	4-Bit Up/Down Binary Counter	9-38
CY54/74FCT240T	8-Bit Buffer/Line Driver	9-44
CY54/74FCT244T	8-Bit Buffer/Line Driver	9-44
CY54/74FCT245T	8-Bit Transceiver	9-49
CY54/74FCT257T	Quad 2-Input Multiplexer	9-54
CY54/74FCT273T	8-Bit Register	9-59
CY54/74FCT373T	8-Bit Latch	9-64
CY54/74FCT573T	8-Bit Latch	9-64
CY54/74FCT374T	8-Bit Register	9-69
CY54/74FCT574T	8-Bit Register	9-69
CY54/74FCT377T	8-Bit Register	9-74
CY54/74FCT399T	Quad 2-Input Register	9-79
CY54/74FCT480T	Dual 8-Bit Parity Generator/Checker	9-84
CY54/74FCT540T	8-Bit Buffer/Line Driver	9-89
CY54/74FCT541T	8-Bit Buffer/Line Driver	9-89
CY54/74FCT543T	8-Bit Latched Registered Transceiver	9-94
CY54/74FCT646T	8-Bit Registered Transceiver	9-100
CY54/74FCT648T	8-Bit Registered Transceiver	9-100
CY54/74FCT652T	8-Bit Registered Transceiver	9-106
CY54/74FCT821T	8-Bit Bus Interface Register	9-112
CY54/74FCT823T	9-Bit Bus Interface Register	9-112
CY54/74FCT825T	10-Bit Bus Interface Register	9-112
CY54/74FCT827T	10-Bit Buffer	9-121
CY54/74FCT841T	10-Bit Latch	9-126
CY54/74FCT2240T	8-Bit Buffer/Line Driver	9-133
CY54/74FCT2244T	8-Bit Buffer/Line Driver	9-133
CY54/74FCT2245T	8-Bit Transceiver	9-138
CY54/74FCT2257T	Quad 2-Input Multiplexer	9-142
CY54/74FCT2373T	8-Bit Latch	9-146
CY54/74FCT2573T	8-Bit Latch	9-146
CY54/74FCT2374T	8-Bit Register	9-151
CY54/74FCT2574T	8-Bit Register	9-151
CY54/74FCT2541T	8-Bit Buffer/Line Driver	9-156
CY54/74FCT2543T	8-Bit Latched Transceiver	9-160
CY54/74FCT2646T	8-Bit Registered Transceiver	9-166
CY54/74FCT2648T	8-Bit Registered Transceiver	9-166
CY54/74FCT2652T	8-Bit Registered Transceiver	9-172
CY54/74FCT2827T	10-Bit Buffer	9-179
CY74FCT16240T	16-Bit Buffer/Line Driver	9-184
CY74FCT162240T	16-Bit Buffer/Line Driver	9-184
CY74FCT16244T	16-Bit Buffer/Line Driver	9-188
CY74FCT162244T	16-Bit Buffer/Line Driver	9-188
CY74FCT16444T	16-Bit Buffer/Line Driver	9-188



Power Specifications

Cypress logic devices do not use a substrate bias generator. As a result, the quiescent or standby current is typically a few microamperes when the voltage at the inputs are either less than 0.2V or greater than $V_{CC}-0.2V$. On the datasheet this current is described as Quiescent Power Supply Current, given the symbol I_{CC} , and specified on a per IC basis. No inputs are switching and all outputs are open, and if possible, disabled.

When the input signal transitions between the logic levels, both the p-channel pull-up transistor and the n-channel pulldown transistor in the input TTL to CMOS translator are partially turned on, which creates a low-impedance path between V_{CC} and ground. On the datasheet this current is described as “Quiescent Power Supply Current (TTL inputs),” given the symbol ΔI_{CC} , and specified on a per input basis. One input is at $V_{IN}=3.4V$ and other inputs at either V_{CC} or 0 Volts, and all outputs are open, and if possible, disabled.

The Dynamic Power Supply Current, given the symbol I_{CCD} , is not measured directly, but is provided so that the user can calculate total current. It is specified in mA per Megahertz at 50% duty cycle, with one input toggling and one output toggling (enabled) but open (unloaded).

Note that the preceding three currents are specified with the outputs open. The AC CVf current required to charge and discharge parasitic capacitances (e.g., other inputs being driven by the outputs), as well as any DC load currents must be calculated separately.

Total supply current, I_C , is specified on the data sheet for several different conditions. The inputs are switched between ground and either TTL (3.4V) or CMOS ($V_{CC}-0.2V$) levels with rise and fall times of 2.5 ns. Slow rise and fall times can cause the dynamic current to increase, because the input signals are within the transition region for longer times. A characterization curve of normalized ($I_{CC}/\Delta I_{CC}$) currents versus V_{IN} is shown in *Figure 14*.

Total device current can be estimated by using the following formula to calculate the total current. This equation implies

calculating the current associated with each input and adding them up. The same procedure must be followed to calculate the CVf current required to charge and discharge the load capacitances.

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_n N_n)$$

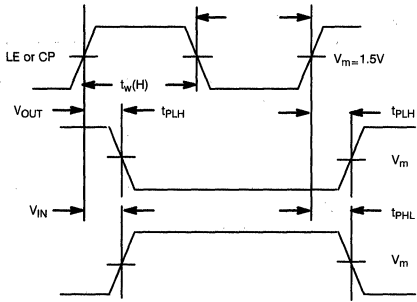
Where:

- I_{CC} = Quiescent Current
- I_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4 V$)
- D_H = Duty Cycle for TTL inputs HIGH
- N_T = Number of TTL inputs at D_H
- I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
- f_{CP} = Clock frequency for registered devices, otherwise zero
- f_n = Input signal frequency
- N_n = Number of inputs changing at F_n

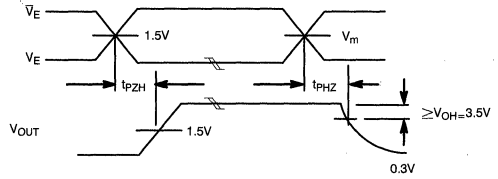
ESD (Electrostatic Discharge)
Precautions

Large electrical fields can damage the thin gate oxides of MOS transistors. Special input protection circuits are used at every input pin of all Cypress products to provide protection against ESD. This circuitry has been designed to withstand repeated applications of high voltages without failure or performance degradation. This is accomplished by preventing the high voltage (ESD) from reaching the thin gate oxides of the internal transistors. For a description of the ESD protection circuit and an explanation of its operation, please see the application note titled “Input/Output Characteristics of Cypress Circuits” in the *Cypress Applications Handbook*.

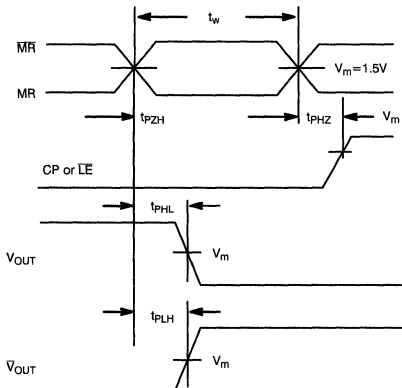
Precautions should be taken by persons handling CMOS devices. It is recommended that individuals wear a grounded wrist strap or ankle strap when handling Cypress FCT-T devices.



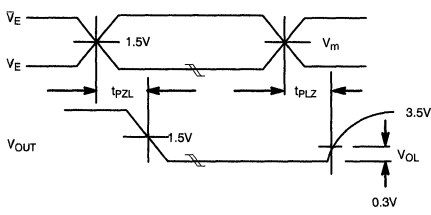
Paran-6

Figure 5. Propagation Delays from Rising-Edge Clock or Enable


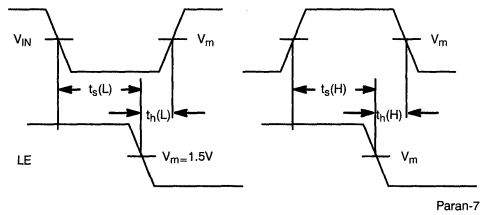
Paran-5

Figure 8. Three-State Output HIGH Enable and Disable Times


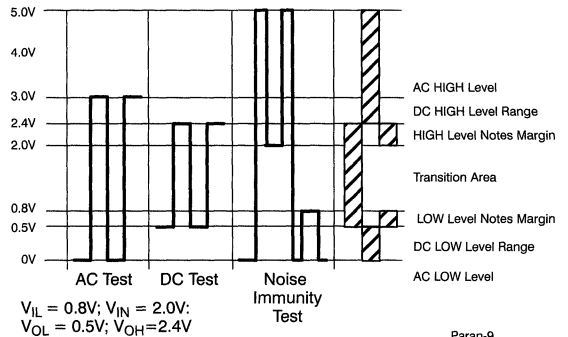
Paran-10

Figure 6. Asynchronous Reset, Active Rising-Edge Clock or Active LOW Enable


Paran-8

Figure 7. Three-State Output LOW Enable and Disable Times


Paran-7

Figure 9. Set-Up and Hold Times to Active HIGH Enable or Parallel Load


Paran-9

Figure 10. Input Signal Levels

8-Bit Registered Transceiver

Features

- Function, pinout, and drive compatible with FCT, F Logic and AM2952
- FCT-C speed at 6.3 ns max. (Com'l)
FCT-B speed at 7.5 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- ESD > 2000V

- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Sink Current **64 mA (Com'l),
48 mA (Mil)**
Source Current **32 mA (Com'l),
12 mA (Mil)**

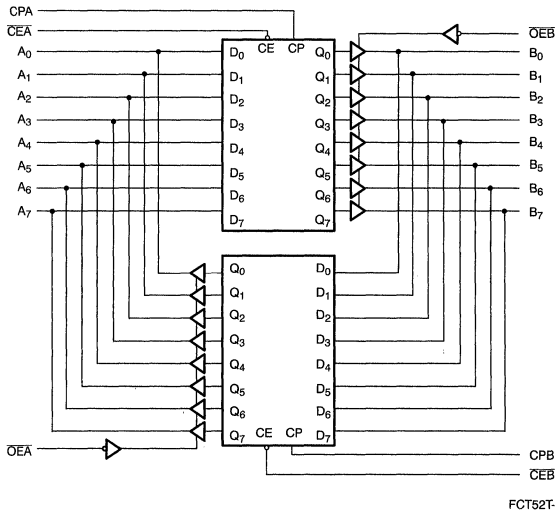
both directions between two bidirectional buses. Separate clock, clock enable, and three-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64 mA.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

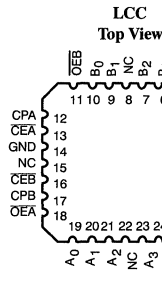
Functional Description

The CY29FCT52T has two 8-bit back-to-back registers that store data flowing in

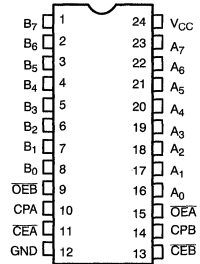
Logic Block Diagram



Pin Configurations



DIP/SOIC/QSOP Top View



Function Table^[1]

Inputs			Internal Q	Function
D	CP	\overline{CE}		
X	X	H	NC	Hold Data
L	\lceil	L	L	Load Data
H	\lceil	L	H	

Note:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.

Output Control

\overline{OE}	Internal Q	Y-Outputs	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} = -32 mA	Com'l	2.0			V
		V _{CC} =Min., I _{OH} = -15 mA	Com'l	2.4	3.3		V
		V _{CC} =Min., I _{OH} = -12 mA	Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =48mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage			2.0			V
V _{IL}	Input LOW Voltage					0.8	V
V _H	Hysteresis ^[6]	All inputs			0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} = -18 mA			-0.7	-1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}				5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V				±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V				±1	μA
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V		-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V				±1	μA

Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Notes:

- Typical values are at V_{CC}=5.0V, T_A= +25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order

to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range

Parameter	Description	29FCT52AT				29FCT52BT				Unit	Fig. No. ^[13]
		Military		Commercial		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay CPA, CPB to A, B	2.0	11.0	2.0	10.0	2.0	8.0	2.0	7.5	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time OEA or OEB to A or B	1.5	13.0	1.5	10.5	1.5	8.5	1.5	8.0	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time OEA or OEB to A or B	1.5	10.0	1.5	10.0	1.5	8.0	1.5	7.5	ns	1, 7, 8
t _S	Set-Up Time HIGH or LOW, A, B to CPA, CPB	2.5		2.5		2.5		2.5		ns	4
t _H	Hold Time HIGH or LOW, A, B to CPA, CPB	2.0		2.0		1.5		1.5		ns	4
t _S	Set-Up Time HIGH or LOW, CEA, CEB to CPA, CPB	3.0		3.0		3.0		3.0		ns	4
t _H	Hold Time HIGH or LOW, CEA, CEB to CPA, CPB	2.0		2.0		2.0		2.0		ns	4
t _W	Pulse Width, ^[6] HIGH or LOW, CPA or CPB	3.0		3.0		3.0		3.0		ns	5

Parameter	Description	29FCT52CT				Unit	Fig. No. ^[13]
		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay CPA, CPB to A, B	2.0	7.3	2.0	6.3	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time, OEA or OEB to A or B	1.5	8.0	1.5	7.0	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time, OEA or OEB to A or B	1.5	7.5	1.5	6.5	ns	1, 7, 8
t _S	Set-Up Time HIGH or LOW, A, B to CPA, CPB	2.5		2.5		ns	4
t _H	Hold Time HIGH or LOW, A, B to CPA, CPB	1.5		1.5		ns	4
t _S	Set-Up Time HIGH or LOW, CEA, CEB to CPA, CPB	3.0		3.0		ns	4
t _H	Hold Time HIGH or LOW, CEA, CEB to CPA, CPB	2.0		2.0		ns	4
t _W	Pulse Width, ^[6] HIGH or LOW, CPA or CPB	3.0		3.0		ns	5

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
 13. See "Parameter Measurement Information" in the General Information Section.

Multi-Level Pipeline Register

Features

- Function, pinout, and drive compatible with FCT, F Logic, and AM29520
- FCT-C speed at 6.0 ns max. (Com'1)
FCT-B speed at 7.5 ns max. (Com'1)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-Off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- ESD > 2000V

- Sink current 64 mA (Com'1),
32 mA (Mil)
Source current 32 mA (Com'1),
12 mA (Mil)
- Single and dual pipeline operation modes
- Multiplexed data inputs and outputs

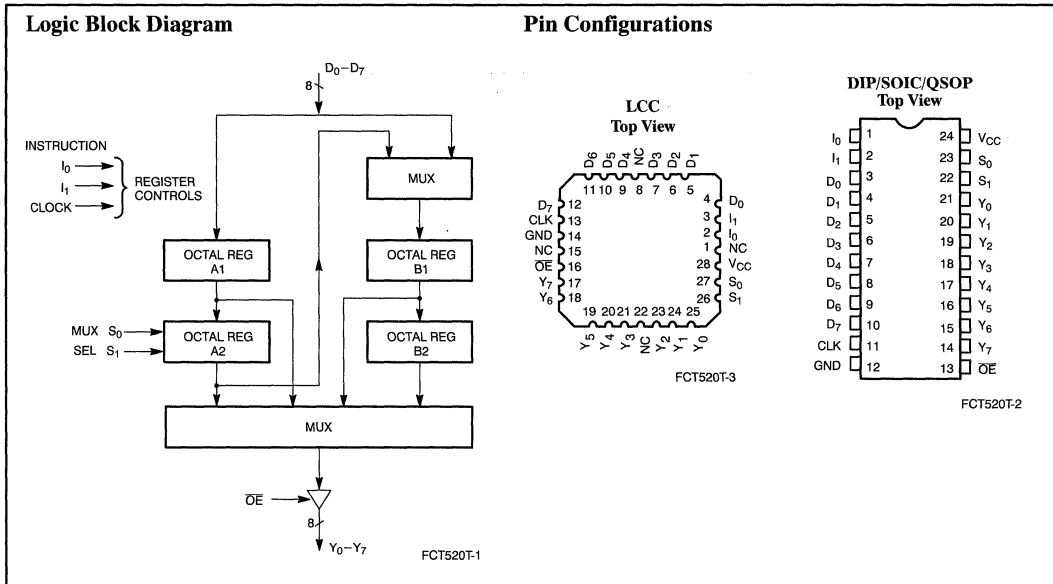
Functional Description

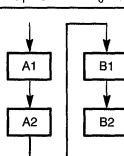
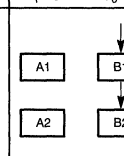
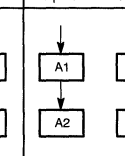
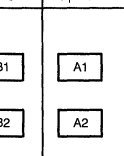
The FCT520T is a multi-level 8-bit-wide pipeline register. The device consists of four registers, A1, A2, B1, and B2, which are configured by the instruction inputs I_0, I_1 as a single 4-level pipeline or as two two-level pipelines. The contents of any register may be read at any time by using the multiplexed output at any time by using the mux-selection controls S_0 and S_1 .

The pipeline register is positive edge triggered and data is shifted by the rising edge of the clock input. Instruction $I=0$ selects the four-level pipeline mode. Instruction $I=1$ selects the two-level B pipeline while $I=2$ selects the two-level A pipeline. $I=3$ is the HOLD instruction; no shifting is performed by the clock in this mode.

In the two-level operation mode, the FCT520T data is shifted from level 1 to level 2 and new data is loaded into level 1.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.


Pipeline Instruction Table

I = 0		I = 1		I = 2		I = 3	
$I_1=0$	$I_0=0$	$I_1=0$	$I_0=1$	$I_1=1$	$I_0=0$	$I_1=1$	$I_0=1$
							
Single four-level		Dual two-level				Hold	

Output Selection Mux Table

Inputs		Output
S_1	S_0	
1	1	A1
1	0	A2
0	1	B1
0	0	B2

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[4]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} \leq 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC} = \text{Max.}, V_{IN} = 3.4V$ ^[7] $f_1 = 0, \text{Outputs Open}$	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ^[8]	$V_{CC} = \text{Max.}, \text{One Input Toggling},$ $50\% \text{ Duty Cycle, Outputs Open},$ $OE = \text{GND},$ $V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current ^[9]	$V_{CC} = \text{Max.}, f_0 = 10 \text{ MHz},$ $50\% \text{ Duty Cycle, Outputs Open},$ $\text{One Bit Toggling at } f_1 = 5 \text{ MHz},$ $OE = \text{GND},$ $V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	0.7	1.4	mA
		$V_{CC} = \text{Max.}, f_0 = 10 \text{ MHz},$ $50\% \text{ Duty Cycle, Outputs Open},$ $\text{One Bit Toggling at } f_1 = 5 \text{ MHz},$ $OE = \text{GND},$ $V_{IN} = 3.4V \text{ or } V_{IN} = \text{GND}$	1.2	3.4	mA
		$V_{CC} = \text{Max.}, f_0 = 10 \text{ MHz},$ $50\% \text{ Duty Cycle, Outputs Open},$ $\text{Eight Bits Toggling at } f_1 = 5 \text{ MHz},$ $OE = \text{GND},$ $V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	2.8	5.6 ^[10]	mA
		$V_{CC} = \text{Max.}, f_0 = 10 \text{ MHz}, 50\% \text{ Duty Cycle},$ $\text{Outputs Open},$ $\text{Eight Bits Toggling at } f_1 = 5 \text{ MHz},$ $OE = \text{GND},$ $V_{IN} = 3.4V \text{ or } V_{IN} = \text{GND}$	5.1	14.3 ^[10]	mA

Notes:

- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_0/2 + f_1 N_1)$
 $I_{CC} = \text{Quiescent Current with CMOS input levels}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL HIGH input}$
 $(V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL inputs HIGH}$

- $N_T = \text{Number of TTL inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current caused by an input transition pair}$
 (HLH or LHL)
 $f_0 = \text{Clock frequency for registered devices, otherwise zero}$
 $f_1 = \text{Input signal frequency}$
 $N_1 = \text{Number of inputs changing at } f_1$
 All currents are in milliamps and all frequencies are in megahertz.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.0	CY29FCT520CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT520CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT520CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.0	CY29FCT520CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT520CTLMB	L64	28-Square Leadless Chip Carrier	
7.5	CY29FCT520BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT520BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT520BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
8.0	CY29FCT520BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT520BTLMB	L64	28-Square Leadless Chip Carrier	
14.0	CY29FCT520ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT520ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT520ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
16.0	CY29FCT520ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT520ATLMB	L64	28-Square Leadless Chip Carrier	

Document #: 38-00274-A

Function Table^[1]

Inputs			Inputs		Shadow Register	Pipeline Register	Operation
MODE	SDI	DCLK	PCLK	SDO			
L	X	┘	X	S ₇	S ₀ ←SDI S _i ←S _{i-1} NA	NA	Serial Shift; D ₇ –D ₀ Output Disabled
L	X	X	┘	S ₇	NA	P _i ←D _i	Load Pipeline Register from Data Input
H	L	┘	X	L	S _i ←Y _i	NA	Load Shadow Register from Y Output
H	H	┘	X	H	Hold	NA	Hold Shadow Register; D ₇ –D ₀ Output Enabled
H	X	X	┘	SDI	NA	P _i ←S _i	Load Pipeline Register from Shadow Register

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–65°C to +135°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Voltage	–0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT, BT	–40°C to +85°C	5V ± 5%
Military ^[4]	All	–55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =–32 mA	Com ¹	2.0			V
		V _{CC} =Min., I _{OH} =–15 mA	Com ¹	2.4	3.3		V
		V _{CC} =Min., I _{OH} =–3 mA	Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com ¹		0.3	0.55	V
		V _{CC} =Min., I _{OL} =20 mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage			2.0			V
V _{IL}	Input LOW Voltage					0.8	V
V _H	Hysteresis ^[6]	All inputs			0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =–18 mA			–0.7	–1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}				5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V				±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V				±1	μA
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} =Max., V _{OUT} =2.7V				10	μA
I _{OZL}	Off State LOW-Level Output Current	V _{CC} =Max., V _{OUT} =0.5V				–10	μA
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V		–60	–120	–225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V				±1	μA

Notes:

1. NA = Not Applicable
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the “instant on” case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.

7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameters tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range^[12]

Parameter	Description	FCT818T				FCT818AT				Unit	Fig. No. ^[14]
		Military		Commercial		Military		Commercial			
		Min. ^[13]	Max.	Min. ^[13]	Max.	Min. ^[13]	Max.	Min. ^[13]	Max.		
t _{PD}	Propagation Delay PCLK to Y		18		13		12		9	ns	5
	MODE to SDO		18		16		18		16	ns	6
	SDI to SDO		18		16		18		15	ns	3
	DCLK to SDO		30		25		30		25	ns	5
t _s	Set-Up Time D to PCLK	10		8		6		4		ns	4
	MODE to PCLK	15		15		15		15		ns	
	Y to DCLK	5		5		5		5		ns	
	MODE to DCLK	12		12		12		12		ns	
	SDI to DCLK	10		10		10		10		ns	
	DCLK to PCLK	15		15		15		15		ns	
	PCLK to DCLK	45		40		45		40		ns	
t _H	Hold Time D to PCLK	2		2		2		2		ns	4
	MODE to PCLK	0		0		0		0		ns	
	Y to DCLK	5		5		5		5		ns	
	MODE to DCLK	5		2		5		2		ns	
	SDI to DCLK	0		0		0		0		ns	
t _{PLZ}	Output Disable Time LOW		20		15		20		15	ns	7
	OE to Y DCLK to D		45		45		45		45	ns	
t _{PHZ}	Output Disable Time HIGH		30		25		30		25	ns	8
	OE to Y DCLK to D		90		85		90		80	ns	
t _{PZL}	Output Enable Time LOW		20		15		20		15	ns	7
	OE to Y DCLK to D		35		30		35		25	ns	
t _{PZH}	Output Enable Time HIGH		20		15		20		15	ns	8
	OE to Y DCLK to D		30		25		30		25	ns	
t _w	Pulse Width PCLK (HIGH and LOW)	15 25		15 25		15 25		10 15		ns ns	5 5

Notes:

12. AC Characteristics guaranteed with C_L = 50 pF as shown in Figure 1 of the "Parameter Measurement Information" in the General Information Section.
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. See "Parameter Measurement Information" in the General Information Section.

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.0	CY29FCT818CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT818CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT818CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.5	CY29FCT818BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT818BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT818BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.6	CY29FCT818CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT818CTLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY29FCT818ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT818ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT818ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
	CY29FCT818BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT818BTLMB	L64	28-Square Leadless Chip Carrier	
12.0	CY29FCT818ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT818ATLMB	L64	28-Square Leadless Chip Carrier	
13.0	CY29FCT818TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT818TQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT818TSOC	S13	24-Lead (300-Mil) Molded SOIC	
18.0	CY29FCT818TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT818TLMB	L64	28-Square Leadless Chip Carrier	

Document #: 38-00275-A

Function Table^[1]

Inputs						Outputs							
\bar{E}_1	\bar{E}_2	E_3	A_0	A_1	A_2	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3	\bar{O}_4	\bar{O}_5	\bar{O}_6	\bar{O}_7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	L	H	L	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

 Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Ambient Temperature with
 Power Applied -65°C to $+135^{\circ}\text{C}$
 Supply Voltage to Ground Potential -0.5V to $+7.0\text{V}$
 DC Input Voltage -0.5V to $+7.0\text{V}$
 DC Output Voltage -0.5V to $+7.0\text{V}$
 DC Output Current (Maximum Sink Current/Pin) 120 mA
 Power Dissipation 0.5W

 Static Discharge Voltage $>2001\text{V}$
 (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 5\%$
Commercial	T, AT	-40°C to $+85^{\circ}\text{C}$	$5\text{V} \pm 5\%$
Military ^[4]	All	-55°C to $+125^{\circ}\text{C}$	$5\text{V} \pm 10\%$

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit	
V_{OH}	Output HIGH Voltage	$V_{CC}=\text{Min.}, I_{OH}=-32\text{ mA}$	Com ¹	2.0		V	
		$V_{CC}=\text{Min.}, I_{OH}=-15\text{ mA}$	Com ¹	2.4	3.3	V	
		$V_{CC}=\text{Min.}, I_{OH}=-12\text{ mA}$	Mil	2.4	3.3	V	
V_{OL}	Output LOW Voltage	$V_{CC}=\text{Min.}, I_{OL}=64\text{ mA}$	Com ¹		0.3	0.55	V
		$V_{CC}=\text{Min.}, I_{OL}=32\text{ mA}$	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0		V	
V_{IL}	Input LOW Voltage				0.8	V	
V_H	Hysteresis ^[6]	All inputs		0.2		V	
V_{IK}	Input Clamp Diode Voltage	$V_{CC}=\text{Min.}, I_{IN}=-18\text{ mA}$		-0.7	-1.2	V	
I_I	Input HIGH Current	$V_{CC}=\text{Max.}, V_{IN}=V_{CC}$			5	μA	
I_{IH}	Input HIGH Current	$V_{CC}=\text{Max.}, V_{IN}=2.7\text{V}$			± 1	μA	
I_{IL}	Input LOW Current	$V_{CC}=\text{Max.}, V_{IN}=0.5\text{V}$			± 1	μA	
I_{OS}	Output Short Circuit Current ^[7]	$V_{CC}=\text{Max.}, V_{OUT}=0.0\text{V}$	-60	-120	-225	mA	
I_{OFF}	Power-Off Disable	$V_{CC}=0\text{V}, V_{OUT}=4.5\text{V}$			± 1	μA	

Notes:

- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at $V_{CC}=5.0\text{V}, T_A=+25^{\circ}\text{C}$ ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT138T				FCT138AT				Unit	Fig. No. ^[12]
		Military		Commercial		Military		Commercial			
		Min. ^[11]	Max.	Min. ^[11]	Max.	Min. ^[11]	Max.	Min. ^[11]	Max.		
t_{PLH} t_{PHL}	Propagation Delay A to \bar{O}	1.5	12.0	1.5	9.0	1.5	7.8	1.5	5.8	ns	1, 2
t_{PLH} t_{PHL}	Propagation Delay \bar{E}_1 or \bar{E}_2 to \bar{O}	1.5	12.5	1.5	9.0	1.5	8.0	1.5	5.9	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay E_3 to \bar{O}	1.5	12.5	1.5	9.0	1.5	8.0	1.5	5.9	ns	1, 5

Parameter	Description	FCT138CT				Unit	Fig. No. ^[12]
		Military		Commercial			
		Min. ^[11]	Max.	Min. ^[11]	Max.		
t_{PLH} t_{PHL}	Propagation Delay A to \bar{O}	1.5	6.0	1.5	5.0	ns	1, 2
t_{PLH} t_{PHL}	Propagation Delay \bar{E}_1 or \bar{E}_2 to \bar{O}	1.5	6.1	1.5	5.0	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay E_3 to \bar{O}	1.5	6.1	1.5	5.0	ns	1, 5

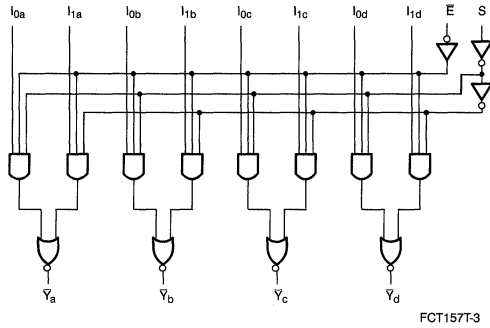
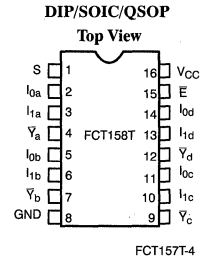
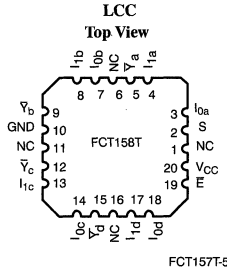
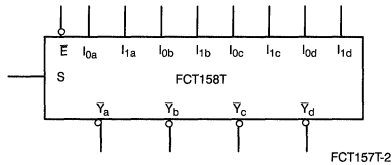
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.0	CY74FCT138CTPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT138CTQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT138CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.8	CY74FCT138ATPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT138ATQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT138ATSOC	S1	16-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT138CTDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT138CTLMB	L61	20-Pin Square Leadless Chip Carrier	
7.8	CY54FCT138ATDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT138ATLMB	L61	20-Pin Square Leadless Chip Carrier	
9.0	CY74FCT138TPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT138TQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT138TSOC	S1	16-Lead (300-Mil) Molded SOIC	
12.0	CY54FCT138TDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT138TLMB	L61	20-Pin Square Leadless Chip Carrier	

Notes:

11. Minimum limits are guaranteed but not tested on Propagation Delays. 12. See "Parameter Measurement Information" in the General Information Section.

Document #: 38-00297-A

Logic Block Diagram, FCT158T

Pin Configurations

Logic Symbol

Pin Description

Name	Description
S	Common Select Input
\bar{E}	Enable Inputs (Active LOW)
I_0	Data Inputs from Source 0
I_1	Data Inputs from Source 1
Y	Non-Inverted Output (FCT157T)
\bar{Y}	Inverted Output (FCT158T)

Function Table^[1]—FCT157T

Inputs				Outputs
\bar{E}	S	I_0	I_1	Y
H	X	X	X	H
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

Function Table^[1]—FCT158T

Inputs				Outputs
\bar{E}	S	I_0	I_1	\bar{Y}
H	X	X	X	H
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

Note:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	0.1	0.2	mA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{CC} =Max., V _{IN} =3.4V ^[8] f ₁ =0, Outputs Open	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.06	0.12	mA/ MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Input Toggling at f ₁ =10 MHz, OE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.7	1.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Input Toggling at f ₁ =10 MHz, OE=GND, V _{IN} =3.4V or V _{IN} =GND	1.0	2.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Four Bits Toggling at f ₁ =2.5 MHz, OE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.7	1.4 ^[11]	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Four Bits Toggling at f ₁ =2.5 MHz, OE=GND, V _{IN} =3.4V or V _{IN} =GND	1.7	5.4 ^[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CCD}_HN_T + I_{CCD}(f₀/2 + f₁N₁)
I_{CC} = Quiescent Current with CMOS input levels
ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
D_H = Duty Cycle for TTL inputs HIGH

- N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
f₀ = Clock frequency for registered devices, otherwise zero
f₁ = Input signal frequency
N₁ = Number of inputs changing at f₁
All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.



Ordering Information—FCT157T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.3	CY74FCT157CTPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT157CTQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT157CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.0	CY74FCT157ATPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT157ATQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT157ATSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.0	CY54FCT157CTDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT157CTLMB	L61	20-Pin Square Leadless Chip Carrier	
5.8	CY54FCT157ATDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT157ATLMB	L61	20-Pin Square Leadless Chip Carrier	
6.0	CY74FCT157TPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT157TQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT157TSOC	S1	16-Lead (300-Mil) Molded SOIC	
7.0	CY54FCT157TDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT157TLMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information—FCT158T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.3	CY74FCT158CTPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT158CTQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT158CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.5	CY74FCT158ATPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT158ATQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT158ATSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.5	CY54FCT158CTDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT158CTLMB	L61	20-Pin Square Leadless Chip Carrier	
6.3	CY54FCT158ATDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT158ATLMB	L61	20-Pin Square Leadless Chip Carrier	
6.5	CY74FCT158TPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT158TQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT158TSOC	S1	16-Lead (300-Mil) Molded SOIC	
7.5	CY54FCT158TDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT158TLMB	L61	20-Pin Square Leadless Chip Carrier	

Document #: 38-00288-A

Function Table^[1]

Inputs				Action on the Rising Clock Edge(s)
SR	PE	CET	CEP	
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Incremental)
H	H	L	X	No Charge (Hold)
H	H	X	L	No Charge (Hold)

Pin Description

Name	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
SR	Synchronous Reset Input (Active LOW)
P	Parallel Data Inputs
PE	Parallel Enable Input (Active LOW)
Q	Flip-Flop Outputs
TC	Terminal Count Output

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +135°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	-40°C to +85°C	5V ± 5%
Military ^[4]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	Com'l	2.0		V	
		V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3	V	
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3	V	
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =32 mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage		2.0			V	
V _{IL}	Input LOW Voltage				0.8	V	
V _H	Hysteresis ^[6]	All inputs		0.2		V	
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V	
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}			5	μA	
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V			±1	μA	
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V			±1	μA	
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V	-60	-120	-225	mA	
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V			±1	μA	

Notes:

- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.

- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT163T				FCT163AT				Unit	Fig. No. ^[13]
		Military		Commercial		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay CP to Q (PE Input HIGH)	2.0	11.5	1.5	11.0	2.0	7.5	1.5	7.2	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay CP to TC (PE Input LOW)	2.0	10.0	1.5	9.5	2.0	6.5	1.5	6.2	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay CP to TC	2.0	16.5	1.5	15.0	2.0	10.8	1.5	9.8	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay CET to TC	1.5	9.0	1.5	8.5	1.5	5.9	1.5	5.5	ns	1, 5
t _S	Set-Up Time, HIGH or LOW P to CP	5.5		4.0		4.5		4.0		ns	4
t _H	Hold Time, HIGH or LOW P to CP	2.0		1.5		2.0		1.5		ns	4
t _{SU}	Set-Up Time HIGH or LOW PE or SR to CP	13.5		9.5		11.5		9.5		ns	4
t _H	Hold Time HIGH or LOW PE or SR to CP	1.5		1.5		1.5		1.5		ns	4
t _{SU}	Set-Up Time HIGH or LOW CEP or CET to CP	13.0		9.5		11.0		9.5		ns	4
t _H	Hold Time HIGH or LOW CEP or CET to CP	0		0		0		0		ns	4
t _W	Clock Pulse Width (Load) HIGH or LOW	5.0		4.0		4.0		4.0		ns	5
t _W	Clock Pulse Width(Count) HIGH or LOW	8.0		6.0		7.0		6.0		ns	5

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.

13. See "Parameter Measurement Information" in the General Information Section.



4-Bit Up/Down Binary Counter

Features

- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 6.2 ns max. (Com'l)
FCT-A speed at 7.8 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- ESD > 2000V

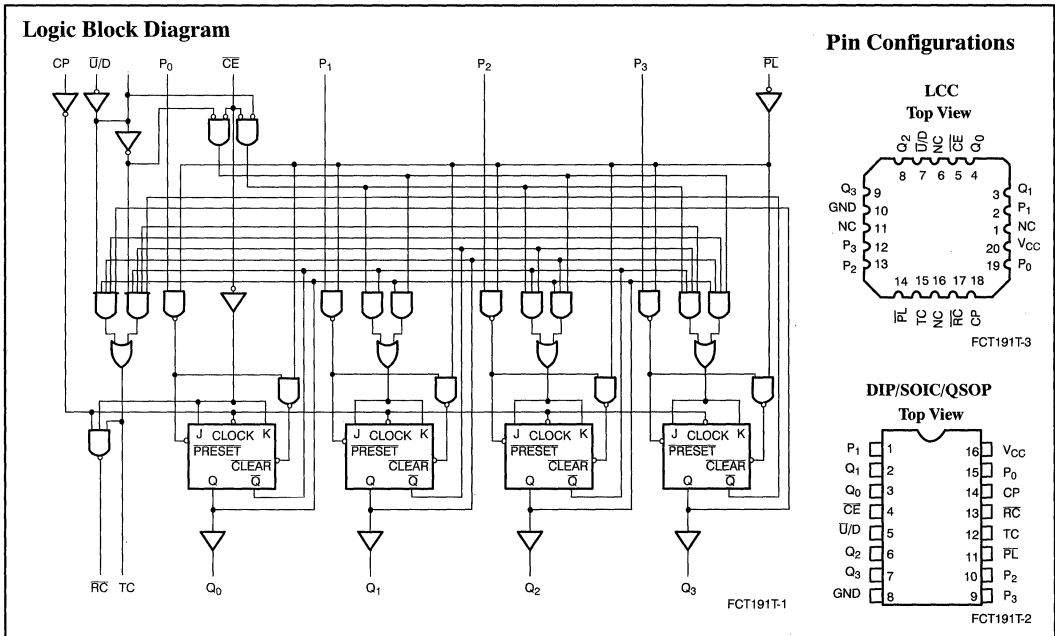
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Sink current 64 mA (Com'l),
 32 mA (Mil)
- Source current 32 mA (Com'l),
 12 mA (Mil)
- Three-State outputs

Functional Description

The FCT191T is a reversible modulo-16 binary counter, featuring synchronous

counting and asynchronous presetting. The preset allows the FCT191T to be used in programmable dividers. The count enable input, terminal count output, and ripple clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.



Pin Description

Name	Description
CE	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
P	Parallel Data Inputs
PL	Asynchronous Parallel Load Input (Active LOW)
U/D	Up/Down Count Control Input
Q	Flip-Flop Outputs
RC	Ripple Clock Output (Active LOW)
TC	Terminal Count Output

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[6]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	0.1	0.2	mA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{CC} =Max., V _{IN} =3.4V, ^[9] f ₁ =0, Outputs Open	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ^[10]	V _{CC} =Max., One Bit Toggling, Preset Mode, 50% Duty Cycle, Outputs Open, MR=V _{CC} =SR, PL=CE=U/D=CP=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.06	0.12	mA/MHz
I _C	Total Power Supply Current ^[11]	V _{CC} =Max., Preset Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =5 MHz, PL=CE=U/D=CP=GND, V _{IN} =V _{CC} , V _{IN} =GND	0.4	0.8	mA
		V _{CC} =Max., Preset Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =5 MHz, V _{IN} =3.4V or V _{IN} =GND	0.7	1.8	mA
		V _{CC} =Max., Preset Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f ₁ =5 MHz, PL=CE=U/D=CP=GND, V _{IN} =V _{CC} , V _{IN} =GND	1.3	2.6 ^[12]	mA
		V _{CC} =Max., Preset Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f ₁ =5 MHz, PL=CE=U/D=CP=GND, V _{IN} =3.4V or V _{IN} =GND	2.3	6.6 ^[12]	mA

Notes:

9. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.

10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

11. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 I_C = I_{CC} + ΔI_{CC}D_HN_T + I_{CCD}(f₀/2 + f₁N₁)
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
 D_H = Duty Cycle for TTL inputs HIGH

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)

f₀ = Clock frequency for registered devices, otherwise zero

f₁ = Input signal frequency

N₁ = Number of inputs changing at f₁

All currents are in milliamps and all frequencies are in megahertz.

12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range (continued)

Parameter	Description	FCT191CT				Unit	Fig. No. ^[14]
		Military		Commercial			
		Min. ^[13]	Max.	Min. ^[13]	Max.		
t _{PLH} t _{PHL}	Propagation Delay CP to Q _n	1.5	8.4	1.5	6.2	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay CP to TC	1.5	9.8	1.5	9.4	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay CP to \overline{RC}	1.5	7.9	1.5	6.8	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay \overline{CE} to \overline{RC}	1.5	6.4	1.5	6.0	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay $\overline{U/D}$ to \overline{RC}	2.5	11.7	1.5	11.0	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay $\overline{U/D}$ to TC	1.5	6.8	1.5	6.1	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay P _n to Q _n	1.5	8.3	1.5	7.7	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay \overline{PL} to Q _n	2.0	7.3	2.0	7.2	ns	1, 5
t _{SU}	Set-Up Time, HIGH or LOW, P _n to \overline{PL}	4.0		3.5			4
t _H	Hold Time, HIGH or LOW, P _n to \overline{PL}	1.5		1.0		ns	4
t _{SU}	Set-Up Time LOW, \overline{CE} to CP	7.6		7.2		ns	4
t _H	Hold Time LOW, \overline{CE} to CP	0		0		ns	4
t _{SU}	Set-Up Time, HIGH or LOW, $\overline{U/D}$ to CP	8.5		8.0		ns	4
t _H	Hold Time, HIGH or LOW, $\overline{U/D}$ to CP	0		0		ns	4
t _w	\overline{PL} Pulse Width LOW	6.0		5.0		ns	5
t _w	Clock Pulse Width ^[6] HIGH or LOW	5.0		4.0		ns	5
t _{REM}	Recovery Time \overline{PL} to CP	5.0		4.5		ns	6



CY54/74FCT240T CY54/74FCT244T

8-Bit Buffers/Line Drivers

Features

- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 4.1 ns max. (Com'l)
FCT-A speed at 4.8 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- ESD > 2000V

- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Sink current 64 mA (Com'l),
48 mA (Mil)
- Source current 32 mA (Com'l),
12 mA (Mil)

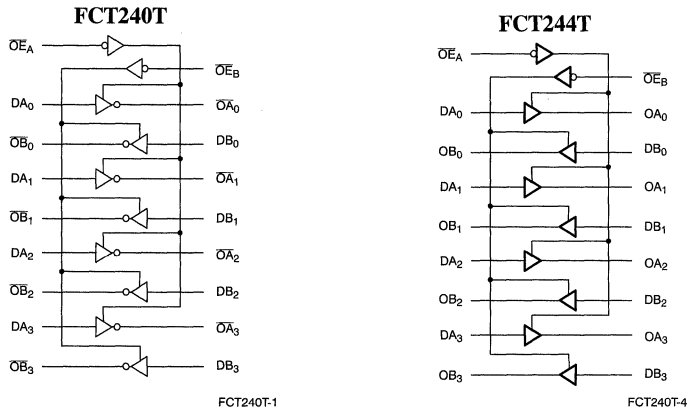
Functional Description

The FCT240T and FCT244T are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers, and bus-oriented

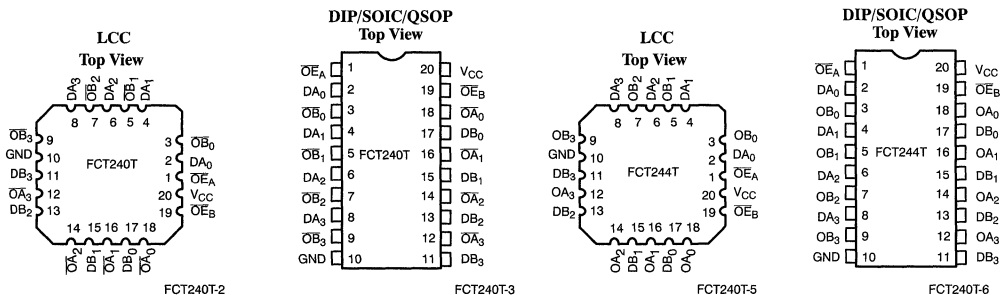
transmitters/receivers. The devices provide speed and drive capabilities equivalent to their fastest bipolar logic counterparts while reducing power consumption. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram



Pin Configurations



Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	0.1	0.2	mA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs)	V _{CC} =Max., V _{IN} =3.4V ^[8] f ₁ =0, Outputs Open	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OE ₁ =OE ₂ =GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.06	0.12	mA/ MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =10 MHz, OE ₁ =OE ₂ =GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.7	1.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =10 MHz, OE ₁ =OE ₂ =GND, V _{IN} =3.4V or V _{IN} =GND	1.0	2.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, OE ₁ =OE ₂ =GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	1.3	2.6 ^[11]	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, OE ₁ =OE ₂ =GND, V _{IN} =3.4V or V _{IN} =GND	3.3	10.6 ^[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC}D_HN_T + I_{CCD}(f₀/2 + f₁N₁)
I_{CC} = Quiescent Current with CMOS input levels
ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
D_H = Duty Cycle for TTL inputs HIGH

- N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
f₀ = Clock frequency for registered devices, otherwise zero
f₁ = Input signal frequency
N₁ = Number of inputs changing at f₁
All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.



Ordering Information—FCT240T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.6	CY74FCT240DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT240DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.3	CY74FCT240CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT240CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
	CY74FCT240CTQC	Q5	20-Lead (150-Mil) QSOP	
4.7	CY54FCT240CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT240CTLMB	L61	20-Pin Square Leadless Chip Carrier	
4.8	CY74FCT240ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT240ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
	CY74FCT240ATQC	Q5	20-Lead (150-Mil) QSOP	
5.1	CY54FCT240ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT240ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.0	CY74FCT240TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT240TSOC	S5	20-Lead (300-Mil) Molded SOIC	
	CY74FCT240TQC	Q5	20-Lead (150-Mil) QSOP	
9.0	CY54FCT240TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT240TLMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information—FCT244T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.6	CY74FCT244DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT244DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.1	CY74FCT244CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT244CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
	CY74FCT244CTQC	Q5	20-Lead (150-Mil) QSOP	
4.6	CY54FCT244CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT244CTLMB	L61	20-Pin Square Leadless Chip Carrier	
4.6	CY74FCT244ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT244ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
	CY74FCT244ATQC	Q5	20-Lead (150-Mil) QSOP	
5.1	CY54FCT244ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT244ATLMB	L61	20-Pin Square Leadless Chip Carrier	
6.5	CY74FCT244TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT244TSOC	S5	20-Lead (300-Mil) Molded SOIC	
	CY74FCT244TQC	Q5	20-Lead (150-Mil) QSOP	
7.0	CY54FCT244TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT244TLMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

Document #: 38-00259-A

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +135°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	-40°C to +85°C	5V ± 5%
Military ^[4]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	Com ¹	2.0		V	
		V _{CC} =Min., I _{OH} =-15 mA	Com ¹	2.4	3.3	V	
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3	V	
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com ¹		0.3	0.55	V
		V _{CC} =Min., I _{OL} =48mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage		2.0			V	
V _{IL}	Input LOW Voltage				0.8	V	
V _H	Hysteresis ^[6]	All inputs		0.2		V	
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V	
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}			5	μA	
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V			±1	μA	
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V			±1	μA	
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V	-60	-120	-225	mA	
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V			±1	μA	

Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Notes:

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT245T				FCT245AT				Unit	Fig. No. ^[13]
		Military		Commercial		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay A to B or B to A	1.5	7.5	1.5	7.0	1.5	4.9	1.5	4.6	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time OE or T/R to A or B	1.5	10.0	1.5	9.5	1.5	6.5	1.5	6.2	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time OE or T/R to A or B	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	ns	1, 7, 8

Switching Characteristics Over the Operating Range

Parameter	Description	FCT245CT				FCT245DT		Unit	Fig. No. ^[13]
		Military		Commercial		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay A to B or B to A	1.5	4.5	1.5	4.1	1.5	3.8	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time OE or T/R to A or B	1.5	6.2	1.5	5.8	1.5	5.0	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time OE or T/R to A or B	1.5	5.2	1.5	4.8	1.5	4.3	ns	1, 7, 8

Shaded areas contain preliminary information.

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information Section.



Quad 2-Input Multiplexer

Features

- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 4.3 ns max. (Com'l) FCT-A speed at 5.0 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- ESD > 2000V

- Sink current 64 mA (Com'l), 32 mA (Mil)
- Source current 32 mA (Com'l), 12 mA (Mil)

Functional Description

The FCT257T has four identical two-input multiplexers which select four bits of data from two sources under the control of a common data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the Select input is HIGH. Data appears at the output in true non-inverted form for the FCT257T.

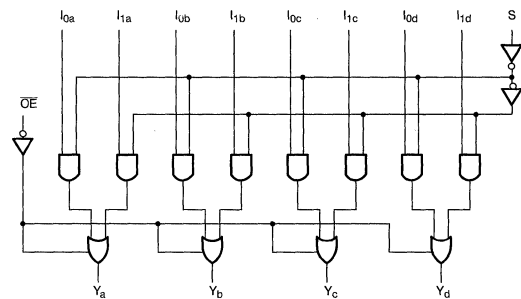
The FCT257T is a logic implementation of a four-pole, two position switch where

the position of the switch is determined by the logic levels supplied to the select input. Outputs are forced to a high-impedance "OFF" state when the Output Enable input (\overline{OE}) is HIGH.

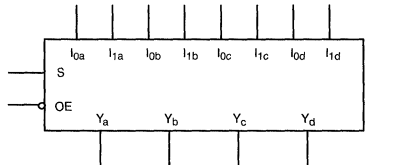
All but one device must be in the high-impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of three-state devices are tied together.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

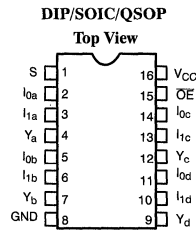
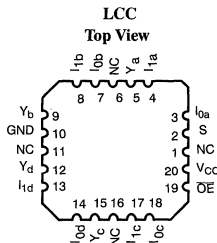
Logic Block Diagram



Logic Symbol



Pin Configurations



FCT257T-1

FCT257T-2

FCT257T-3

FCT257T-4

Pin Description

Name	Description
I	Data Inputs
S	Common Select Input
\overline{OE}	Enable Inputs (Active LOW)
Y	Data Outputs

Function Table^[1]

Inputs				Output
\overline{OE}	S	I_0	I_1	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

Note:

1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, Z = High impedance (OFF) state

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	0.1	0.2	mA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{CC} =Max., V _{IN} =3.4V ^[8] f ₁ =0, Outputs Open	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.06	0.12	mA/ MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Input Toggling at f ₁ =10 MHz, OE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.7	1.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Input Toggling at f ₁ =10 MHz, OE=GND, V _{IN} =3.4V or V _{IN} =GND	1.0	2.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Four Bits Toggling at f ₁ =2.5 MHz, OE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.7	1.4 ^[11]	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Four Bits Toggling at f ₁ =2.5 MHz, OE=GND, V _{IN} =3.4V or V _{IN} =GND	1.7	5.4 ^[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 I_C = I_{CC} + ΔI_{CC}D_HN_T + I_{CCD}(f₀/2 + f₁N₁)
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
 D_H = Duty Cycle for TTL inputs HIGH

- N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f₀ = Clock frequency for registered devices, otherwise zero
 f₁ = Input signal frequency
 N₁ = Number of inputs changing at f₁
 All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.3	CY74FCT257CTPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT257CTQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT257CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.0	CY54FCT257CTDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT257CTLMB	L61	20-Pin Square Leadless Chip Carrier	
5.0	CY74FCT257ATPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT257ATQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT257ATSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.8	CY54FCT257ATDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT257ATLMB	L61	20-Pin Square Leadless Chip Carrier	
6.0	CY74FCT257TPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT257TQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT257TSOC	S1	16-Lead (300-Mil) Molded SOIC	
7.0	CY54FCT257TDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT257TLMB	L61	20-Pin Square Leadless Chip Carrier	

Document #: 38-00289-A

Maximum Ratings^[2,3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +135°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	-40°C to +85°C	5V ± 5%
Military ^[4]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	Com'l	2.0			V
		V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3		V
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =32mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage			2.0			V
V _{IL}	Input LOW Voltage					0.8	V
V _H	Hysteresis ^[6]	All inputs			0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA			-0.7	-1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}				5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V				±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V				±1	μA
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V		-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V				±1	μA

Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Notes:

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT273T				FCT273AT				Unit	Fig. No. ^[13]
		Military		Commercial		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Clock to Output	2.0	15.0	2.0	13.0	2.0	8.3	2.0	7.2	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay MR to Output	2.0	15.0	2.0	13.0	2.0	8.3	2.0	7.2	ns	1, 6
t _S	Set-Up Time HIGH or LOW D to Clock	3.5		2.0		2.0		2.0		ns	4
t _H	Hold Time HIGH or LOW D to Clock	2.0		1.5		1.5		1.5		ns	4
t _W	Clock Pulse Width HIGH or LOW	7.0		6.0		6.0		6.0		ns	5
t _W	MR Pulse Width LOW	7.0		6.0		6.0		6.0		ns	6
t _{REC}	Recovery Time MR to Clock	5.0		2.0		2.5		2.0		ns	6

Parameter	Description	FCT273CT				Unit	Fig. No. ^[13]
		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Clock to Output	2.0	6.5	2.0	5.8	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay MR to Output	2.0	6.8	2.0	6.1	ns	1, 6
t _S	Set-Up Time HIGH or LOW D to Clock	2.0		2.0		ns	4
t _H	Hold Time HIGH or LOW D to Clock	1.5		1.5		ns	4
t _W	Clock Pulse Width HIGH or LOW	6.0		6.0		ns	5
t _W	MR Pulse Width LOW	6.0		6.0		ns	6
t _{REC}	Recovery Time MR to Clock	2.5		2.0		ns	6

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays. 13. See "Parameter Measurement Information" in the General Information Section.

Features

- Function, pinout and drive compatible with the fastest bipolar logic
- FCT-C speed at 4.2 ns max. (Com'1)
FCT-A speed at 5.2 ns max. (Com'1)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times

- ESD > 2000V
- Fully compatible with TTL input and output logic levels
- Sink Current 64 mA (Com'1),
 32 mA (Mil)
- Source Current 32 mA (Com'1),
 12 mA (Mil)

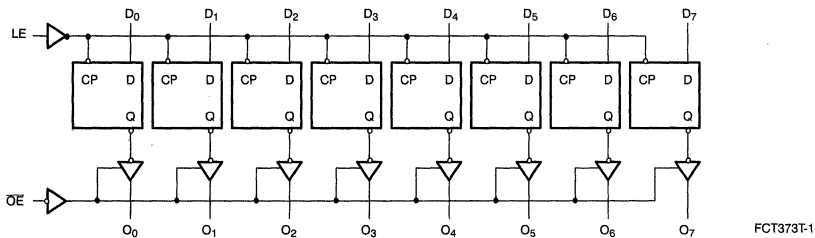
Functional Description

The FCT373T and FCT573T consist of eight latches with three-state outputs for bus organized system applications. When latch enable (LE) is HIGH, the flip-flops

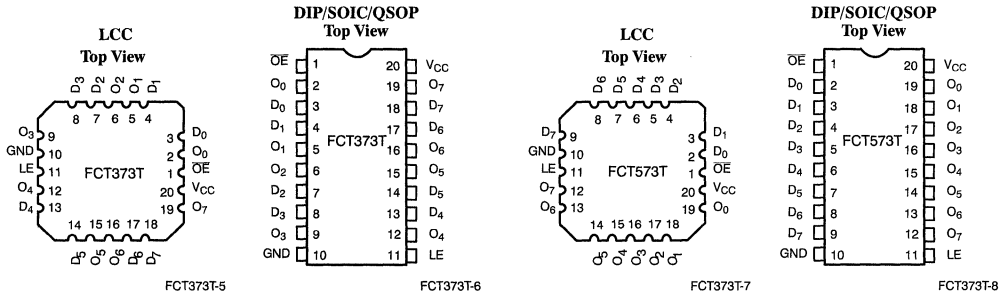
appear transparent to the data. Data that meets the required set-up times are latched when LE transitions from HIGH to LOW. Data appears on the bus when the output enable (\overline{OE}) is LOW. When output enable is HIGH, the bus output is in the high impedance state. In this mode, data may be entered into the latches. The FCT573T is identical to FCT373T except for flow-through pinout, which simplifies board design.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

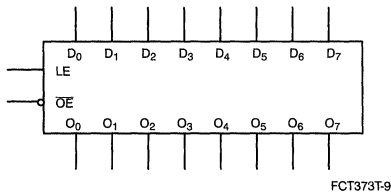
Logic Block Diagram



Pin Configurations



Logic Symbol



Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	6	10	pF
C _{OUT}	Output Capacitance	8	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	0.1	0.2	mA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{CC} =Max., V _{IN} =3.4V, ^[8] f ₁ =0, Outputs Open	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.6	0.12	mA/ MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =10 MHz, OE=GND, LE=V _{CC} V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.7	1.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =10 MHz, OE=GND, LE=V _{CC} V _{IN} =3.4V or V _{IN} =GND	1.0	2.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, OE=GND, LE=V _{CC} V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	1.3	2.6 ^[11]	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, OE=GND, LE=V _{CC} V _{IN} =3.4V or V _{IN} =GND	3.3	10.6 ^[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC}D_{HN}N_T + I_{CCD}(f₀/2 + f₁N₁)
I_{CC} = Quiescent Current with CMOS input levels
ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
D_H = Duty Cycle for TTL inputs HIGH

- N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
f₀ = Clock frequency for registered devices, otherwise zero
f₁ = Input signal frequency
N₁ = Number of inputs changing at f₁
All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.



Ordering Information—FCT373T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT373DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT373DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.2	CY74FCT373CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT373CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT373CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.1	CY54FCT373CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT373CTLMB	L61	20-Pin Square Leadless Chip Carrier	
5.2	CY74FCT373ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT373ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT373ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.6	CY54FCT373ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT373ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.0	CY74FCT373TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT373TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT373TSOC	S5	20-Lead (300-Mil) Molded SOIC	
8.5	CY54FCT373TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT373TLMB	L61	20-Pin Square Leadless Chip Carrier	



Ordering Information—FCT573T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT573DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT573DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.2	CY74FCT573CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT573CTQC	Q5	20-Lead (150-Mil) QSOP	
5.1	CY54FCT573CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT573CTLMB	L61	20-Pin Square Leadless Chip Carrier	
5.2	CY74FCT573ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT573ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT573ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.6	CY54FCT573ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT573ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.0	CY74FCT573TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT573TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT573TSOC	S5	20-Lead (300-Mil) Molded SOIC	
8.5	CY54FCT573TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT573TLMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

Document #: 38-00272-A

Function Table^[1]

Inputs			Outputs
D	CP	OE	O
H		L	H
L		L	L
X	X	H	Z

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +135°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W

 Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	-40°C to +85°C	5V ± 5%
Military ^[4]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	Com'l	2.0		V	
		V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3	V	
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3	V	
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =32 mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage		2.0			V	
V _{IL}	Input LOW Voltage				0.8	V	
V _H	Hysteresis ^[6]	All inputs		0.2		V	
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V	
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}			5	μA	
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V			±1	μA	
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V			±1	μA	
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} = Max., V _{OUT} = 2.7V			10	μA	
I _{OZL}	Off State LOW-Level Output Current	V _{CC} = Max., V _{OUT} = 0.5V			-10	μA	
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V	-60	-120	-225	mA	
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V			±1	μA	

Notes:

- H = HIGH Voltage Level.
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance
┌ = LOW-to-HIGH clock transition
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameters tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range^[12]

Parameter	Description	FCT374T/FCT574T				FCT374AT/FCT574AT				Unit	Fig. No. ^[14]
		Military		Commercial		Military		Commercial			
		Min. ^[13]	Max.	Min. ^[13]	Max.	Min. ^[13]	Max.	Min. ^[13]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Clock to Output	2.0	11.0	2.0	10.0	2.0	7.2	2.0	6.5	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time	1.5	14.0	1.5	12.5	1.5	7.5	1.5	6.5	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	8.0	1.5	8.0	1.5	6.5	1.5	5.5	ns	1, 7, 8
t _S	Set-Up Time HIGH or LOW D to CP	2.0		2.0		2.0		2.0		ns	4
t _H	Hold Time HIGH or LOW D to CP	1.5		1.5		1.5		1.5		ns	4
t _W	Clock Pulse Width ^[15] HIGH or LOW	7.0		7.0		6.0		5.0		ns	5

Parameter	Description	FCT374CT/FCT574CT				FCT374DT/ FCT574DT		Unit	Fig. No. ^[14]
		Military		Commercial		Commercial			
		Min. ^[13]	Max.	Min. ^[13]	Max.	Min. ^[13]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Clock to Output	2.0	6.2	2.0	5.2	2.0	4.2	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time	1.5	6.2	1.5	5.5	1.5	4.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	5.7	1.5	5.0	1.5	4.0	ns	1, 7, 8
t _S	Set-Up Time, HIGH or LOW D to CP	2.0		2.0		2.0		ns	4
t _H	Hold Time, HIGH or LOW D to CP	1.5		1.5		1.5		ns	4
t _W	Clock Pulse Width ^[15] HIGH or LOW	6.0		5.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

12. AC Characteristics guaranteed with C_L = 50 pF as shown in Figure 1 of the "Parameter Measurement Information" in the General Information Section.
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. See "Parameter Measurement Information" in the General Information Section.
15. With one data channel toggling, t_W(L) = t_W(H) = 4.0 ns and t_r = t_f = 1.0 ns.

Features

- Function, pinout and drive compatible with FCT and F logic
- FCT-C speed at 5.2 ns max. (Com'l)
FCT-A speed at 7.2 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- ESD > 2000V

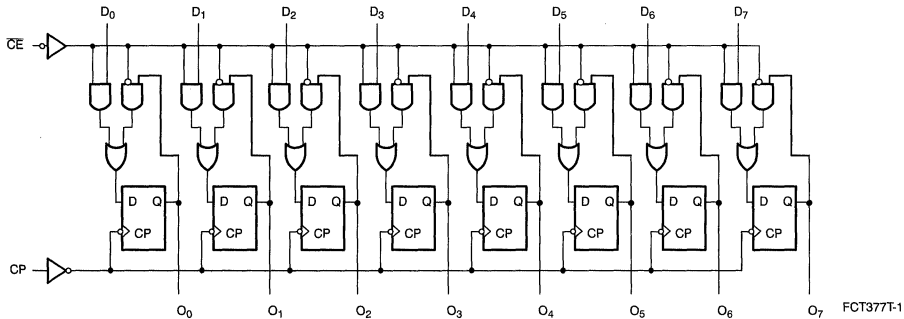
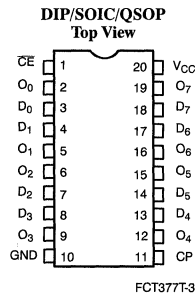
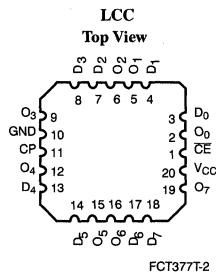
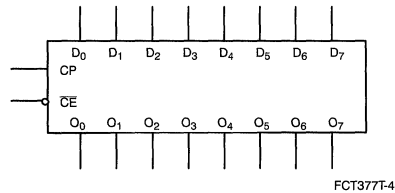
- Fully compatible with TTL input and output logic levels
- Sink current **64 mA (Com'l),
32 mA (Mil)**
- Source current **32 mA (Com'l),
12 mA (Mil)**
- Clock Enable for address and data synchronization application
- Eight edge-triggered D flip-flops

Functional Description

The FCT377T has eight triggered D-type flip-flops with individual D inputs. The common buffered clock inputs (CP) loads

all flip-flops simultaneously when the Clock Enable (\overline{CE}) is LOW. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The \overline{CE} input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram

Pin Configurations

Logic Symbol


Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	0.1	0.2	mA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{CC} =Max., V _{IN} =3.4V ^[8] f ₁ =0, Outputs Open	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Bit Toggling, 50% Duty Cycle, Outputs Open, CE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.06	0.12	mA/ MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., f ₀ =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =5 MHz, CE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.7	1.4	mA
		V _{CC} =Max., f ₀ =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =5 MHz, CE=GND, V _{IN} =3.4V or V _{IN} =GND	1.2	3.4	mA
		V _{CC} =Max., f ₀ =10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, CE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	1.6	3.2 ^[11]	mA
		V _{CC} =Max., f ₀ =10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, CE=GND, V _{IN} =3.4V or V _{IN} =GND	3.9	12.2 ^[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
 9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

10. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 I_C = I_{CC} + ΔI_{CCD_{HN}} + I_{CCD}(f₀/2 + f₁N₁)
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
 D_H = Duty Cycle for TTL inputs HIGH

- N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f₀ = Clock frequency for registered devices, otherwise zero
 f₁ = Input signal frequency
 N₁ = Number of inputs changing at f₁
 All currents are in milliamps and all frequencies are in megahertz.
 11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Ordering Information—FCT377T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.2	CY74FCT377CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT377CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT377CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.5	CY54FCT377CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT377CTLMB	L61	20-Pin Square Leadless Chip Carrier	
7.2	CY74FCT377ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT377ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT377ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
8.3	CY54FCT377ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT377ATLMB	L61	20-Pin Square Leadless Chip Carrier	
13.0	CY74FCT377TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT377TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT377TSOC	S5	20-Lead (300-Mil) Molded SOIC	
15.0	CY54FCT377TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT377TLMB	L61	20-Pin Square Leadless Chip Carrier	

Document #: 38-00279-A



Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied -65°C to +135°C
 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Input Voltage -0.5V to +7.0V
 DC Output Voltage -0.5V to +7.0V
 DC Output Current (Maximum Sink Current/Pin) 120 mA
 Power Dissipation 0.5W

Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	-40°C to +85°C	5V ± 5%
Military ^[4]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	Com'l	2.0		V	
		V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3	V	
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3	V	
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =32 mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage		2.0			V	
V _{IL}	Input LOW Voltage				0.8	V	
V _H	Hysteresis ^[6]	All inputs		0.2		V	
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V	
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}			5	μA	
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V			±1	μA	
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V			±1	μA	
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V	-60	-120	-225	mA	
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V			±1	μA	

Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Notes:

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques is preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT399T				FCT399AT				Unit	Fig. No. ^[13]
		Military		Commercial		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay CP to Q	3.0	11.5	3.0	10.0	2.5	7.5	2.5	7.0	ns	1, 5
t _S	Set-Up Time HIGH or LOW I _n to CP	4.5		3.5		4.0		3.5		ns	4
t _H	Hold Time HIGH or LOW I _n to CP	1.5		1.0		1.0		1.0		ns	4
t _S	Set-Up Time HIGH or LOW S to CP	9.5		8.5		9.0		8.5		ns	4
t _H	Hold Time HIGH or LOW S to CP	0		0		0		0		ns	4
t _w	Clock Pulse Width ^[6] HIGH or LOW	7.0		5.0		6.0		5.0		ns	5

Parameter	Description	FCT399CT				Unit	Fig. No. ^[13]
		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay CP to Q	2.5	6.6	2.5	6.1	ns	1, 5
t _S	Set-Up Time, HIGH or LOW, I _n to CP	4.0		3.5		ns	4
t _H	Hold Time, HIGH or LOW, I _n to CP	1.0		1.0		ns	4
t _S	Set-Up Time, HIGH or LOW, S to CP	9.0		8.5		ns	4
t _H	Hold Time, HIGH or LOW, S to CP	0		0		ns	4
t _w	Clock Pulse Width ^[6] HIGH or LOW	6.0		5.0		ns	5

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays. 13. See "Parameter Measurement Information" in the General Information Section.



Dual 8-Bit Parity Generator/Checker

Features

- Function, pinout and drive compatible with FCT and F logic
- FCT-A speed at 7.5 ns max. (Com'l)
FCT-B speed at 5.6 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- ESD > 2000V

- Fully compatible with TTL input and output logic levels
- Sink Current 64 mA (Com'l), 32 mA (Mil)
Source Current 32 mA (Com'l), 12 mA (Mil)
- Two 8-bit parity generator/checkers
- Open drain Active LOW parity error output
- Expandable for larger word widths

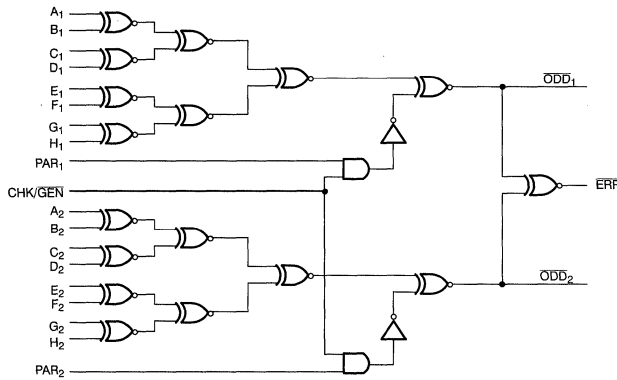
Functional Description

The FCT480T is a high-speed dual 8-bit parity generator/checker. Each parity generator/checker accepts eight data bits

and one parity bit as inputs, and generates a sum and parity error output. The FCT480T can be used in ODD parity systems. The parity error output is open-drain, designed for easy expansion of the word width by a wired-OR connection of several FCT480T type devices. Since additional logic is not needed, the parity generation or checking times remain the same as for an individual FCT480T device.

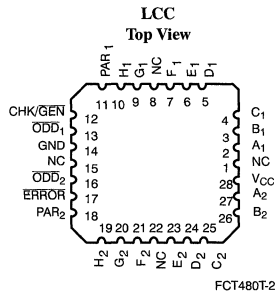
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram

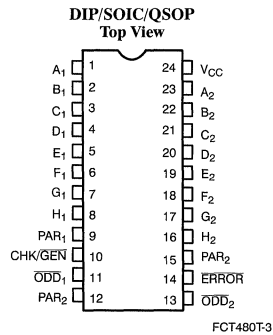


FCT480T-1

Pin Configurations



FCT480T-2



FCT480T-3

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[4]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} = -32 mA	Com'l	2.0			V
		V _{CC} =Min., I _{OH} = -15 mA	Com'l	2.4	3.3		V
		V _{CC} =Min., I _{OH} = -12 mA	Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =32 mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage			2.0			V
V _{IL}	Input LOW Voltage					0.8	V
V _H	Hysteresis ^[5]	All inputs			0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} = -18 mA			-0.7	-1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}				5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V				±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V				±1	μA
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} = Max., V _{OUT} = 2.7V				10	μA
I _{OZL}	Off State LOW-Level Output Current	V _{CC} = Max., V _{OUT} = 0.5V				-10	μA
I _{OS}	Output Short Circuit Current ^[6]	V _{CC} =Max., V _{OUT} =0.0V		-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V				±1	μA

Capacitance^[5]

Parameter	Description	Typ. ^[4]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Notes:

- Typical values are at V_{CC}=5.0V, T_A= +25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order

to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.6	CY74FCT480BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT480BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT480BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.0	CY54FCT480BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT480BTLMB	L64	28-Square Leadless Chip Carrier	
7.5	CY74FCT480ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT480ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT480ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
9.5	CY54FCT480ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT480ATLMB	L64	28-Square Leadless Chip Carrier	
13.0	CY74FCT480TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT480TQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT480TSOC	S13	24-Lead (300-Mil) Molded SOIC	
17.0	CY54FCT480TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT480TLMB	L64	28-Square Leadless Chip Carrier	

Document #: 38-00281-A

Function Table FCT540T^[1]

Inputs			Output
\overline{OE}_A	\overline{OE}_B	D	
L	L	L	H
L	L	H	L
H	H	X	Z

Function Table FCT541T^[1]

Inputs			Output
\overline{OE}_A	\overline{OE}_B	D	
L	L	L	L
L	L	H	H
H	H	X	Z

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +135°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	-40°C to +85°C	5V ± 5%
Military ^[4]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	Com'l	2.0		V	
		V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3	V	
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3	V	
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =48 mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage		2.0			V	
V _{IL}	Input LOW Voltage				0.8	V	
V _H	Hysteresis ^[6]	All inputs		0.2		V	
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V	
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}			5	μA	
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V			±1	μA	
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V			±1	μA	
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} =Max., V _{OUT} =2.7V			10	μA	
I _{OZL}	Off State LOW-Level Output Current	V _{CC} =Max., V _{OUT} =0.5V			-10	μA	
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V	-60	-120	-225	mA	
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V			±1	μA	

Notes:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.

- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parametric tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT540T/FCT541T				FCT540AT/FCT541AT				Unit	Fig. No. ^[13]
		Military		Commercial		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output (FCT540)	1.5	9.5	1.5	8.5	1.5	5.1	1.5	4.8	ns	1, 2
t _{PLH} t _{PHL}	Propagation Delay Data to Output (FCT541)	1.5	9.0	1.5	8.0	1.5	5.1	1.5	4.8	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time	1.5	10.5	1.5	10.0	1.5	6.5	1.5	6.2	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	10.0	1.5	9.5	1.5	5.9	1.5	5.6	ns	1, 7, 8

Parameter	Description	FCT540CT/FCT541CT				FCT540DT/ FCT541DT		Unit	Fig. No. ^[13]
		Military		Commercial		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output (FCT540)	1.5	4.7	1.5	4.1	1.5	3.8	ns	1, 2
t _{PLH} t _{PHL}	Propagation Delay Data to Output (FCT541)	1.5	4.6	1.5	4.1	1.5	3.3	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time	1.5	6.5	1.5	5.8	1.5	5.2	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	5.7	1.5	5.2	1.5	5.0	ns	1, 7, 8

Shaded areas contain preliminary information.

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays. 13. See "Parameter Measurement Information" in the General Information section.



8-Bit Latched Registered Transceiver

Features

- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 5.3 ns max. (Com'1)
FCT-A speed at 6.5 ns max. (Com'1)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- ESD > 2000V

- Sink current 64 mA (Com'1), 48 mA (Mil)
- Source current 32 mA (Com'1), 12 mA (Mil)
- Separation controls for data flow in each direction
- Back to back latches for storage

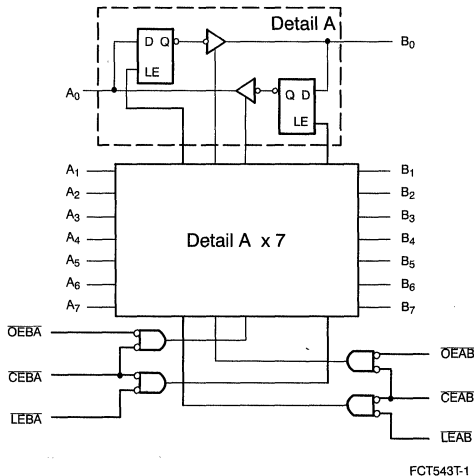
Functional Description

The FCT543T octal latched transceiver contains two sets of eight D-type latches with separate latch enable (LEAB, LEBA) and output enable (OEAB, OEBA) controls for each set to permit independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B enable (CEAB) input must be

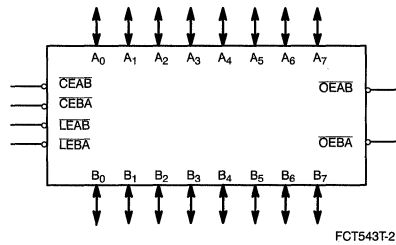
LOW in order to enter data from A or to take data from B, as indicated in the truth table. With CEAB LOW, a LOW signal on the A-to-B latch enable (LEAB) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the LEAB signal puts the A latches in the storage mode and their output no longer change with the A inputs. With CEAB and OEAB both LOW, the three-stage B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses CEBA, LEBA, and OEBA inputs.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Functional Block Diagram

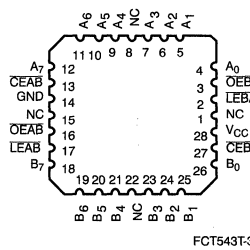


Logic Block Diagram

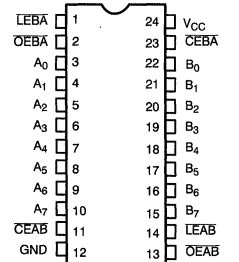


Pin Configurations

LCC Top View



DIP/SOIC/QSOP Top View



Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[7]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	Com'l	2.0			V
		V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3		V
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =48mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage			2.0			V
V _{IL}	Input LOW Voltage					0.8	V
V _H	Hysteresis ^[8]	All inputs			0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA			-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}				5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V				±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V				±1	μA
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} = Max., V _{OUT} = 2.7V				10	μA
I _{OZL}	Off State LOW-Level Output Current	V _{CC} = Max., V _{OUT} = 0.5V				-10	μA
I _{OS}	Output Short Circuit Current ^[9]	V _{CC} =Max., V _{OUT} =0.0V		-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V				±1	μA

Capacitance^[8]

Parameter	Description	Typ. ^[7]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Notes:

7. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
8. This parameter is guaranteed but not tested.
9. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT543T				FCT543AT				Unit	Fig. No. ^[15]
		Military		Commercial		Military		Commercial			
		Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Transparent Mode A to B or B to A	2.0	10.0	2.5	8.5	2.5	7.5	2.5	6.5	ns	1, 3
t _{PLH} t _{PHL}	Propagation Delay LEBA to A LEAB to B	2.5	14.0	2.5	12.5	2.5	9.0	2.5	8.0	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	2.0	14.0	2.0	12.0	2.0	10.0	2.0	9.0	ns	1, 7, 8
t _{PZH} t _{PZL}	Output Disable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	2.0	13.0	2.0	9.0	2.0	8.5	2.0	7.5	ns	1, 7, 8
t _S	Set-Up Time HIGH or LOW, A or B to LEBA or LEAB	3.0		2.0		2.0		2.0		ns	9
t _H	Hold Time HIGH or LOW, A or B to LEBA or LEAB	2.0		2.0		2.0		2.0		ns	9
t _W	Pulse Width LOW ^[6] LEBA or LEAB	5.0		5.0		5.0		5.0		ns	5

Parameter	Description	FCT543CT				FCT543DT		Unit	Fig. No. ^[15]
		Military		Commercial		Commercial			
		Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Transparent Mode A to B or B to A	2.5	6.1	2.5	5.3	1.5	4.4	ns	1, 3
t _{PLH} t _{PHL}	Propagation Delay LEBA to A, LEAB to B	2.5	8.0	2.5	7.0	1.5	5.0	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	2.0	9.0	2.0	8.0	1.5	5.4	ns	1, 7, 8
t _{PZH} t _{PZL}	Output Disable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	2.0	7.5	2.0	6.5	1.5	4.3	ns	1, 7, 8
t _S	Set-Up Time, HIGH or LOW, A or B to LEBA or LEAB	2.0		2.0		1.5		ns	9
t _H	Hold Time, HIGH or LOW, A or B to LEBA or LEAB	2.0		2.0		1.5		ns	9
t _W	Pulse Width LOW LEBA or LEAB ^[6]	5.0		5.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

14. Minimum limits are guaranteed but not tested on Propagation Delays. 15. See "Parameter Measurement Information" in the General Information Section.

8-Bit Registered Transceivers

Features

- Function, pinout and drive compatible with FCT and F logic
- FCT-C speed at 5.4 ns max. (Com'l)
FCT-A speed at 6.3 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- ESD > 2000V

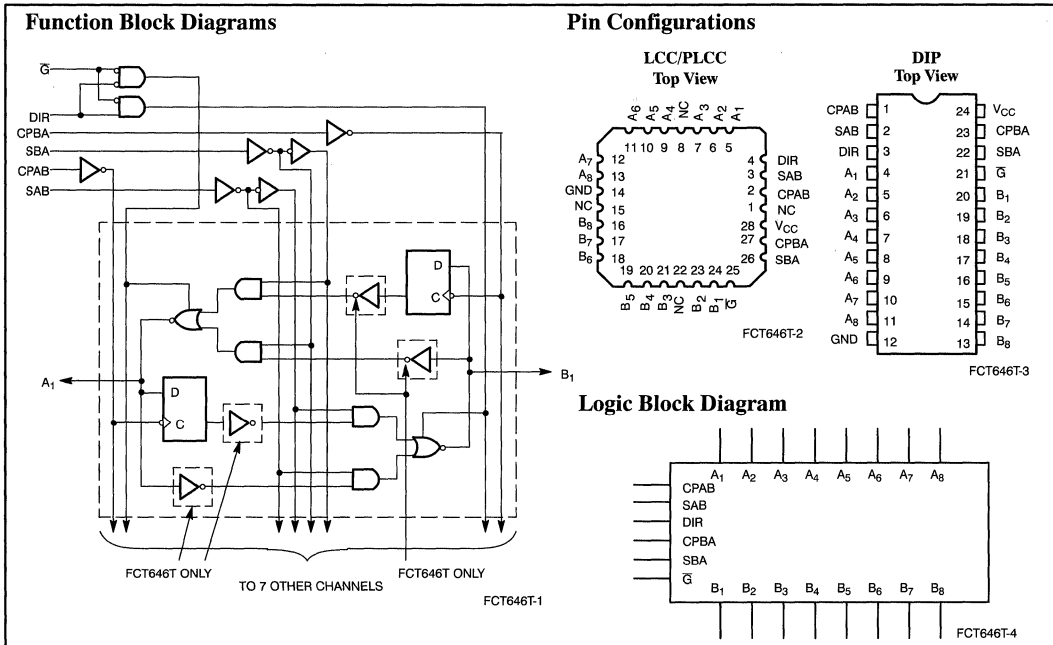
- Sink current 64 mA (Com'l),
48 mA (Mil)
- Source current 32 mA (Com'l),
12 mA (Mil)
- Independent register for A and B buses
- Three-state output

Functional Description

The FCT646T and FCT648T consist of a bus transceiver circuit with three-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH

logic level. Enable Control \bar{G} and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the A or B register, or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control \bar{G} is Active LOW. In the isolation mode (enable Control \bar{G} HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.



Pin Description

Name	Description
A	Data Register A Inputs, Data Register B Outputs
B	Data Register B Inputs, Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, \bar{G}	Output Enable Inputs



Maximum Ratings^[4, 5]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +135°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	-40°C to +85°C	5V ± 5%
Military ^[6]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[7]	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	Com'l	2.0		V	
		V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3	V	
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3	V	
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =48 mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage		2.0			V	
V _{IL}	Input LOW Voltage				0.8	V	
V _H	Hysteresis ^[8]	All inputs		0.2		V	
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V	
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}			5	µA	
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V			±1	µA	
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V			±1	µA	
I _{OS}	Output Short Circuit Current ^[9]	V _{CC} =Max., V _{OUT} =0.0V	-60	-120	-225	mA	
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V			±1	µA	

Capacitance^[8]

Parameter	Description	Typ. ^[7]	Max.	Unit
C _{IN}	Input Capacitance	6	10	pF
C _{OUT}	Output Capacitance	8	12	pF

Notes:

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.



Switching Characteristics Over the Operating Range

Parameter	Description	FCT646T/FCT648T				FCT646AT/FCT648AT				Unit	Fig. No. ^[15]
		Military		Commercial		Military		Commercial			
		Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	2.0	11.0	1.5	9.0	2.0	7.7	1.5	6.3	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time Enable to Bus and DIR to A _n or B _n	2.0	15.0	1.5	14.0	2.0	10.5	1.5	9.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time Ḡ to Bus and DIR to Bus	2.0	11.0	1.5	9.0	2.0	7.7	1.5	6.3	ns	1, 7, 8
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus	2.0	10.0	1.5	9.0	2.0	7.0	1.5	6.3	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay SBA or SAB to A or B	2.0	12.0	1.5	11.0	2.0	8.4	1.5	7.7	ns	1, 5
t _S	Set-Up Time HIGH or LOW, Bus to Clock	4.5		4.0		2.0		2.0		ns	4
t _H	Hold Time HIGH or LOW, Bus to Clock	2.0		2.0		1.5		1.5		ns	4
t _w	Pulse Width, ^[6] HIGH or LOW	6.0		6.0		5.0		5.0		ns	5

Parameter	Description	FCT646CT/FCT648CT				Unit	Fig. No. ^[15]
		Military		Commercial			
		Min. ^[14]	Max.	Min. ^[14]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	1.5	6.0	1.5	5.4	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time Enable to Bus and DIR to A _n or B _n	1.5	8.9	1.5	7.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time Ḡ to Bus and DIR to Bus	1.5	7.7	1.5	6.3	ns	1, 7, 8
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus	1.5	6.3	1.5	5.7	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay SBA or SAB to A or B	1.5	7.0	1.5	6.2	ns	1, 5
t _S	Set-Up Time, HIGH or LOW, Bus to Clock	2.0		2.0		ns	4
t _H	Hold Time, HIGH or LOW, Bus to Clock	1.5		1.5		ns	4
t _w	Pulse Width, ^[6] HIGH or LOW	5.0		5.0		ns	5

Notes:

14. Minimum limits are guaranteed but not tested on Propagation Delays. 15. See "Parameter Measurement Information" in the General Information Section.

8-Bit Registered Transceiver

Features

- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 5.4 ns max. (Com'l)
FCT-A speed at 6.3 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Sink current 64 mA (Com'l),
 48 mA (Mil)
- Source current 32 mA (Com'l),
 12 mA (Mil)
- ESD > 2000V

- Independent register for A and B buses
- Multiplexed real-time and stored data transfer

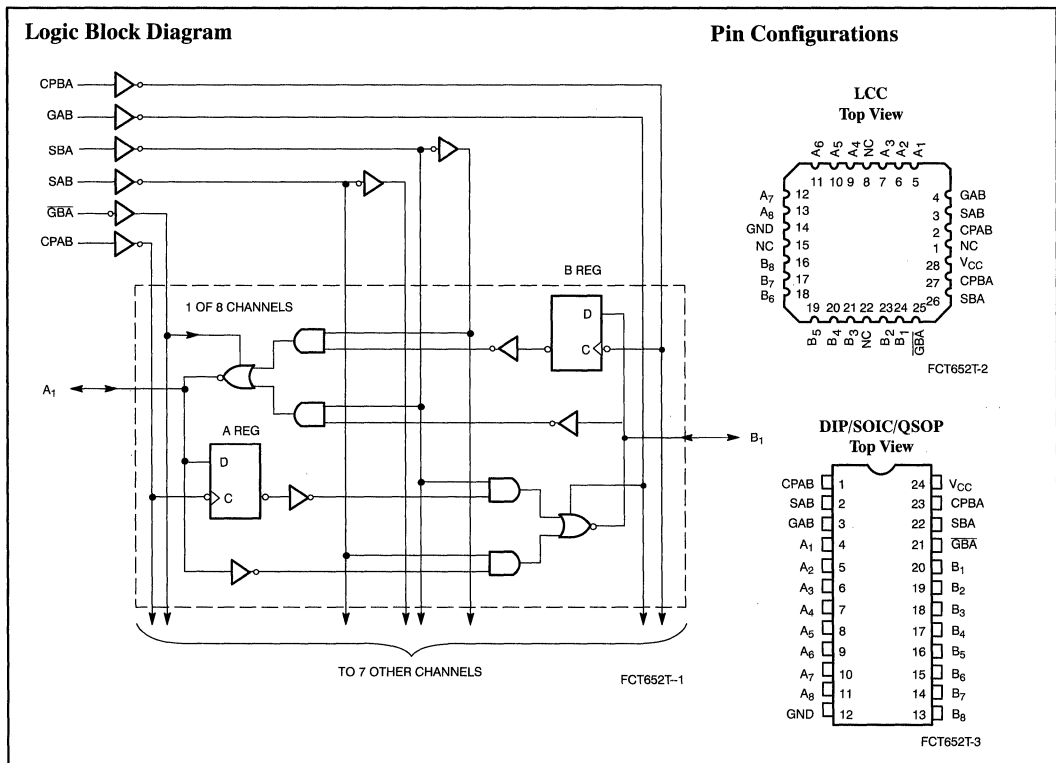
Functional Description

The FCT652T consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. GAB and $\overline{G}BA$ control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input

level selects real-time data and a HIGH selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}BA$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.



Maximum Ratings^[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +135°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W

 Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	-40°C to +85°C	5V ± 5%
Military ^[5]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[6]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	Com'l	2.0			V
		V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3		V
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =48 mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage			2.0			V
V _{IL}	Input LOW Voltage					0.8	V
V _H	Hysteresis ^[7]	All inputs			0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA			-0.7	-1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}				5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V				±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V				±1	μA
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} =Max., V _{OUT} =2.7V				10	μA
I _{OZL}	Off State LOW-Level Output Current	V _{CC} =Max., V _{OUT} =0.5V				-10	μA
I _{OS}	Output Short Circuit Current ^[8]	V _{CC} =Max., V _{OUT} =0.0V		-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V				±1	μA

Capacitance^[7]

Parameter	Description	Typ. ^[6]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Notes:

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics^[13] Over the Operating Range

Parameter	Description	FCT652T				FCT652AT				Unit	Fig. No. ^[15]
		Military		Commercial		Military		Commercial			
		Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	2.0	11.0	1.5	9.0	2.0	7.7	1.5	6.3	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time Enable to Bus	2.0	15.0	1.5	14.0	2.0	10.5	1.5	9.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time Enable to Bus	2.0	11.0	1.5	9.0	2.0	7.7	1.5	6.3	ns	1, 7, 8
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus	2.0	10.0	1.5	9.0	2.0	7.0	1.5	6.3	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay SBA or SAB to A or B	2.0	12.0	1.5	11.0	2.0	8.4	1.5	7.7	ns	1, 5
t _S	Set-Up Time HIGH or LOW Bus to Clock	4.5		4.0		2.0		2.0		ns	4
t _H	Hold Time HIGH or LOW Bus to Clock	2.0		2.0		1.5		1.5		ns	4
t _w	Clock Pulse Width, ^[16] HIGH or LOW	6.0		6.0		5.0		5.0		ns	5

Parameter	Description	FCT652CT				FCT652DT		Unit	Fig. No. ^[15]
		Military		Commercial		Commercial			
		Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	1.5	6.0	1.5	5.4	1.5	4.4	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time Enable to Bus	1.5	8.9	1.5	7.8	1.5	5.0	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time Enable to Bus	1.5	7.7	1.5	6.3	1.5	4.3	ns	1, 7, 8
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus	1.5	6.3	1.5	5.7	1.5	4.4	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay SBA or SAB to A or B	1.5	7.0	1.5	6.2	1.5	5.0	ns	1, 5
t _S	Set-Up Time HIGH or LOW Bus to Clock	2.0		2.0		1.5		ns	4
t _H	Hold Time HIGH or LOW Bus to Clock	1.5		1.5		1.0		ns	4
t _w	Pulse Width, ^[16] HIGH or LOW	5.0		5.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

13. AC Characteristics guaranteed with C_L = 50 pF as shown in Figure 1 of "Parameter Measurement Information" in the General Information section.
14. Minimum limits are guaranteed but not tested on Propagation Delays.

15. See "Parameter Measurement Information" in the General Information Section.
16. With one data channel toggling, t_w(L) = t_w(H) = 4.0 ns and t_r = t_f = 1.0 ns.



CY54/74FCT821T
CY54/74FCT823T
CY54/74FCT825T

8-/9-/10-Bit Bus Interface Registers

Features

- **Function, pinout and drive compatible with FCT, F, and Am29821/23/25 logic**
- **FCT-C speed at 6.0 ns max. (Com'l)**
FCT-B speed at 7.5 ns max. (Com'l)
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **ESD > 2000V**

- **Sink current** **64 mA (Com'l),**
 32 mA (Mil)
- **Source current** **32 mA (Com'l),**
 12 mA (Mil)
- **High-speed parallel registers with positive edge-triggered D-type flip-flops**
- **Buffered common clock enable (\overline{EN}) and asynchronous clear input (\overline{CLR})**

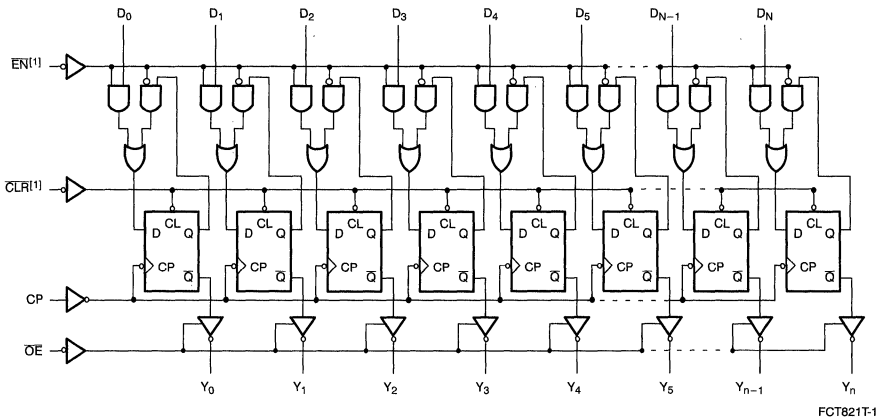
Functional Description

These bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The FCT821T is a buffered, 10-bit wide version of the popular FCT374 function. The FCT823T is a 9-bit wide buffered register

with clock enable (\overline{EN}) and clear (\overline{CLR}) — ideal for parity bus interfacing in high-performance microprogrammed systems. The FCT825T is an 8-bit buffered register with all the FCT823T controls plus multiple enables ($\overline{OE}_1, \overline{OE}_2, \overline{OE}_3$) to allow multiuser control of the interface, e.g., CS, DMA, and RD/WR. They are ideal for use as an output port requiring high I_{OL}/I_{OH} .

These devices are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high-impedance state and are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram



Note:

1. Not on FCT821.

Pin Description

Name	I/O	Description
D	I	The D flip-flop data inputs.
CLR	I	When CLR is LOW and OE is LOW, the Q outputs are LOW. When CLR is HIGH, data can be entered into the register.
CP	O	Clock Pulse for the register; enters data into the register on the LOW-to-HIGH transition.
Y	O	The register three-state outputs.
EN	I	Clock Enable. When EN is LOW, data on the D input is transferred to the Q output on the LOW-to-HIGH clock transition. When EN is HIGH, the Q outputs do not change state, regardless of the data or clock input transitions.
OE	I	Output Control. When OE is HIGH, the Y outputs are in the high-impedance state. When OE is LOW, the TRUE register data is present at the Y outputs.

Function Table^[2]

Inputs					Internal Outputs		Function
OE	CLR	EN	D	CP	Q	Y	
H	H	L	L	┌	L	Z	High Z
H	H	L	H	┐	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	┌	L	Z	Load
H	H	L	H	┐	H	Z	
L	H	L	L	┌	L	L	
L	H	L	H	┐	H	H	

Maximum Ratings^[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with
 Power Applied -65°C to +135°C
 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Input Voltage -0.5V to +7.0V
 DC Output Voltage -0.5V to +7.0V
 DC Output Current (Maximum Sink Current/Pin) 120 mA
 Power Dissipation 0.5W

Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	AT, BT	-40°C to +85°C	5V ± 5%
Military ^[5]	All	-55°C to +125°C	5V ± 10%

Notes:

- H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, NC = No Change, J = LOW-to-HIGH Transition, Z = HIGH Impedance.
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[6]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} \leq 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC} = \text{Max.}, V_{IN} = 3.4V$, ^[9] $f_1 = 0, \text{Outputs Open}$	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ^[10]	$V_{CC} = \text{Max.}, \text{One Bit Toggling},$ $50\% \text{ Duty Cycle, Outputs Open},$ $\overline{OE} = \overline{EN} = \text{GND},$ $V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current ^[11]	$V_{CC} = \text{Max.}, f_0 = 10 \text{ MHz},$ $50\% \text{ Duty Cycle, Outputs Open},$ $\text{One Bit Toggling at } f_1 = 5 \text{ MHz},$ $\overline{OE} = \overline{EN} = \text{GND},$ $V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	0.7	1.4	mA
		$V_{CC} = \text{Max.}, f_0 = 10 \text{ MHz},$ $50\% \text{ Duty Cycle, Outputs Open},$ $\text{One Bit Toggling at } f_1 = 5 \text{ MHz},$ $\overline{OE} = \overline{EN} = \text{GND},$ $V_{IN} = 3.4V \text{ or } V_{IN} = \text{GND}$	1.2	3.4	mA
		$V_{CC} = \text{Max.}, f_0 = 10 \text{ MHz},$ $50\% \text{ Duty Cycle, Outputs Open},$ $\text{Eight Bits Toggling at } f_1 = 2.5 \text{ MHz},$ $\overline{OE} = \overline{EN} = \text{GND},$ $V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	1.6	3.2 ^[11]	mA
		$V_{CC} = \text{Max.}, f_0 = 10 \text{ MHz},$ $50\% \text{ Duty Cycle, Outputs Open},$ $\text{Eight Bits Toggling at } f_1 = 2.5 \text{ MHz},$ $\overline{OE} = \overline{EN} = \text{GND},$ $V_{IN} = 3.4V \text{ or } V_{IN} = \text{GND}$	3.9	12.2 ^[12]	mA

Notes:

9. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
11. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH

- N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamps and all frequencies are in megahertz.

12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range (continued)

Param.	Description	Test Load	FCT821CT/FCT823CT/FCT825CT				Unit	Fig. No. ^[14]
			Military		Commercial			
			Min. ^[13]	Max.	Min. ^[13]	Max.		
t _{PLH} t _{PHL}	Propagation Delay CP to Y (\overline{OE} =LOW)	C _L =50 pF R _L =500Ω		7.0		6.0	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay CP to Y (\overline{OE} =LOW) ^[6]	C _L =300 pF R _L =500Ω		13.5		12.5	ns	1, 5
t _{PLH}	Propagation Delay CLR to Y ₁	C _L =50 pF R _L =500Ω		8.5		8.0	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time OE to Y	C _L =50 pF R _L =500Ω		8.0		7.0	ns	1, 7, 8
t _{PZH} t _{PZL}	Output Enable Time OE to Y ^[6]	C _L =300 pF R _L =500Ω		13.5		12.5	ns	1, 7, 8
t _{PHZ} t _{PHL}	Output Disable Time OE to Y ^[6]	C _L =5 pF R _L =500Ω		6.2		6.0	ns	1, 7, 8
t _{PHZ} t _{PHL}	Output Disable Time OE to Y	C _L =50 pF R _L =500Ω		6.5		6.5	ns	1, 7, 8
t _{SU}	Data to CP Set-Up Time	C _L =50 pF R _L =500Ω	3.0		3.0		ns	4
t _H	Data to CP Hold Time		1.5		1.5		ns	4
t _{SU}	Enable \overline{EN} to CP Set-Up Time		3.0		3.0		ns	4
t _H	Enable \overline{EN} to CP Hold Time		0.0		0.0		ns	4
t _{REM}	Clear Recovery Time CLR to CP		6.0		6.0		ns	6
t _w	Clock Pulse Width		6.0		6.0		ns	5
t _w	\overline{CLR} Pulse Width LOW		6.0		6.0		ns	5



Ordering Information—FCT825T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT825CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT825CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT825CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT825CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT825CTLMB	L64	28-Square Leadless Chip Carrier	
6.3	CY74FCT825BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT825BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT825BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.7	CY54FCT825BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT825BTLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY74FCT825ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT825ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT825ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT825ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT825ATLMB	L64	28-Square Leadless Chip Carrier	

Document #: 38-00282-A

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +135°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W

 Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	AT, BT	-40°C to +85°C	5V ± 5%
Military ^[4]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	Com'l	2.0		V	
		V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3	V	
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3	V	
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =32 mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage		2.0			V	
V _{IL}	Input LOW Voltage				0.8	V	
V _H	Hysteresis ^[6]	All inputs		0.2		V	
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V	
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}			5	μA	
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V			±1	μA	
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V			±1	μA	
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} = Max., V _{OUT} = 2.7V			10	μA	
I _{OZL}	Off State LOW-Level Output Current	V _{CC} = Max., V _{OUT} = 0.5V			-10	μA	
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V	-60	-120	-225	mA	
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V			±1	μA	

Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Notes:

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range^[12]

Parameter	Description	Test Load	FCT827AT				FCT827BT				Unit	Fig. No. ^[13]
			Military		Commercial		Military		Commercial			
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay D to Y	C _L =50 pF R _L =500Ω	1.5	9.0	1.5	8.0	1.5	6.5	1.5	5.0	ns	1, 3
t _{PLH} t _{PHL}	Propagation Delay D to Y ^[6]	C _L =300 pF R _L =500Ω	1.5	17.0	1.5	15.0	1.5	14.0	1.5	13.0	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time OE to Y	C _L =50 pF R _L =500Ω	1.5	13.0	1.5	12.0	1.5	9.0	1.5	8.0	ns	1, 7, 8
t _{PZH} t _{PZL}	Output Enable Time OE to Y ^[6]	C _L =300 pF R _L =500Ω	1.5	25.0	1.5	23.0	1.5	16.0	1.5	15.0	ns	1, 7, 8
t _{PHZ} t _{PHL}	Output Disable Time- OE to Y ^[6]	C _L =5 pF	1.5	9.0	1.5	9.0	1.5	7.0	1.5	6.0	ns	1, 7, 8
t _{PHZ} t _{PHL}	Output Disable Time OE to Y	C _L =50 pF R _L =500Ω	1.5	10.0	1.5	10.0	1.5	8.0	1.5	7.0	ns	1, 7, 8

Parameter	Description	Test Load	FCT827CT				Unit	Fig. No. ^[13]
			Military		Commercial			
			Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay D to Y	C _L =50 pF R _L =500Ω	1.5	5.0	1.5	4.4	ns	1, 3
t _{PLH} t _{PHL}	Propagation Delay D to Y ^[6]	C _L =300 pF R _L =500Ω	1.5	11.0	1.5	10.0	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time OE to Y	C _L =50 pF R _L =500Ω	1.5	8.0	1.5	7.0	ns	1, 7, 8
t _{PZH} t _{PZL}	Output Enable Time OE to Y ^[6]	C _L =300 pF R _L =500Ω	1.5	15.0	1.5	14.0	ns	1, 7, 8
t _{PHZ} t _{PHL}	Output Disable Time OE to Y ^[6]	C _L =5 pF R _L =500Ω	1.5	6.7	1.5	5.7	ns	1, 7, 8
t _{PHZ} t _{PHL}	Output Disable Time OE to Y	C _L =50 pF R _L =500Ω	1.5	7.0	1.5	6.0	ns	1, 7, 8

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information Section.

10-Bit Latch

Features

- Function, pinout and drive compatible with FCT, F, and AM29841 logic
- FCT-C speed at 5.5ns max. (Com'l)
- FCT-B speed at 6.5ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- ESD > 2000V

- Fully compatible with TTL input and output logic levels
- Sink current 64 mA (Com'l), 32 mA (Mil)
- Source current 32 mA (Com'l), 12 mA (Mil)
- High-speed parallel latches
- Buffered common latch enable input

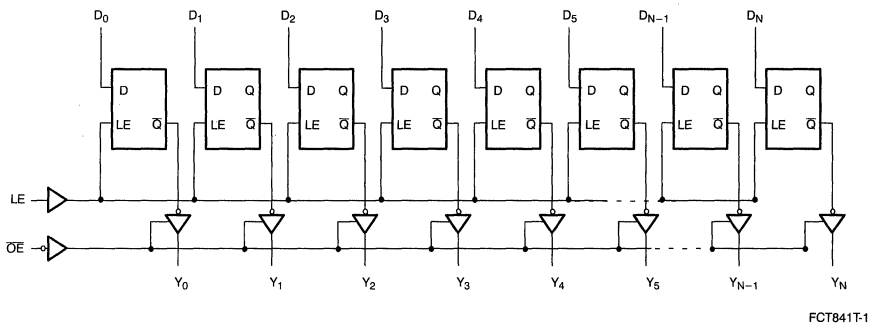
Functional Description

The FCT841T bus interface latch is designed to eliminate the extra packages required to buffer existing latches and

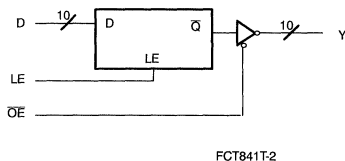
provide extra data width for wider address/data paths or buses carrying parity. The FCT841T is a buffered 10-bit wide version of the FCT373 function.

The FCT841T high-performance interface is designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high impedance state and are designed with a power-off disable feature to allow for live insertion of boards.

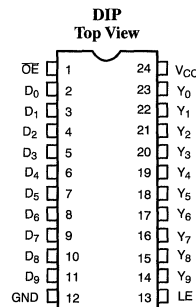
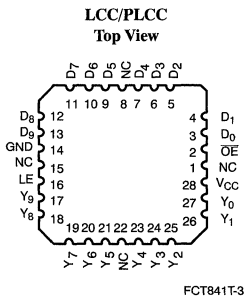
Functional Block Diagram



Logic Block Diagram



Pin Configurations



Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	Com'l	2.0			V
		V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3		V
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =32 mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage			2.0			V
V _{IL}	Input LOW Voltage					0.8	V
V _H	Hysteresis ^[6]	All inputs			0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA			-0.7	-1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}				5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V				±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V				±1	μA
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} = Max., V _{OUT} = 2.7V				10	μA
I _{OZL}	Off State LOW-Level Output Current	V _{CC} = Max., V _{OUT} = 0.5V				-10	μA
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V		-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V				±1	μA

Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Notes:

- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order

to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range^[12]

Parameter	Description	Test Load	FCT841AT				FCT841BT				Unit	Fig. No. ^[13]
			Military		Commercial		Military		Commercial			
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay D ₁ to Y ₁ (LE=HIGH)	C _L =50 pF R _L =500Ω	1.5	10.0	1.5	9.0	1.5	7.5	1.5	6.5	ns	1, 3
	Propagation Delay D ₁ to Y ₁ (LE=HIGH)	C _L =300 pF R _L =500Ω	1.5	15.0	1.5	13.0	1.5	15.0	1.5	13.0	ns	1, 3
t _{SU}	Data to LE Set-Up Time	C _L =50 pF R _L =500Ω	2.5		2.5		2.5		2.5		ns	9
t _H	Data to LE Hold Time	C _L =50 pF R _L =500Ω	3.0		2.5		2.5		2.5		ns	9
t _{PLH} t _{PHL}	Propagation Delay LE to Y ₁	C _L =50 pF R _L =500Ω	1.5	13.0	1.5	12.0	1.5	10.5	1.5	8.0	ns	1, 3
	Propagation Delay LE to Y ₁ ^[6]	C _L =300 pF R _L =500Ω	1.5	20.0	1.5	16.0	1.5	18.0	1.5	15.5	ns	1, 3
t _W	LE Pulse Width (HIGH)	C _L =50 pF R _L =500Ω	5.0		4.0		4.0		4.0		ns	5
t _{PZH} t _{PZL}	Output Enable Time OE to Y ₁	C _L =50 pF R _L =500Ω	1.5	13.0	1.5	11.5	1.5	8.5	1.5	8.0	ns	1, 7, 8
	Output Enable Time OE to Y ₁ ^[6]	C _L =300 pF R _L =500Ω	1.5	25.0	1.5	23.0	1.5	15.0	1.5	14.0	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time OE to Y ₁ ^[6]	C _L =5 pF R _L =500Ω	1.5	9.0	1.5	7.0	1.5	6.5	1.5	6.0	ns	1, 7, 8
	Output Disable Time OE to Y ₁	C _L =50 pF R _L =500Ω	1.5	10.0	1.5	8.0	1.5	7.5	1.5	7.0	ns	1, 7, 8

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
 13. See "Parameter Measurement Information" in the General Information Section.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.5	CY74FCT841CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT841CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT841CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.3	CY54FCT841CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT841CTLMB	L64	28-Square Leadless Chip Carrier	
6.5	CY74FCT841BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT841BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT841BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.5	CY54FCT841BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT841BTLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY74FCT841ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT841ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT841ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
10.0	CY54FCT841ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT841ATLMB	L64	28-Square Leadless Chip Carrier	

Document #: 38-00273-A



Function Table FCT2240T^[1]

Inputs			Output
\overline{OE}_A	\overline{OE}_B	D	
L	L	L	H
L	L	H	L
H	H	X	Z

Function Table FCT2244T^[1]

Inputs			Output
\overline{OE}_A	\overline{OE}_B	D	
L	L	L	L
L	L	H	H
H	H	X	Z

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with
 Power Applied -65°C to +135°C
 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Input Voltage -0.5V to +7.0V
 DC Output Voltage -0.5V to +7.0V
 DC Output Current (Maximum Sink Current/Pin) 120 mA
 Power Dissipation 0.5W

Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	-40°C to +85°C	5V ± 5%
Military ^[4]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3	V	
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3	V	
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =12 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =12 mA	Mil		0.3	0.55	V
R _{OUT}	Output Resistance	V _{CC} =Min., I _{OL} =12 mA	Com'l	20	25	40	Ω
		V _{CC} =Min., I _{OL} =12 mA	Mil		25		Ω
V _{IH}	Input HIGH Voltage		2.0			V	
V _{IL}	Input LOW Voltage				0.8	V	
V _H	Hysteresis ^[6]	All inputs		0.2		V	
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V	
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}			5	μA	
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V			±1	μA	
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V			±1	μA	
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} =Max., V _{OUT} =2.7V			10	μA	
I _{OZL}	Off State LOW-Level Output Current	V _{CC} =Max., V _{OUT} =0.5V			-10	μA	
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V	-60	-120	-225	mA	
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V			±1	μA	

Notes:

- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.



Switching Characteristics FCT2240T Over the Operating Range^[12]

Parameter	Description	FCT2240T				FCT2240AT				Unit	Fig. No. ^[13]
		Military		Commercial		Military		Commercial			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Input	1.5	9.0	1.5	8.0	1.5	5.1	1.5	4.8	ns	1, 2
t _{PZH} t _{PZL}	Output Enable Time	1.5	10.5	1.5	10.0	1.5	6.5	1.5	6.2	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	10.0	1.5	9.5	1.5	5.9	1.5	5.6	ns	1, 7, 8

Parameter	Description	FCT2240CT		Unit	Fig. No. ^[13]
		Commercial			
		Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Input	1.5	4.1	ns	1, 2
t _{PZH} t _{PZL}	Output Enable Time	1.5	5.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	5.2	ns	1, 7, 8

Switching Characteristics FCT2244T Over the Operating Range^[12]

Parameter	Description	FCT2244T				FCT2244A				Unit	Fig. No. ^[13]
		Military		Commercial		Military		Commercial			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Input	1.5	7.0	1.5	6.5	1.5	5.1	1.5	4.6	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time	1.5	8.5	1.5	8.0	1.5	6.5	1.5	6.2	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	7.5	1.5	7.0	1.5	5.9	1.5	5.6	ns	1, 7, 8

Parameter	Description	FCT2244CT		FCT2244DT		Unit	Fig. No. ^[13]
		Commercial		Commercial			
		Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Input	1.5	4.1	1.5	3.6	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time	1.5	5.8	1.5	4.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	5.2	1.5	4.0	ns	1, 7, 8

Shaded areas contain preliminary information.

Notes:

- 12. Minimum limits are guaranteed but not tested on Propagation Delays.
- 13. See "Parameter Measurement Information" in the General Information section.

8-Bit Transceiver
Features

- Function and pinout compatible with FCT and F logic
- 25Ω output series resistors to reduce transmission line reflection noise
- FCT-C speed at 4.1 ns max. (Com'l)
FCT-A speed at 4.6 ns max. (Com'l)
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Fully compatible with TTL input and output logic levels
- ESD > 2000V

- Sink current 12 mA (Com'l),
 12 mA (Mil)
- Source current 15 mA (Com'l),
 12 mA (Mil)

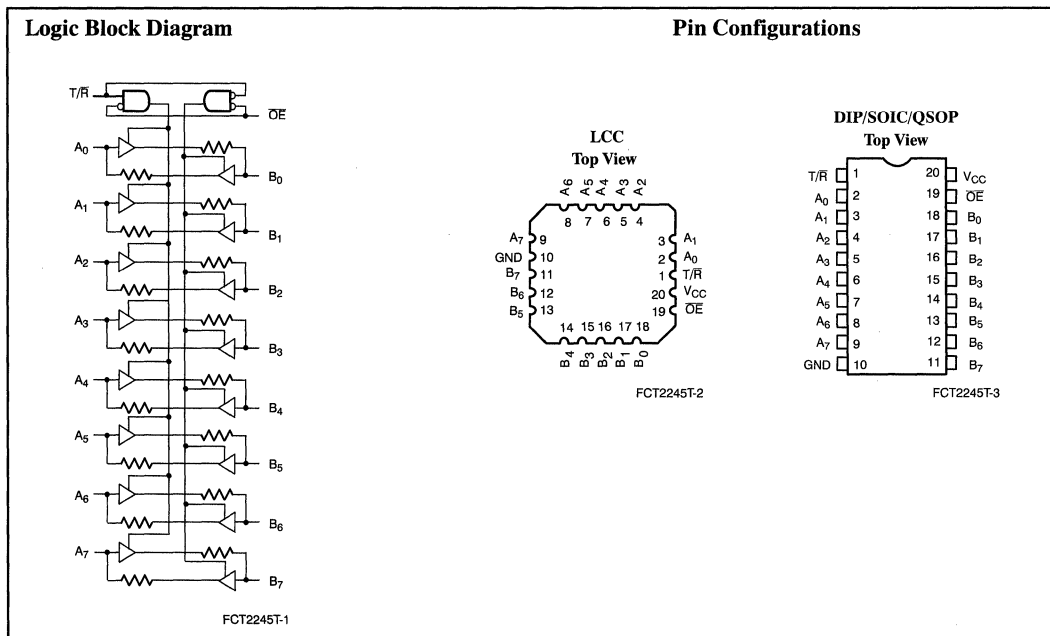
Three-state outputs
Functional Description

The FCT2245T contains eight non-inverting, bidirectional buffers with three-state outputs intended for bus oriented applications. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. For this reason, the FCT2245T can be used in an existing design to replace the FCT245T. The FCT2245T current sink-

ing capability is 12 mA at the A and B ports.

The Transmit/Receive (T/\bar{R}) input determines the direction of data flow through the bidirectional transceiver. Transmit (Active HIGH) enables data from A ports to B ports; receive (Active LOW) enables data from B ports to A ports. The output enable (\bar{OE}) input, when HIGH, disables both the A and B ports by putting them in a High Z condition.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.


Function Table ^[1]

Inputs		Output
\bar{OE}	T/\bar{R}	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

Note:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} \leq 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	$V_{CC} = \text{Max.}, V_{IN} = 3.4V$ ^[8] $f_1 = 0, \text{Outputs Open}$	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ^[9]	$V_{CC} = \text{Max.}, \text{One Input Toggling},$ 50% Duty Cycle, Outputs Open, $T/\bar{R} = OE = GND,$ $V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current ^[10]	$V_{CC} = \text{Max.}, 50\% \text{ Duty Cycle},$ Outputs Open, One Bit Toggling at $f_1 = 10 \text{ MHz},$ $T/\bar{R} = OE = GND,$ $V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	0.7	1.4	mA
		$V_{CC} = \text{Max.},$ 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 10 \text{ MHz},$ $T/\bar{R} = OE = GND,$ $V_{IN} = 3.4V \text{ or } V_{IN} = GND$	1.0	2.4	mA
		$V_{CC} = \text{Max.},$ 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5 \text{ MHz},$ $T/\bar{R} = OE = GND,$ $V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	1.3	2.6 ^[11]	mA
		$V_{CC} = \text{Max.},$ 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5 \text{ MHz},$ $T/\bar{R} = OE = GND,$ $V_{IN} = 3.4V \text{ or } V_{IN} = GND$	3.3	10.6 ^[11]	mA

Notes:

8. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Quad 2-Input Multiplexer

Features

- Function and pinout compatible with FCT and F logic
- 25Ω output series resistors to reduce transmission line reflection noise
- FCT-C speed at 4.3 ns max. (Com'l)
FCT-A speed at 5.0 ns max. (Com'l)
- TTL output level versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Fully compatible with TTL input and output logic levels
- ESD > 2000V

- Sink current 12 mA (Com'l),
12 mA (Mil)
- Source current 15 mA (Com'l),
12 mA (Mil)
- Three-state outputs

Functional Description

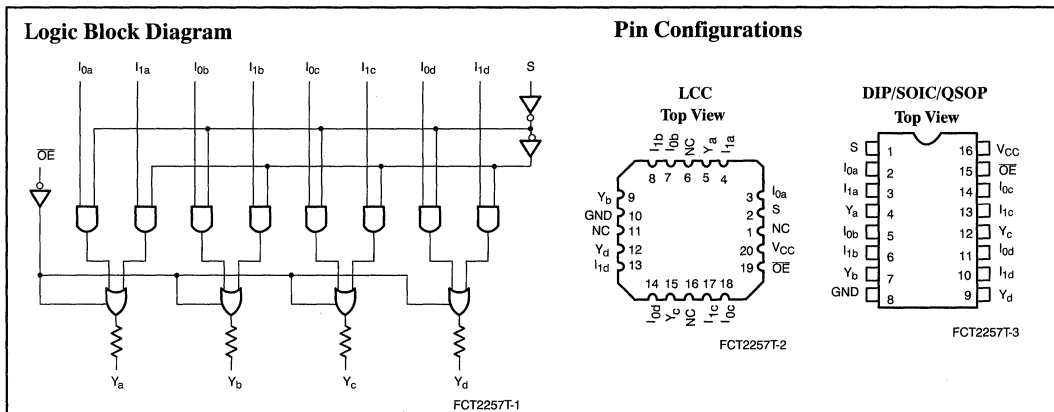
The FCT2257T has four identical two-input multiplexers that select four bits of data from two sources under the control of a common data Select input (S). The I₀ inputs are selected when the Select input is LOW and the I₁ inputs are selected when the Select input is HIGH. Data appears at the output in true non-inverted form for the FCT2257T. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. The FCT2257T can be used to replace the

FCT2257T to reduce noise in an existing design

The FCT2257T is a logic implementation of a four-pole, two-position switch where the position of the switch is determined by the logic levels supplied to the select input. Outputs are forced to a high-impedance "OFF" state when the Output Enable input (OE) is HIGH.

All but one device must be in the high-impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of three-state devices are tied together.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.


Pin Description

Name	Description
I	Data Inputs
S	Common Select Input
OE	Enable Inputs (Active LOW)
Y	Data Outputs

Function Table^[1]

Inputs				Output
OE	S	I ₀	I ₁	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

Notes:

1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, Z = High impedance (OFF) state

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} \leq 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	$V_{CC} = \text{Max.}, V_{IN} = 3.4V,$ ^[8] $f_1 = 0, \text{Outputs Open}$	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ^[9]	$V_{CC} = \text{Max.}, \text{One Input Toggling},$ $50\% \text{ Duty Cycle, Outputs Open, } OE = GND,$ $V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current ^[10]	$V_{CC} = \text{Max.}, 50\% \text{ Duty Cycle,}$ Outputs Open, $\text{One Bit Toggling at } f_1 = 10 \text{ MHz,}$ $OE = GND,$ $V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	0.7	1.4	mA
		$V_{CC} = \text{Max.},$ $50\% \text{ Duty Cycle, Outputs Open,}$ $\text{One Bit Toggling at } f_1 = 10 \text{ MHz,}$ $OE = GND,$ $V_{IN} = 3.4V \text{ or } V_{IN} = GND$	1.0	2.4	mA
		$V_{CC} = \text{Max.},$ $50\% \text{ Duty Cycle, Outputs Open,}$ $\text{Four Bits Toggling at } f_1 = 2.5 \text{ MHz,}$ $OE = GND,$ $V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	0.7	1.4 ^[11]	mA
		$V_{CC} = \text{Max.},$ $50\% \text{ Duty Cycle, Outputs Open,}$ $\text{Four Bits Toggling at } f_1 = 2.5 \text{ MHz,}$ $OE = GND,$ $V_{IN} = 3.4V \text{ or } V_{IN} = GND$	1.7	5.4 ^[11]	mA

Notes:

8. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
 9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

10. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HN} N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamps and all frequencies are in megahertz.

11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

8-Bit Latches

Features

- Function and pinout compatible with the fastest bipolar logic
- 25Ω output series resistors to reduce transmission line reflection noise
- FCT-C speed at 4.7 ns max. (Com'l)
FCT-A speed at 5.2 ns max. (Com'l)
- Reduced V_{OH} (typically=3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- ESD > 2000V

- Fully compatible with TTL input and output logic levels

- Sink current 12 mA (Com'l),
 12 mA (Mil)
- Source current 15 mA (Com'l),
 12 mA (Mil)

Functional Description

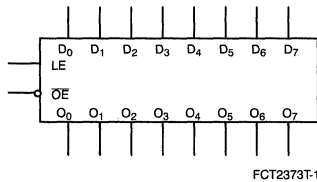
The FCT2373T and FCT2573T are 8-bit, high-speed CMOS TTL-compatible buffered latches with three-state outputs that are ideal for driving high-capacitance loads, such as memory and address buffers. On-chip 25Ω termination resistors have been added to the outputs to reduce system noise caused by reflections. FCT2373T can be used to replace

FCT373T, and FCT2573T to replace FCT573T to reduce noise in an existing design.

When latch enable (LE) is HIGH, the flip-flops appear transparent to the data. Data that meets the required set-up times are latched when LE transitions from HIGH to LOW. Data appears on the bus when the output enable (OE) is LOW. When output enable is HIGH, the bus output is in the high impedance state. In this mode, data can still be entered into the latches.

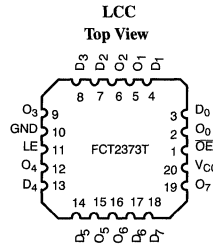
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Symbol



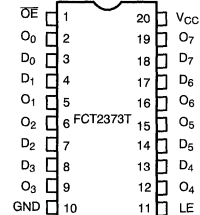
FCT2373T-1

Pin Configurations



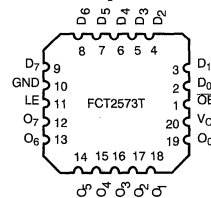
FCT2373T-4

DIP/SOIC/QSOP Top View



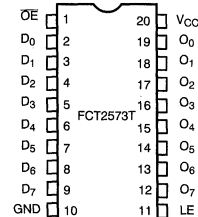
FCT2373T-5

LCC Top View



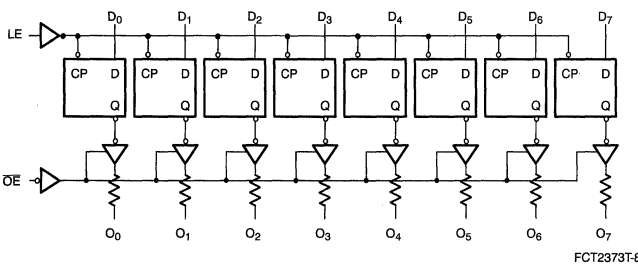
FCT2373T-6

DIP/SOIC/QSOP Top View



FCT2373T-7

Logic Block Diagram



FCT2373T-8

Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	6	10	pF
C _{OUT}	Output Capacitance	8	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	0.1	0.2	mA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs)	V _{CC} =Max., V _{IN} =3.4V, ^[8] f ₁ =0, Outputs Open	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.06	0.12	mA/ MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =10 MHz, OE=GND, LE=V _{CC} , V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.7	1.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =10 MHz, OE=GND, LE=V _{CC} , V _{IN} =3.4V or V _{IN} =GND	1.0	2.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, OE=GND, LE=V _{CC} , V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	1.3	2.6 ^[11]	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, OE=GND, LE=V _{CC} , V _{IN} =3.4V or V _{IN} =GND	3.3	10.6 ^[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CCD_HN_T} + I_{CCD}(f₀/2 + f₁N₁)
I_{CC} = Quiescent Current with CMOS input levels
ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
D_H = Duty Cycle for TTL inputs HIGH

- N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
f₀ = Clock frequency for registered devices, otherwise zero
f₁ = Input signal frequency
N₁ = Number of inputs changing at f₁
All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT2373DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2373DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.2	CY74FCT2373CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2373CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2373CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.1	CY54FCT2373CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2373CTLMB	L61	20-Pin Square Leadless Chip Carrier	
5.2	CY74FCT2373ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2373ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2373ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.6	CY54FCT2373ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2373ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.0	CY74FCT2373TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2373TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2373TSOC	S5	20-Lead (300-Mil) Molded SOIC	
8.5	CY54FCT2373TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2373TLMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT2573DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2573DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.2	CY74FCT2573CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2573CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2573CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.1	CY54FCT2573CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2573CTLMB	L61	20-Pin Square Leadless Chip Carrier	
5.2	CY74FCT2573ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2573ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2573ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.6	CY54FCT2573ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2573ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.0	CY74FCT2573TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2573TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2573TSOC	S5	20-Lead (300-Mil) Molded SOIC	
8.5	CY54FCT2573TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2573TLMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

Document #: 38-00338-A

Function Table^[1]

Inputs			Outputs
D	CP	\overline{OE}	O
H	\lrcorner	L	H
L	\lrcorner	L	L
X	X	H	Z

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +135°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W

 Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	-40°C to +85°C	5V ± 5%
Military ^[4]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3	V	
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3	V	
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =12 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =12 mA	Mil		0.3	0.55	V
R _{OUT}	Output Resistance	V _{CC} =Min., I _{OL} =12 mA	Com'l	20	25	40	Ω
		V _{CC} =Min., I _{OL} =12 mA	Mil		25		Ω
V _{IH}	Input HIGH Voltage		2.0			V	
V _{IL}	Input LOW Voltage				0.8	V	
V _H	Hysteresis ^[6]	All inputs		0.2		V	
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V	
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}			5	μA	
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V			±1	μA	
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V			±1	μA	
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} = Max., V _{OUT} = 2.7V			10	μA	
I _{OZL}	Off State LOW-Level Output Current	V _{CC} = Max., V _{OUT} = 0.5V			-10	μA	
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V	-60	-120	-225	mA	
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V			±1	μA	

Notes:

- H = HIGH Voltage Level.
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance
 \lrcorner = LOW-to-HIGH clock transition
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.



Switching Characteristics Over the Operating Range

Parameter	Description	FCT2374T/FCT2574T				FCT2374AT/FCT2574AT				Unit	Fig. No. ^[13]
		Military		Commercial		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Clock to Output	2.0	11.0	2.0	10.0	2.0	7.2	2.0	6.5	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time	1.5	14.0	1.5	12.5	1.5	7.5	1.5	6.5	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	8.0	1.5	8.0	1.5	6.5	1.5	5.5	ns	1, 7, 8
t _S	Set-Up Time, HIGH or LOW D to CP	2.0		2.0		2.0		2.0		ns	4
t _H	Hold Time, HIGH or LOW D to CP	1.5		1.5		1.5		1.5		ns	4
t _W	Clk Pulse Width HIGH or LOW	6.0		7.0		6.0		5.0		ns	5

Parameter	Description	FCT2374CT/FCT2574CT				FCT2374DT/ FCT2574DT		Unit	Fig. No. ^[13]
		Military		Commercial		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Clock to Output	2.0	6.5	2.0	5.2	2.0	4.2	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time	1.5	6.9	1.5	6.2	1.5	4.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	6.5	1.5	5.0	1.5	4.0	ns	1, 7, 8
t _S	Set-Up Time, HIGH or LOW D to CP	2.0		1.5		2.0		ns	4
t _H	Hold Time, HIGH or LOW D to CP	1.0		1.0		1.0		ns	4
t _W	Clk Pulse Width HIGH or LOW	5.0		4.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information section.

8-Bit Buffer/Line Driver

Features

- Function and pinout compatible with FCT and F logic
- FCT-C speed at 4.1 ns max. (Com'l)
FCT-A speed at 4.8 ns max. (Com'l)
- 25Ω output series to reduce transmission line reflection noise
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- ESD > 2000V

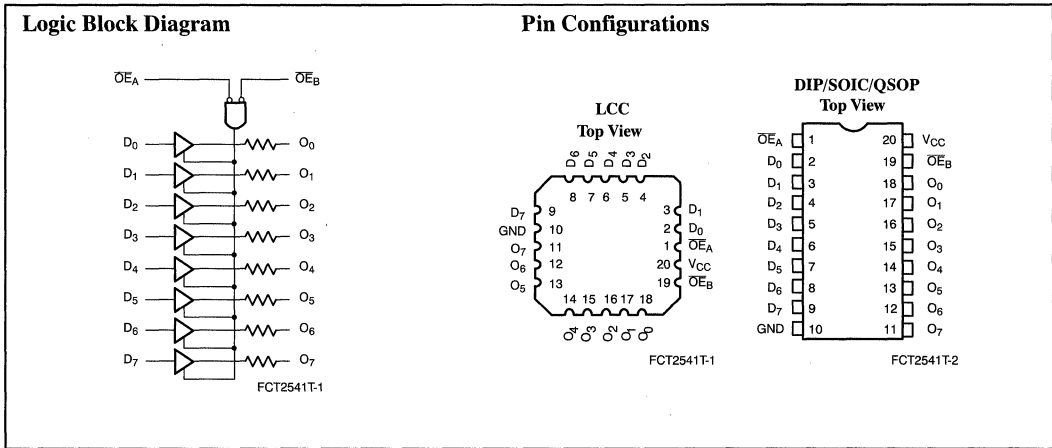
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Sink current 12 mA (Com'l),
 12 mA (Mil)
- Source current 15 mA (Com'l),
 12 mA (Mil)
- Three-state outputs

Functional Description

The FCT2541T is an octal buffer and line driver designed to be employed as a memory address driver, clock driver, and bus-oriented transmitter/receiver. On-chip

termination resistors have been added to the outputs to reduce system noise caused by reflections. The FCT2541T can be used to replace the FCT541T to reduce noise in an existing design. The speed of the FCT2541T is comparable to bipolar logic counterparts while reducing power dissipation. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.



Function Table^[1]

Inputs			Output
\overline{OE}_A	\overline{OE}_B	D	
L	L	L	L
L	L	H	H
H	H	X	Z

Note:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedence

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} \leq 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	$V_{CC} = \text{Max.}, V_{IN} = 3.4V,$ ^[8] $f_1 = 0,$ Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ^[9]	$V_{CC} = \text{Max.}, 50\%$ Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}_A = \overline{OE}_B = \text{GND}, V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current ^[10]	$V_{CC} = \text{Max.}, 50\%$ Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 10$ MHz, $\overline{OE}_A = \overline{OE}_B = \text{GND}, V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	0.7	1.4	mA
		$V_{CC} = \text{Max.}, 50\%$ Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 10$ MHz, $\overline{OE}_A = \overline{OE}_B = \text{GND}, V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	1.0	2.4	mA
		$V_{CC} = \text{Max.}, 50\%$ Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5$ MHz, $\overline{OE}_A = \overline{OE}_B = \text{GND}, V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	1.3	2.6 ^[11]	mA
		$V_{CC} = \text{Max.}, 50\%$ Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5$ MHz, $\overline{OE}_A = \overline{OE}_B = \text{GND}, V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	3.3	10.6 ^[11]	mA

Notes:

8. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
 9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
 10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH

- N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamps and all frequencies are in megahertz.

11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

8-Bit Latched Transceiver

Features

- Function and pinout compatible with FCT and F logic
- FCT-C speed at 5.3 ns max. (Com'l)
FCT-A speed at 6.5 ns max. (Com'l)
- 25W output series resistors to reduce transmission line reflection noise
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Sink current 12 mA (Com'l),
 12 mA (Mil)
- Source current 15 mA (Com'l),
 12 mA (Mil)

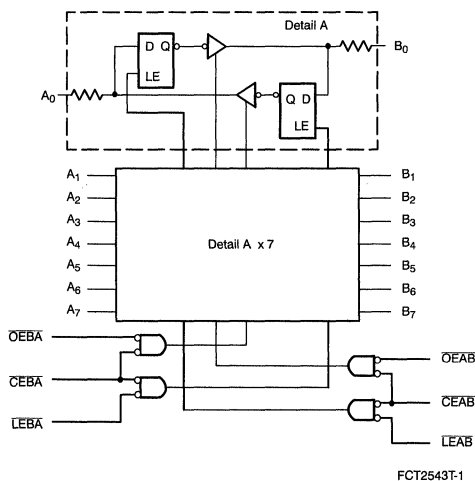
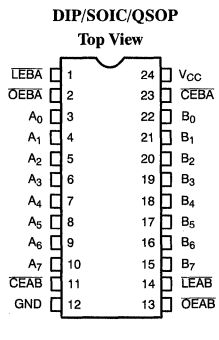
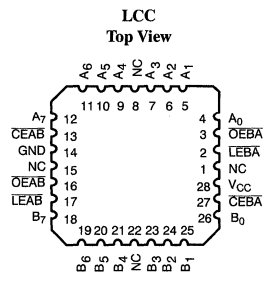
- Separation controls for data flow in each direction
- Back to back latches for storage
- ESD > 2000V

Functional Description

The FCT2543T Octal Latched Transceiver contains two sets of eight D-type latches. Separate Latch Enable (LEAB, LEBA) and Output Enable (OEAB, OEBA) permits each latch set to have independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B Enable (CEAB) input must be LOW to enter data from A or to take data from B, as indicated in the truth table. With CEAB LOW, a LOW signal on the A-to-B Latch Enable (LEAB) input makes the A-to-B

latches transparent; a subsequent LOW-to-HIGH transition of the LEAB signal puts the A latches in the storage mode and their output no longer change with the A inputs. With CEAB and OEAB both LOW, the three-state B output buffers are active and reflect data present at the output of the A latches. Control of data from B to A is similar, but uses CEAB, LEAB, and OEAB inputs. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. The FCT2543T can be used to replace the FCT543T to reduce noise in an existing design.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Functional Block Diagram

Pin Configurations


Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[7]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3		V
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =12 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =12 mA	Mil		0.3	0.55	V
R _{OUT}	Output Resistance	V _{CC} =Min., I _{OL} =12 mA	Com'l	20	25	40	Ω
		V _{CC} =Min., I _{OL} =12 mA	Mil		25		Ω
V _{IH}	Input HIGH Voltage			2.0			V
V _{IL}	Input LOW Voltage					0.8	V
V _H	Hysteresis ^[8]	All inputs			0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA			-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}				5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V				±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V				±1	μA
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} = Max., V _{OUT} = 2.7V				15	μA
I _{OZL}	Off State LOW-Level Output Current	V _{CC} = Max., V _{OUT} = 0.5V				-15	μA
I _{OS}	Output Short Circuit Current ^[9]	V _{CC} =Max., V _{OUT} =0.0V		-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V				±1	μA

Capacitance^[8]

Parameter	Description	Test Conditions	Typ. ^[7]	Max.	Unit
C _{IN}	Input Capacitance		5	10	pF
C _{OUT}	Output Capacitance		9	12	pF

Notes:

- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order

to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametrics tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT2543T				FCT2543AT				Unit	Fig. No. ^[15]
		Military		Commercial		Military		Commercial			
		Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Transparent Mode A to B or B to A	2.0	10.0	2.5	8.5	2.5	7.5	2.5	6.5	ns	1, 3
t _{PLH} t _{PHL}	Propagation Delay LEBA to A LEAB to B	2.5	14.0	2.5	12.5	2.5	9.0	2.5	8.0	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	2.0	14.0	2.0	12.0	2.0	10.0	2.0	9.0	ns	1, 7, 8
t _{PZH} t _{PZL}	Output Disable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	2.0	13.0	2.0	9.0	2.0	8.5	2.0	7.5	ns	1, 7, 8
t _S	Set-Up Time HIGH or LOW, A or B to LEBA or LEAB	3.0		2.0		2.0		2.0		ns	9
t _H	Hold Time HIGH or LOW, A or B to LEBA or LEAB	2.0		2.0		2.0		2.0		ns	9
t _W	Pulse Width LOW LEBA or LEAB	5.0		5.0		5.0		5.0		ns	5

Parameter	Description	FCT2543CT				FCT2543DT		Unit	Fig. No. ^[15]
		Military		Commercial		Commercial			
		Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Transparent Mode A to B or B to A	2.5	6.1	2.5	5.5	1.5	4.4	ns	1, 3
t _{PLH} t _{PHL}	Propagation Delay LEBA to A, LEAB to B	2.5	8.0	2.5	7.0	1.5	5.0	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	2.0	9.0	2.0	8.0	1.5	5.4	ns	1, 7, 8
t _{PZH} t _{PZL}	Output Disable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	2.0	7.5	2.0	6.5	1.5	4.3	ns	1, 7, 8
t _S	Set-Up Time HIGH or LOW, A or B to LEBA or LEAB	2.0		2.0		1.5		ns	9
t _H	Hold Time HIGH or LOW, A or B to LEBA or LEAB	2.0		2.0		1.5		ns	9
t _W	Pulse Width LOW LEBA or LEAB	5.0		5.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

14. Minimum limits are guaranteed but not tested on Propagation Delays. 15. See "Parameter Measurement Information" in the General Information Section.



8-Bit Registered Transceivers

Features

- Function and pinout compatible with FCT and F logic
- FCT-C speed at 5.4 ns max. (Com'l)
- FCT-A speed at 6.3 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- 25Ω output series resistors to reduce transmission line reflection noise
- Reduced V_{OH} (typically=3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- ESD > 2000V

- Fully compatible with TTL input and output logic levels
- Sink current 12 mA (Com'l), 12 mA (Mil)
- Source current 15 mA (Com'l), 12 mA (Mil)
- Independent register for A and B buses
- Three-state output

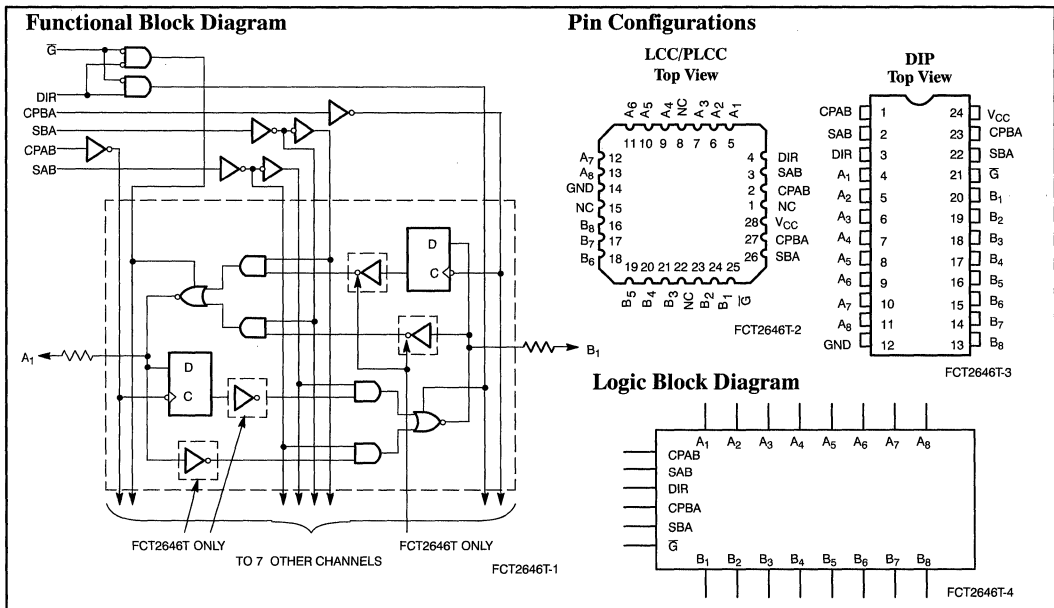
Functional Description

The FCT2646T and FCT2648T consist of a bus transceiver circuit with three-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH logic level. Enable Control \bar{G} and direction pins are provided to control the

transceiver function. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections so that the FCT2646T and the FCT2648T can be used to replace the FCT646T and the FCT648T, respectively, in an existing design.

In the transceiver mode, data present at the high impedance port may be stored in either the A or B register, or in both. Select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control \bar{G} is Active LOW. In the isolation mode (enable control \bar{G} HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.



Pin Description

Name	Description
A	Data Register A Inputs, Data Register B Outputs
B	Data Register B Inputs, Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, \bar{G}	Output Enable Inputs



Maximum Ratings^[4, 5]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied -65°C to +135°C
 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Input Voltage -0.5V to +7.0V
 DC Output Voltage -0.5V to +7.0V
 DC Output Current (Maximum Sink Current/Pin) 120 mA
 Power Dissipation 0.5W

Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	-40°C to +85°C	5V ± 5%
Military ^[6]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[7]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-15 mA Com'l	2.4	3.3		V
		V _{CC} =Min., I _{OH} =-12 mA Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =12 mA Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =12 mA Mil		0.3	0.55	V
R _{OUT}	Output Resistance	V _{CC} =Min., I _{OL} =12 mA Com'l	20	25	40	Ω
		V _{CC} =Min., I _{OL} =12 mA Mil		25		Ω
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Hysteresis ^[8]	All inputs		0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}			5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V			±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V			±1	μA
I _{OS}	Output Short Circuit Current ^[9]	V _{CC} =Max., V _{OUT} =0.0V	-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V			±1	μA

Capacitance^[8]

Parameter	Description	Typ. ^[7]	Max.	Unit
C _{IN}	Input Capacitance	6	10	pF
C _{OUT}	Output Capacitance	8	12	pF

Notes:

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.



Switching Characteristics Over the Operating Range

Parameter	Description	FCT2646T/FCT2648T				FCT2646AT/FCT2648AT				Unit	Fig. No. ^[15]
		Military		Commercial		Military		Commercial			
		Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	1.5	11.0	1.5	9.0	1.5	7.7	1.5	6.3	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time Enable to Bus and DIR to A _n or B _n	1.5	15.0	1.5	14.5	1.5	10.5	1.5	9.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time G̅ to Bus and DIR to Bus	1.5	11.0	1.5	9.0	1.5	7.7	1.5	6.3	ns	1, 7, 8
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus	1.5	10.0	1.5	9.0	1.5	7.0	1.5	6.3	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay SBA or SAB to A or B	1.5	12.0	1.5	11.0	1.5	8.4	1.5	7.7	ns	1, 5
t _S	Set-Up Time HIGH or LOW, Bus to Clock	4.5		4.0		2.0		2.0		ns	4
t _H	Hold Time HIGH or LOW, Bus to Clock	2.0		2.0		1.5		1.5		ns	4
t _W	Pulse Width, ^[6] HIGH or LOW	6.0		6.0		5.0		5.0		ns	5

Parameter	Description	FCT2646CT/FCT2648CT				Unit	Fig. No. ^[15]
		Military		Commercial			
		Min. ^[14]	Max.	Min. ^[14]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	1.5	6.0	1.5	5.4	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time Enable to Bus and DIR to A _n or B _n	1.5	8.9	1.5	7.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time G̅ to Bus and DIR to Bus	1.5	7.7	1.5	6.3	ns	1, 7, 8
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus	1.5	6.3	1.5	5.7	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay SBA or SAB to A or B	1.5	7.0	1.5	6.2	ns	1, 5
t _S	Set-Up Time HIGH or LOW, Bus to Clock	2.0		2.0		ns	4
t _H	Hold Time HIGH or LOW, Bus to Clock	1.5		1.5		ns	4
t _W	Pulse Width, ^[6] HIGH or LOW	5.0		5.0		ns	5

- Notes:
 14. Minimum limits are guaranteed but not tested on Propagation Delays.
 15. See "Parameter Measurement Information" in the General Information Section.

8-Bit Registered Transceiver

Features

- Function and pinout compatible with FCT and F logic
- FCT-C speed at 5.4 ns max. (Com'l)
FCT-A speed at 6.3 ns max. (Com'l)
- 25Ω output series resistors to reduce transmission line reflection noise
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Sink current 12 mA (Com'l),
 12 mA (Mil)
- Source current 15 mA (Com'l),
 12 mA (Mil)
- ESD > 2000V

- Independent register for A and B buses
- Multiplexed real-time and stored data transfer

Functional Description

The FCT2652T consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. GAB and GBA control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer.

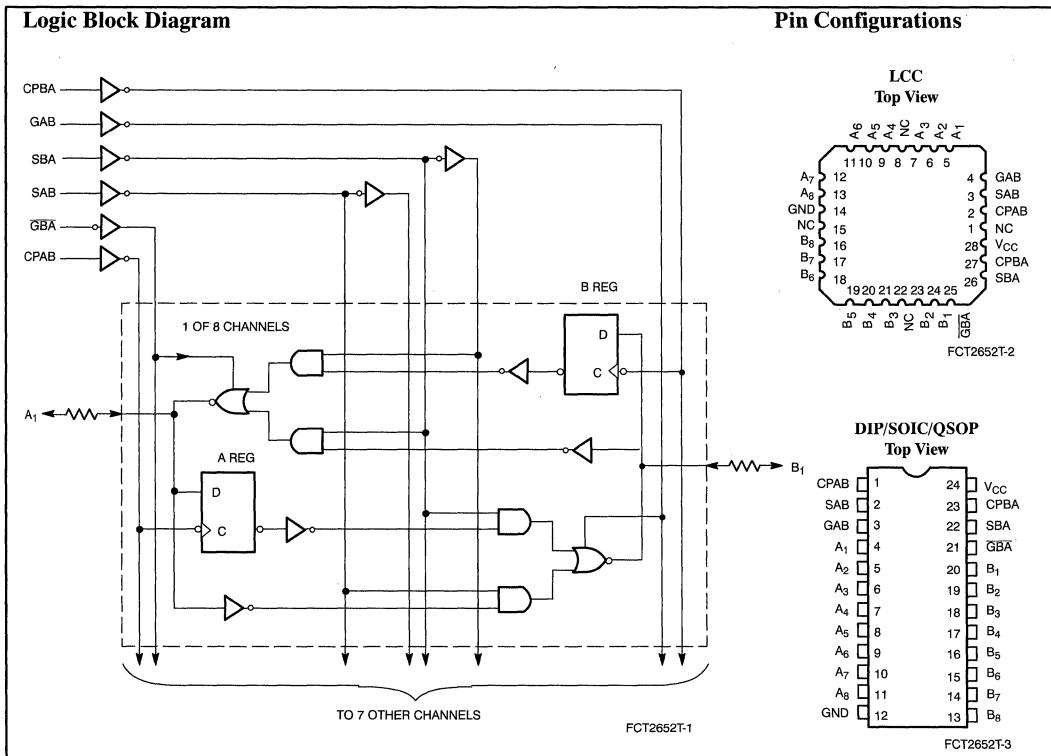
On-chip termination resistors are added to the outputs to reduce system noise caused by reflections. The FCT2652T can replace the FCT652T to reduce noise in an existing design.

The circuitry used for select control will eliminate the typical decoding glitch that

occurs in a multiplexer during transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.



Function Table^[1]

Inputs						Data I/O		Operation or Function
GAB	GBA	CPAB	CPBA	SAB	SBA	A ₁ thru A ₈	B ₁ thru B ₈	
L L	H H	H or L ┐	H or L ┐	X X	X X	Input	Input	Isolation Store A and B Data
X H	H H	┐ ┐	H or L ┐	X X ^[1]	X X	Input Input	Unspecified ^[2] Output	Store A, Hold B Store A in both registers
L L	X L	H or L ┐	┐ ┐	X X	X X ^[1]	Unspecified ^[2] Output	Input Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real-Time B Data to A Bus Stored B Data to A Bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real-Time A Data to B Bus Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

Maximum Ratings^[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +135°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
DC Output Voltage	−0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military ^[5]	All	−55°C to +125°C	5V ± 10%

Notes:

- Select control=L: clocks can occur simultaneously. Select control=H: clocks must be staggered in order to load both registers. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
- The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[6]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} \leq 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC} = \text{Max.}, V_{IN} = 3.4V$ ^[9] $f_1 = 0, \text{Outputs Open}$	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ^[10]	$V_{CC} = \text{Max.}, \text{One Input Toggling},$ 50% Duty Cycle, Outputs Open, GAB=GND, GBA=GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current ^[11]	$V_{CC} = \text{Max.}, f_0 = 10 \text{ MHz},$ 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5 \text{ MHz},$ GAB=GND, GBA=GND, SAB=CPAB=GND SBA= $V_{CC},$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	0.7	1.4	mA
		$V_{CC} = \text{Max.}, f_0 = 10 \text{ MHz},$ 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5 \text{ MHz},$ GAB=GND, GBA=GND, SAB=CPAB=GND SBA= $V_{CC},$ $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	1.2	3.4	mA
		$V_{CC} = \text{Max.}, f_0 = 10 \text{ MHz},$ 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 5 \text{ MHz},$ GAB=GBA=GND, SAB=CPAB=GND SBA= $V_{CC},$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	2.8	5.6 ^[12]	mA
		$V_{CC} = \text{Max.}, f_0 = 10 \text{ MHz}, 50\% \text{ Duty Cycle},$ Outputs Open, Eight Bits Toggling at $f_1 = 5 \text{ MHz},$ GAB=GBA=GND, SAB=CPAB=GND SBA= $V_{CC},$ $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	5.1	14.6 ^[12]	mA

Notes:

9. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
 10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

11. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH

- N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamps and all frequencies are in megahertz.
 12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.4	CY74FCT2652DTQC	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT2652DTSOC	S13	24-Lead (300-Mil) Molded SOIC	
5.4	CY74FCT2652CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2652CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2652CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT2652CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2652CTLMB	L64	28-Square Leadless Chip Carrier	
6.3	CY74FCT2652ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2652ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2652ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.7	CY54FCT2652ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2652ATLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY74FCT2652TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2652TOC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2652TSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT2652TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2652TLMB	L64	28-Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

Document #: 38-00344-A

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +135°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	AT, BT	-40°C to +85°C	5V ± 5%
Military ^[4]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3	V	
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3	V	
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =12 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =12 mA	Mil		0.3	0.55	V
R _{OUT}	Output Resistance	V _{CC} =Min., I _{OL} =12 mA	Com'l	20	25	40	Ω
		V _{CC} =Min., I _{OL} =12 mA	Mil		25		Ω
V _{IH}	Input HIGH Voltage		2.0			V	
V _{IL}	Input LOW Voltage				0.8	V	
V _H	Hysteresis ^[6]	All inputs		0.2		V	
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V	
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}			5	μA	
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V			±1	μA	
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V			±1	μA	
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} = Max., V _{OUT} = 2.7V			10	μA	
I _{OZL}	Off State LOW-Level Output Current	V _{CC} = Max., V _{OUT} = 0.5V			-10	μA	
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V	-60	-120	-225	mA	
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V			±1	μA	

Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Notes:

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range

Param.	Description	Test Load	FCT2827AT				FCT2827BT				Unit	Fig. No. ^[12]
			Military		Commercial		Military		Commercial			
			Min. ^[13]	Max.	Min. ^[13]	Max.	Min. ^[13]	Max.	Min. ^[13]	Max.		
t _{PLH} t _{PHL}	Propagation Delay D to Y	C _L =50 pF R _L =500Ω	1.5	9.0	1.5	8.0	1.5	6.5	1.5	5.0	ns	1, 3
t _{PLH} t _{PHL}	Propagation Delay D to Y ^[6]	C _L =300 pF R _L =500Ω	1.5	17.0	1.5	15.0	1.5	14.0	1.5	13.0	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time OE to Y	C _L =50 pF R _L =500Ω	1.5	13.0	1.5	12.0	1.5	9.0	1.5	8.0	ns	1, 7, 8
t _{PZH} t _{PZL}	Output Enable Time OE to Y ^[6]	C _L =300 pF R _L =500Ω	1.5	25.0	1.5	23.0	1.5	16.0	1.5	15.0	ns	1, 7, 8
t _{PHZ} t _{PHL}	Output Disable Time OE to Y ^[6]	C _L =5 pF R _L =500Ω	1.5	10.0	1.5	9.0	1.5	7.0	1.5	6.0	ns	1, 7, 8
t _{PHZ} t _{PHL}	Output Disable Time OE to Y	C _L =50 pF R _L =500Ω	1.5	10.0	1.5	9.0	1.5	8.0	1.5	7.0	ns	1, 7, 8

Param.	Description	Test Load	FCT2827CT				Unit	Fig. No. ^[12]
			Military		Commercial			
			Min. ^[13]	Max.	Min. ^[13]	Max.		
t _{PLH} t _{PHL}	Propagation Delay D to Y	C _L =50 pF R _L =500Ω	1.5	5.0	1.5	4.4	ns	1, 3
t _{PLH} t _{PHL}	Propagation Delay D to Y ^[6]	C _L =300 pF R _L =500Ω	1.5	11.0	1.5	10.0	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time OE to Y	C _L =50 pF R _L =500Ω	1.5	8.0	1.5	7.0	ns	1, 7, 8
t _{PZH} t _{PZL}	Output Enable Time OE to Y ^[6]	C _L =300 pF R _L =500Ω	1.5	15.0	1.5	14.0	ns	1, 7, 8
t _{PHZ} t _{PHL}	Output Disable Time OE to Y ^[6]	C _L =5 pF R _L =500Ω	1.5	6.7	1.5	5.7	ns	1, 7, 8
t _{PHZ} t _{PHL}	Output Disable Time OE to Y	C _L =50 pF R _L =500Ω	1.5	7.0	1.5	6.0	ns	1, 7, 8

Notes:

12. See "Parameter Measurement Information" in the General Information section.
13. Minimum limits are guaranteed but not tested on Propagation Delays.



CY74FCT16240T CY74FCT162240T

16-Bit Buffers/Line Drivers

Features

- Low power, pin compatible replacement for ABT functions
- FCT-C speed at 4.3 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000 V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 5\text{V} \pm 10\%$

CY74FCT16240T Features:

- 64 mA sink current (Com'l), 32 mA source current (Com'l)
- Typical V_{OLP} (ground bounce) < 1.0V at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$

CY74FCT162240T Features:

- Balanced output drivers: 24 mA
- Reduced system switching noise
- Typical V_{OLP} (ground bounce) < 0.6V at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$

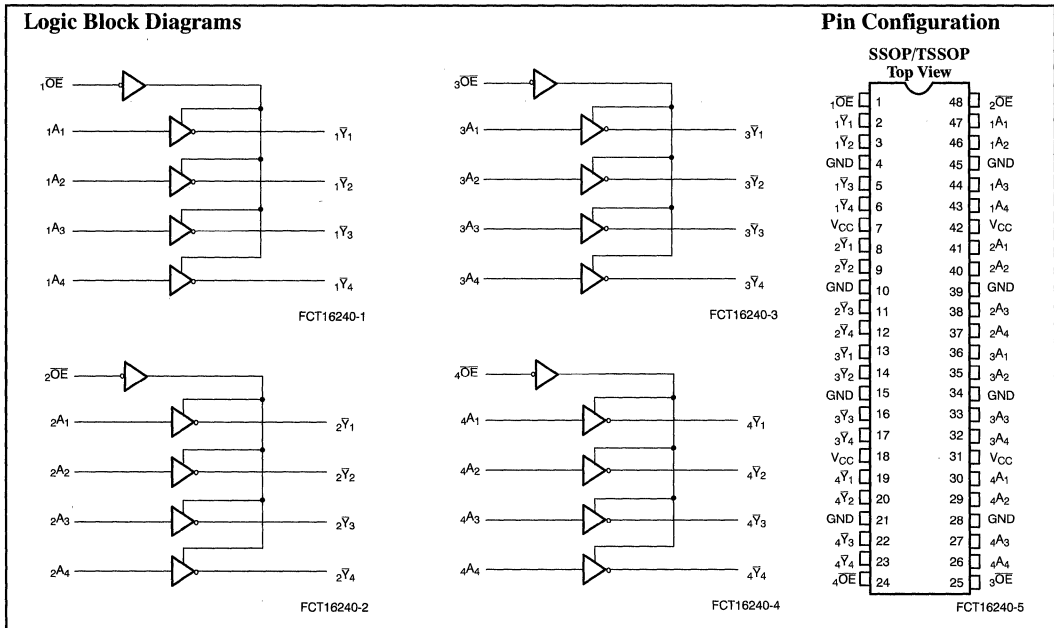
Functional Description

These 16-bit buffer/line drivers are used in memory driver, clock driver, or other bus interface applications, where high speed and low power are required. With flow-through

pinout and small shrink packaging, board layout is simplified. The three-state controls are designed to allow 4-, 8-, or 16-bit operation. The outputs are designed with a power-off disable feature to allow for live insertion of boards.

The CY74FCT16240T is ideally suited for driving high capacitance loads and low-impedance backplanes.

The CY74FCT162240T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162240T is ideal for driving transmission lines.



Pin Summary

Name	Description
$\overline{\text{OE}}$	Three-State Output Enable Inputs (Active LOW)
A	Data Inputs
$\overline{\text{Y}}$	Three-State Outputs

Note:

1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, Z = High Impedance.

Function Table^[1]

Inputs		Outputs
$\overline{\text{OE}}$	A	$\overline{\text{Y}}$
L	L	H
L	H	L
H	X	Z

Capacitance^[5] ($T_A = +25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

Parameter	Description	Test Conditions	Typ. ^[4]	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4.5	6.0	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ. ^[4]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$	5	500	μA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC} = \text{Max.}$	$V_{IN} = 3.4V^{[7]}$	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ^[8]	$V_{CC} = \text{Max.}$, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE} = \text{GND}$	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	60	100	$\mu\text{A}/\text{MHz}$
I_C	Total Power Supply Current ^[9]	$V_{CC} = \text{Max.}$, $f_1 = 10\text{ MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE} = \text{GND}$	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	0.6	1.5	mA
			$V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	0.9	2.3	mA
		$V_{CC} = \text{Max.}$, $f_1 = 2.5\text{ MHz}$, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE} = \text{GND}$	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	2.4	4.5 ^[10]	mA
			$V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	6.4	16.5 ^[10]	mA

Switching Characteristics Over the Operating Range

Parameter	Description	CY74FCT16240T CY74FCT162240T		CY74FCT16240AT CY74FCT162240AT		CY74FCT16240CT CY74FCT162240CT		Unit	Fig. No. ^[12]
		Min. ^[11]	Max.	Min. ^[11]	Max.	Min. ^[11]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.5	8.0	1.5	4.8	1.5	4.3	ns	1, 2
t_{PZH} t_{PZL}	Output Enable Time	1.5	10.0	1.5	6.2	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	9.5	1.5	5.6	1.5	5.2	ns	1, 7, 8
$t_{SK(O)}$	Output Skew ^[13]		0.5		0.5		0.5	ns	—

Notes:

- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)

- f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamps and all frequencies are in megahertz.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- See "Parameter Measurement Information" in the General Information Section.
- Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.



CY74FCT16244T/2244T CY74FCT16444T/2H244T

16-Bit Buffers/Line Drivers

Features

- Low power, pin-compatible replacement for ABT functions
- FCT-C speed at 4.1 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000 V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Extended commercial range of -40 °C to +85 °C
- $V_{CC} = 5V \pm 10\%$

CY74FCT16244T Features:

- 64 mA sink current, 32 mA source current
- Typical V_{OLP} (ground bounce) < 1.0V at $V_{CC} = 5V, T_A = 25^\circ C$

CY74FCT162244T Features:

- Balanced output drivers: 24 mA

- Reduced system switching noise
- Typical V_{OLP} (ground bounce) < 0.6V at $V_{CC} = 5V, T_A = 25^\circ C$

CY74FCT16444T Features:

- 64 mA sink current, 32 mA source current
- Reduced system loading
- Bus hold on data inputs
- Eliminates the need for external pull-up or pull-down resistors

Functional Description

These 16-bit buffers/line drivers are designed for use in memory driver, clock driver, or other bus interface applications, where high-speed and low power are required. With flow-through pinout and small shrink packaging board layout is simplified. The three-state controls are designed to allow 4-bit, 8-bit or combined 16-bit operation. The outputs are de-

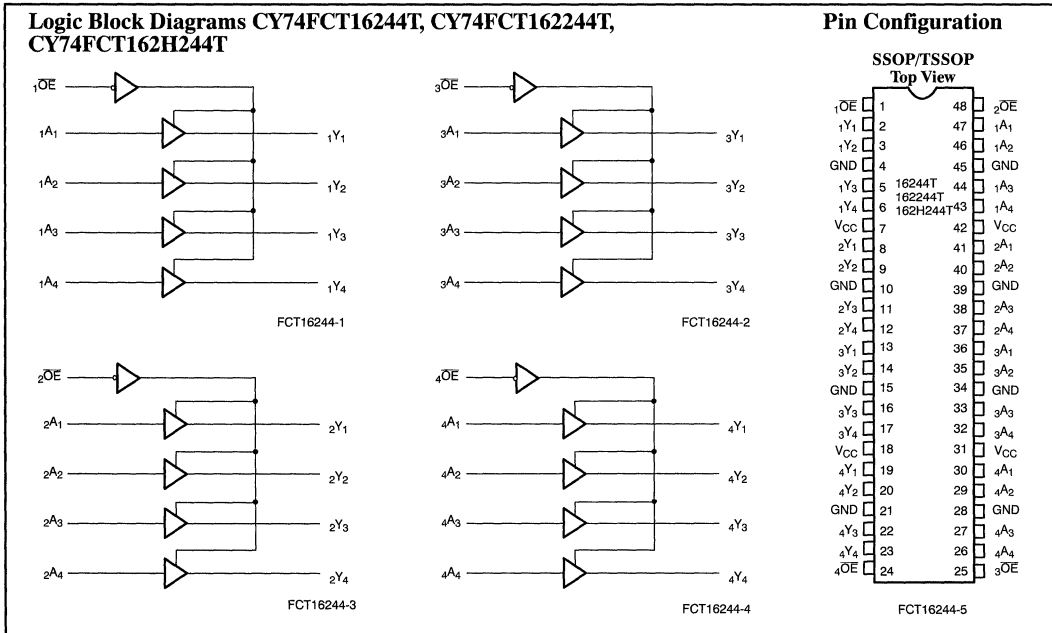
signed with a power-off disable feature to allow for live insertion of boards.

The CY74FCT16244T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162244T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162244T is ideal for driving transmission lines.

The CY74FCT16444 is designed for 16-bit operation, reducing control lines from four \overline{OE} to one \overline{OE} reduce input loading.

The CY74FCT162H244T is a 24-mA balanced output part that has "bus hold" on the data inputs. The device retains the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.



Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[6]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	Standard	V _{CC} =Max., V _I =V _{CC}		±1	μA
		Bus Hold			±100	
I _{IL}	Input LOW Current	Standard	V _{CC} =Max., V _I =GND		±1	μA
		Bus Hold			±100	μA
I _{BHH} I _{BBL}	Bus Hold Sustain Current on Bus Hold Input ^[7]	V _{CC} =Min.	V _I =2.0V	-50		μA
			V _I =0.8V	+50		
I _{BHHO} I _{BHLO}	Bus Hold Overdrive Current on Bus Hold Input ^[7]	V _{CC} =Max., V _I =1.5V			TBD	mA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	μA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	μA
I _{OS}	Short Circuit Current ^[8]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA
I _O	Output Drive Current ^[6]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V			±1	μA

Output Drive Characteristics for CY74FCT16244T, CY74FCT16444T

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} =-15 mA	2.4	3.5		V
		V _{CC} =Min., I _{OH} =-32 mA	2.0	3.0		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162244T, CY74FCT162H244T

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
I _{ODL}	Output LOW Current ^[6]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	60	115	150	mA
I _{ODH}	Output HIGH Current ^[6]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-24 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =24 mA		0.3	0.55	V

Note:

- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Pins with bus hold are described in Pin Description.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test

apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.



Ordering Information CY74FCT16244

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT16244CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16244CTPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT16244ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16244ATPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT16244TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16244TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162244

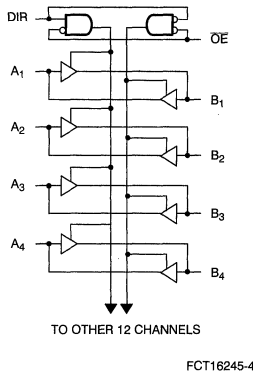
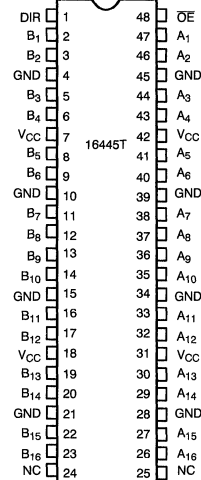
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT162244CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162244CTPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT162244ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162244ATPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT162244TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162244TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT16444

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT16444CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16444CTPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT16444ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16444ATPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT16444TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16444TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162H244

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT162H244CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H244CTPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT162H244ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H244ATPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT162H244TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H244TPVC	O48	48-Lead (300-Mil) SSOP	

Logic Block Diagram CY74FCT16445T

Pin Configuration
SSOP/TSSOP
Top View

Pin Description

Name	Description
OE	Three-State Output Enable Inputs (Active LOW)
DIR	Direction Control
A	Inputs or Three-State Outputs ^[1]
B	Inputs or Three-State Outputs ^[1]

Function Table^[2]

Inputs		Outputs
OE	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

Maximum Ratings^[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature Com'l -55°C to +125°C

Ambient Temperature with

Power Applied Com'l -55°C to +125°C

DC Input Voltage -0.5V to +7.0V

DC Output Voltage -0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin) -60 to +120 mA

Notes:

- On CY74FCT162H245T these pins have bus hold.
- H = HIGH Voltage Level, L = LOW Voltage Level.
X = Don't Care, Z = High Impedance.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

Power Dissipation 1.0W
 Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	-40°C to +85°C	5V ± 10%

- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Capacitance^[6] ($T_A = +25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4.5	6.0	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ. ^[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$	5	500	μA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC} = \text{Max.}$	$V_{IN} = 3.4V$ ^[9]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ^[10]	$V_{CC} = \text{Max.}$, One Input Toggling, 50% Duty Cycle, Outputs Open, $OE = \text{DIR} = \text{GND}$	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	60	100	$\mu\text{A}/\text{MHz}$
I_C	Total Power Supply Current ^[11]	$V_{CC} = \text{Max.}$, $f_1 = 10\text{ MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling, $OE = \text{DIR} = \text{GND}$	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	0.6	1.5	mA
			$V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	0.9	2.3	mA
		$V_{CC} = \text{Max.}$, $f_1 = 2.5\text{ MHz}$, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $OE = \text{DIR} = \text{GND}$	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	2.4	4.5 ^[12]	mA
			$V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	6.4	16.5 ^[12]	mA

Notes:

9. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.

10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

11. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamps and all frequencies are in megahertz.
 12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.



Ordering Information CY74FCT16245

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT16245CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16245CTPVC	O48	48-Lead (300-Mil) SSOP	
4.5	CY74FCT16245ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16245ATPVC	O48	48-Lead (300-Mil) SSOP	
7.0	CY74FCT16245TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16245TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162245

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT162245CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162245CTPVC	O48	48-Lead (300-Mil) SSOP	
4.5	CY74FCT162245ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162245ATPVC	O48	48-Lead (300-Mil) SSOP	
7.0	CY74FCT162245TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162245TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT16445

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT16445CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16445CTPVC	O48	48-Lead (300-Mil) SSOP	
4.5	CY74FCT16445ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16445ATPVC	O48	48-Lead (300-Mil) SSOP	
7.0	CY74FCT16445TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16445TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162H245

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT162H245CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H245CTPVC	O48	48-Lead (300-Mil) SSOP	
4.5	CY74FCT162H245ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H245ATPVC	O48	48-Lead (300-Mil) SSOP	
7.0	CY74FCT162H245TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H245TPVC	O48	48-Lead (300-Mil) SSOP	

Document #: 38-00389



Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature Com'l -55°C to +125°C
 Ambient Temperature with Power Applied Com'l -55°C to +125°C
 DC Input Voltage -0.5V to +7.0V
 DC Output Voltage -0.5V to +7.0V
 DC Output Current (Maximum Sink Current/Pin) -60 to +120 mA

Power Dissipation 1.0W
 Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	-40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[5]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =V _{CC}			±1	µA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND			±1	µA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	µA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	µA
I _{OS}	Short Circuit Current ^[6]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA
I _O	Output Drive Current ^[6]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V			±1	µA

Output Drive Characteristics for CY74FCT16373T

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} =-15 mA	2.4	3.5		V
		V _{CC} =Min., I _{OH} =-32 mA	2.0	3.0		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162373T

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
I _{ODL}	Output LOW Current ^[6]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	60	115	150	mA
I _{ODH}	Output HIGH Current ^[6]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-24 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =24 mA		0.3	0.55	V

Notes:

- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.



Switching Characteristics Over the Operating Range

Parameter	Description	CY74FCT16373T CY74FCT162373T		CY74FCT16373AT CY74FCT162373AT		CY74FCT16373CT CY74FCT162373CT		Unit	Fig. No. ^[12]
		Min. ^[11]	Max.	Min. ^[11]	Max.	Min. ^[11]	Max.		
t _{PLH} t _{PHL}	Propagation Delay D to O	1.5	8.0	1.5	5.2	1.5	4.2	ns	1, 3
t _{PLH} t _{PHL}	Propagation Delay LE to O	2.0	13.0	2.0	6.7	2.0	5.5	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time	1.5	12.0	1.5	6.1	1.5	5.5	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	7.5	1.5	5.5	1.5	5.0	ns	1, 7, 8
t _{SU}	Set-Up Time HIGH or LOW, D to LE	2.0		2.0		2.0		ns	9
t _H	Hold Time HIGH or LOW, D to LE	1.5		1.5		1.5		ns	9
t _w	LE Pulse Width HIGH	6.0		3.3		3.3		ns	5
t _{SK(O)}	Output Skew ^[13]		0.5		0.5		0.5	ns	—

Ordering Information CY74FCT16373

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT16373CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16373CTPVC	O48	48-Lead (300-Mil) SSOP	
5.2	CY74FCT16373ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16373ATPVC	O48	48-Lead (300-Mil) SSOP	
8.0	CY74FCT16373TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16373TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162373





Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT162373CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162373CTPVC	O48	48-Lead (300-Mil) SSOP	
5.2	CY74FCT162373ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162373ATPVC	O48	48-Lead (300-Mil) SSOP	
8.0	CY74FCT162373TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162373TPVC	O48	48-Lead (300-Mil) SSOP	

Notes:

11. Minimum limits are guaranteed but not tested on Propagation Delays.
 12. See "Parameter Measurement Information" in the General Information Section.
 13. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Document #: 38-00386

Function Table^[1]

Inputs			Outputs	Function
D	CLK	OE	O	
X	L	H	Z	High-Z
X	H	H	Z	
L		L	L	Load Register
H		L	H	
L		H	Z	
H		H	Z	

Pin Description

Name	Description
D	Data Inputs
CLK	Clock Inputs
OE	Three-State Output Enable Inputs (Active LOW)
O	Three-State Outputs

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	Com'1	-55°C to +125°C
Ambient Temperature with Power Applied	Com'1	-55°C to +125°C
DC Input Voltage		-0.5V to +7.0V
DC Output Voltage		-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)		-60 to +120 mA

Power Dissipation	1.0W
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	-40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[5]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =V _{CC}			±1	µA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND			±1	µA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	µA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	µA
I _{OS}	Short Circuit Current ^[6]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA
I _O	Output Drive Current ^[6]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V			±1	µA

Notes:

- H = HIGH Voltage Level. L = LOW Voltage Level.
X = Don't Care. Z = HIGH Impedance.
┐ = LOW-to-HIGH Transition.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.

- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range

Parameter	Description	CY74FCT16374T CY74FCT162374T		CY74FCT16374AT CY74FCT162374AT		CY74FCT16374CT CY74FCT162374CT		Unit	Fig. No. ^[12]
		Min. ^[11]	Max.	Min. ^[11]	Max.	Min. ^[11]	Max.		
t _{PLH} t _{PHL}	Propagation Delay CLK to O	2.0	10.0	2.0	6.5	2.0	5.2	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time	1.5	12.5	1.5	6.5	1.5	5.5	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	8.0	1.5	5.5	1.5	5.0	ns	1, 7, 8
t _{SU}	Set-Up Time HIGH or LOW, D to CLK	2.0		2.0		2.0		ns	4
t _H	Hold Time HIGH or LOW, D to CLK	1.5		1.5		1.5		ns	4
t _w	CLK Pulse Width HIGH or LOW	5.0		5.0		3.3		ns	5
t _{SK(O)}	Output Skew ^[13]		0.5		0.5		0.5	ns	

Ordering Information CY74FCT16374

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.2	CY74FCT16374CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16374CTPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT16374ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16374ATPVC	O48	48-Lead (300-Mil) SSOP	
10.0	CY74FCT16374TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16374TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162374

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.2	CY74FCT162374CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162374CTPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT162374ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162374ATPVC	O48	48-Lead (300-Mil) SSOP	
10.0	CY74FCT162374TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162374TPVC	O48	48-Lead (300-Mil) SSOP	

Notes:

- Minimum limits are guaranteed but not tested on Propagation Delays.
- See "Parameter Measurement Information" in the General Information Section.
- Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Document #: 38-00391

Pin Summary

Name	Description
OEAB	A-to-B Output Enable Input
OEBA	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input (Active LOW)
CLKBA	B-to-A Clock Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs
B	B-to-A Data Inputs or A-to-B Three-State Outputs

Function Table^[1, 2]

Inputs				Outputs
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	⌋	L	L
H	L	⌋	H	H
H	L	H	X	B ^[3]
H	L	L	X	B ^[4]

Maximum Ratings^[5, 6]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	Com'1 -55°C to +125°C
Ambient Temperature with Power Applied	Com'1 -55°C to +125°C
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	-60 to +120 mA

Power Dissipation	1.0W
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	-40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[7]	Max.	Unit
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[8]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =V _{CC}			±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND.			±1	μA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	μA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	μA
I _{OS}	Short Circuit Current ^[9]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA
I _O	Output Drive Current ^[9]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V			±1	μA

Notes:

- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = HIGH Impedance. ⌋ = HIGH-to-LOW Transition.
- A-to-B data flow is shown, B-to-A data flow is similar but uses OEBA, LEBA, and CLKBA.
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was LOW before LEAB went LOW.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.



Switching Characteristics Over the Operating Range

Parameter	Description	CY74FCT16500AT/ CY74FCT162500AT		CY74FCT16500CT/ CY74FCT162500CT		Unit	Fig. No. ^[5]
		Min. ^[14]	Max.	Min. ^[14]	Max.		
f _{MAX}	CLKAB or CLKBA frequency		150	150	150	MHz	
t _{PLH} t _{PHL}	Propagation Delay A to B or B to A	1.5	5.1	1.5	4.6	ns	1, 3
t _{PLH} t _{PHL}	Propagation Delay LEBA to A, LEAB to B	1.5	5.6	1.5	5.3	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay CLKBA to A, CLKAB to B	1.5	5.6	1.5	5.3	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time OEBA to A, OEAB to B	1.5	6.0	1.5	5.4	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time OEBA to A, OEAB to B	1.5	5.6	1.5	5.2	ns	1, 7, 8
t _{SU}	Set-Up Time, HIGH or LOW A to CLKAB, B to CLKBA	3.0		3.0		ns	9
t _H	Hold Time, HIGH or LOW A to CLKAB, B to CLKBA	0		0		ns	9
t _{SU}	Set-Up Time, HIGH or LOW A to LEAB, B to LEBA	Clock HIGH	3.0		3.0	ns	4
		Clock LOW	1.5		1.5	ns	4
t _H	Hold Time, HIGH or LOW A to LEAB, B to LEBA	1.5		1.5		ns	4
t _W	LEAB or LEBA Pulse Width HIGH	3.0		2.5		ns	5
t _W	CLKAB or CLKBA Pulse Width HIGH or LOW	3.0		3.0		ns	5
t _{SK(O)}	Output Skew ^[16]		0.5		0.5	ns	

Ordering Information CY74FCT16500T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT16500CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16500CTPVC	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT16500ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16500ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162500T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT162500CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162500CTPVC	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT162500ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162500ATPVC	O56	56-Lead (300-Mil) SSOP	

Notes:

14. Minimum limits are guaranteed but not tested on Propagation Delays.
 15. See "Parameter Measurement Information" in the General Information Section.
 16. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Document #: 38-00381



Pin Description

Name	Description
OEAB	A-to-B Output Enable Input
\overline{OEBA}	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A	A-to-B Data Inputs or B-to-A Three-State Outputs ^[1]
B	B-to-A Data Inputs or A-to-B Three-State Outputs ^[1]

Function Table^[2,3]

Inputs				Outputs
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	\lrcorner	L	L
H	L	\lrcorner	H	H
H	L	L	X	B ^[4]
H	L	H	X	B ^[5]

Maximum Ratings^[6,7]

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-55°C to +125°C
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	-60 to +120 mA
Power Dissipation	1.0W

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	-40°C to +85°C	5V ± 10%

Notes:

- On the 74FCT162H501T these pins have bus hold.
- A-to-B data flow is shown. B-to-A data flow is similar but uses \overline{OEBA} , LEBA, and CLKBA.
- H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 Z = High-impedance
 \lrcorner = LOW-to-HIGH Transition
- Output level before the indicated steady-state input conditions were established.

- Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Power Supply Characteristics

Sym.	Parameter	Test Conditions ^[12]		Min.	Typ. ^[8]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max.	V _{IN} ≤0.2V V _{IN} ≥V _{CC} -0.2V	—	5	500	μA
ΔI _{CC}	Quiescent Power Supply Current TTL inputs HIGH	V _{CC} = Max., V _{IN} = 3.4V ^[13]		—	0.5	1.5	mA
I _{CCD}	Dynamic Power Supply Current ^[14]	V _{CC} =Max., Outputs Open OEAB=OEBA=V _{CC} or GND One Input Toggling, 50% Duty Cycle	V _{IN} =V _{CC} or V _{IN} =GND	—	75	120	μA/ MHz
I _C	Total Power Supply Current ^[15]	V _{CC} =Max., Outputs Open f ₀ = 10MHz (CLKAB) 50% Duty Cycle OEAB=OEBA=V _{CC} LEAB = GND, One Bit Toggling f ₁ = 5MHz, 50% Duty Cycle	V _{IN} =V _{CC} or V _{IN} =GND	—	0.8	1.7	mA
			V _{IN} =3.4V or V _{IN} =GND	—	1.3	3.2	
		V _{CC} =Max., Outputs Open f ₀ = 10MHz (CLKAB) 50% Duty Cycle OEAB=OEBA=V _{CC} LEAB=GND Eighteen Bits Toggling f ₁ =2.5MHz, 50% Duty Cycle	V _{IN} =V _{CC} or V _{IN} =GND	—	3.8	6.5 ^[16]	
			V _{IN} =3.4V or V _{IN} =GND	—	8.5	20.8 ^[16]	

Notes:

12. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
13. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
14. This parameter is not directly testable, but is derived for use in Total Power Supply.
15. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 I_C = I_{CC} + ΔI_{CC}D_HN_T + I_{CCD}(f₀/2 + f₁N₁)
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)

- D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f₀ = Clock frequency for registered devices, otherwise zero
 f₁ = Input signal frequency
 N₁ = Number of inputs changing at f₁
 All currents are in milliamps and all frequencies are in megahertz.
16. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.



Ordering Information CY74FCT16501T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT16501CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16501CTPVC	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT16501ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16501ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162501T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT162501CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162501CTPVC	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT162501ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162501ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162H501T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT162H501CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H501CTPVC	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT162H501ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H501ATPVC	O56	56-Lead (300-Mil) SSOP	

Document #: 38-00382

Pin Description

Name	Description
\overline{OEAB}	A-to-B Output Enable Input (Active LOW)
\overline{OEBA}	B-to-A Output Enable Input (Active LOW)
\overline{CEAB}	A-to-B Enable Input (Active LOW)
\overline{CEBA}	B-to-A Enable Input (Active LOW)
\overline{LEAB}	A-to-B Latch Enable Input (Active LOW)
\overline{LEBA}	B-to-A Latch Enable Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs
B	B-to-A Data Inputs or A-to-B Three-State Outputs

Function Table^[1]

Inputs			Latch Status	Output Buffers
\overline{CEAB}	\overline{LEAB}	\overline{OEAB}	A to B	B
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs ^[2]

Maximum Ratings^[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	Com'1	-55°C to +125°C
DC Output Voltage		-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)		-60 to +120 mA
Power Dissipation		1.0W

Notes:

- A-to-B data flow shown; B-to-A flow control is the same, except using \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} .
- Data prior to \overline{LEAB} LOW-to-HIGH Transition.
H = HIGH Voltage Level, L = LOW Voltage Level.
X = Don't Care, Z = High Impedance.

Ambient Temperature with

Power Applied Com'1 -55°C to +125°C

DC Input Voltage -0.5V to +7.0V

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ. ^[8]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$	$V_{IN} \leq 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$	5	500	μA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC} = \text{Max.}$	$V_{IN} = 3.4V^{[9]}$	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ^[10]	$V_{CC} = \text{Max.},$ One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE} = GND$	$V_{IN} = V_{CC}$ or $V_{IN} = GND$	60	100	$\mu A /$ MHz
I_C	Total Power Supply Current ^[11]	$V_{CC} = \text{Max.},$ $f_1 = 10$ MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE} = GND$	$V_{IN} = V_{CC}$ or $V_{IN} = GND$	0.6	1.5	mA
			$V_{IN} = 3.4V$ or $V_{IN} = GND$	0.9	2.3	mA
		$V_{CC} = \text{Max.},$ $f_1 = 2.5$ MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE} = GND$	$V_{IN} = V_{CC}$ or $V_{IN} = GND$	2.4	4.5 ^[12]	mA
			$V_{IN} = 3.4V$ or $V_{IN} = GND$	6.4	16.5 ^[12]	mA

Notes:

- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH

- N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamps and all frequencies are in megahertz.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.



Ordering Information CY74FCT16543

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.1	CY74FCT16543CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16543CTPVC	O56	56-Lead (300-Mil) SSOP	
6.5	CY74FCT16543ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16543ATPVC	O56	56-Lead (300-Mil) SSOP	
8.5	CY74FCT16543TPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16543TPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162543

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.1	CY74FCT162543CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162543CTPVC	O56	56-Lead (300-Mil) SSOP	
6.5	CY74FCT162543ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162543ATPVC	O56	56-Lead (300-Mil) SSOP	
8.5	CY74FCT162543TPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162543TPVC	O56	56-Lead (300-Mil) SSOP	

Document #: 38-00388

Pin Description

Pin Names	Description
A	Data Register A Inputs Data Register B Outputs
B	Data Register B Inputs Data Register A Outputs
CLKAB, CLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR	Direction
\overline{OE}	Output Enable (Active LOW)

Function Table^[1]

Inputs						Data I/O ^[2]		Function
\overline{OE}	DIR	CLKAB	CLKBA	SAB	SBA	A	B	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	┘	┘	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

Notes:

- H = High Voltage Level
L = LOW Voltage Level
X = Don't Care
┘ = LOW-to-HIGH Transition
- The data output functions may be enabled or disabled by various signals at the \overline{OE} or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[6]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =V _{CC}			±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND			±1	μA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	μA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	μA
I _{OS}	Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA
I _O	Output Drive Current ^[7]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V			±1	μA

Output Drive Characteristics for CY74FCT16646T

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} =-15 mA	2.4	3.5		V
		V _{CC} =Min., I _{OH} =-32 mA	2.0	3.0		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162646T

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
I _{ODL}	Output LOW Current ^[7]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	60	115	150	mA
I _{ODH}	Output HIGH Current ^[7]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-24 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =24 mA		0.3	0.55	V

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Description ^[8]	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

Notes:

- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametrics tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- This parameter is measured at characterization but not tested.



Switching Characteristics Over the Operating Range

Parameter	Description	Cond.	74FCT16646T 74FCT162646T		74FCT16646AT 74FCT162646AT		74FCT16646CT 74FCT162646CT		Unit	Fig. No. ^[14]
			Min. ^[15]	Max.	Min. ^[15]	Max.	Min. ^[15]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	C _L = 50 pF R _L = 500Ω	1.5	9.0	1.5	6.3	1.5	5.4	ns	1, 2
t _{PZH} t _{PZL}	Output Enable Time DIR or OE to Bus		1.5	14.0	1.5	9.8	1.5	7.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time DIR or OE to Bus		1.5	9.0	1.5	6.3	1.5	6.3	ns	1, 7, 8
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus		1.5	9.0	1.5	6.3	1.5	5.7	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay SBA or SAB to Bus		1.5	11.0	1.5	7.7	1.5	6.2	ns	1, 5
t _{SU}	Set-Up Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	2.0	—	ns	4
t _H	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	1.5	—	ns	4
t _w	Clock Pulse Width HIGH or LOW		5.0	—	5.0	—	5.0	—	ns	6
t _{SK(O)}	Output Skew ^[16]		—	0.5	—	0.5	—	0.5	ns	—

Ordering Information CY74FCT16646

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT16646CTPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16646CTPVC	O56	48-Lead (300-Mil) SSOP	
6.3	CY74FCT16646ATPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16646ATPVC	O56	48-Lead (300-Mil) SSOP	
9.0	CY74FCT16646TPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16646TPVC	O56	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162646

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT162646CTPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162646CTPVC	O56	48-Lead (300-Mil) SSOP	
6.3	CY74FCT162646ATPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162646ATPVC	O56	48-Lead (300-Mil) SSOP	
9.0	CY74FCT162646TPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162646TPVC	O56	48-Lead (300-Mil) SSOP	

Notes:

14. See "Parameter Measurement Information" in the General Information Section.
15. Minimum limits are guaranteed but not tested on Propagation Delays.

16. Skew any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Pin Description

Name	Description
A	Data Register A Inputs Data Register B Outputs
B	Data Register B Inputs Data Register A Outputs
CLKAB, CLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
OEAB, OEBA	Output Enable Inputs

Function Table^[1]

Inputs						Data I/O ^[2]		Operation or Function
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A	B	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	┘	┘	X	X			Store A and B Data
X	H	┘	H or L	X	X	Input	Unspecified ^[2]	Store A, Hold B
H	H	┘	┘	X ^[3]	X	Input	Output	Store A in Both Registers
L	X	H or L	┘	X	X	Unspecified ^[2]	Input	Hold A, Store B
L	L	┘	┘	X	X ^[3]		Input	Store B in both Registers
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

Notes:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
┘ = LOW-to-HIGH Transition
- The data output functions may be enabled or disabled by various signals at the OEAB or OEBA inputs. Data input functions are always

enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

- Select control=L; clocks can occur simultaneously.
Select control=H; clocks must be staggered to load both registers.

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions ^[5]	Min.	Typ. ^[6]	Max.	Unit
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
V _H	Input Hysteresis			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current ^[7]	V _{CC} =Max., V _I =V _{CC}			±1	µA
I _{IL}	Input LOW Current ^[7]	V _{CC} =Max., V _I =GND			±1	µA
I _{OZH}	High Impedance Output ^[7] Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	µA
I _{OZL}	High Impedance Output ^[7] Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	µA
I _{OS}	Short Circuit Current	V _{CC} =Max., V _{OUT} =GND ^[8]	-80	-140	-200	mA
I _O	Output Drive Current	V _{CC} =Max., V _{OUT} =2.5V ^[8]	-50		-180	mA
I _{OFF}	Power-Off Disable ^[7]	V _{CC} =0V, V _{OUT} ≤4.5V			±1	µA

Output Drive Characteristics for CY74FCT16652T

Parameter	Description	Test Conditions ^[5]	Min.	Typ. ^[6]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} =-15 mA	2.4	3.5		V
		V _{CC} =Min., I _{OH} =-32 mA ^[9]	2.0	3.0		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162652T

Parameter	Description	Test Conditions ^[5]	Min.	Typ. ^[6]	Max.	Unit
I _{ODL}	Output LOW Current	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V ^[8]	60	115	150	mA
I _{ODH}	Output HIGH Current	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V ^[8]	-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-24 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =24 mA		0.3	0.55	V

Capacitance (T_A = +25°C, f = 1.0 MHz)

Parameter	Description ^[10]	Test Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC}=5.0V, +25°C ambient.
- The test limit for this parameter is +5mA at T_A=-55°C.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition cannot exceed one second.
- This parameter is measured at characterization but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	Cond. ^[17]	74FCT16652T 74FCT162652T		74FCT16652AT 74FCT162652AT		74FCT16652CT 74FCT162652CT		Unit	Fig. No. ^[18]
			Min. ^[19]	Max.	Min. ^[19]	Max.	Min. ^[19]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	C _L =50 pF R _L =500Ω	1.5	9.0	1.5	6.3	1.5	5.4	ns	1, 3
t _{PZH} t _{PHL}	Output Enable Time OEAB or OEBA to Bus		1.5	14.0	1.5	9.8	1.5	7.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time OEAB or OEBA to Bus		1.5	9.0	1.5	6.3	1.5	6.3	ns	1, 7, 8
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus		1.5	9.0	1.5	6.3	1.5	5.7	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay SBA or SAB to Bus		1.5	11.0	1.5	7.7	1.5	6.2	ns	1, 5
t _{SU}	Set-Up time HIGH or LOW Bus to Clock		2.0	—	2.0	—	2.0	—	ns	4
t _H	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	1.5	—	ns	4
t _w	Clock Pulse Width HIGH or LOW		5.0	—	5.0	—	5.0	—	ns	5
t _{SK(O)}	Output Skew ^[20]		—	0.5	—	0.5	—	0.5	ns	

Notes:

17. See test circuits and waveforms.

18. See "Parameter Measurement Information" in the General Information Section.

19. Minimum limits are guaranteed, but not tested, on propagation delays.

20. Skew between any two outputs of the same package switching in the same direction. This parameter guaranteed by design.



CY74FCT16823T CY74FCT162823T

18-Bit Registers

Features

- Low power, pin compatible replacement for ABT functions
- FCT-C speed at 6.0 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000 V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 5V \pm 10\%$

CY74FCT16823T Features:

- 64 mA sink current (Com'l), 32 mA source current (Com'l)
- Typical V_{OLP} (ground bounce) < 1.0V at $V_{CC} = 5V, T_A = 25^\circ C$

CY74FCT162823T Features:

- Balanced output drivers: 24 mA
- Reduced system switching noise
- Typical V_{OLP} (ground bounce) < 0.6V at $V_{CC} = 5V, T_A = 25^\circ C$

Functional Description

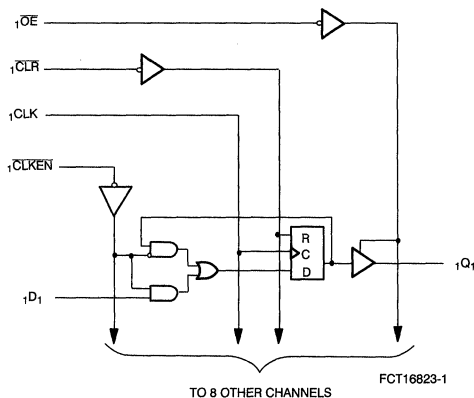
The CY74FCT16823T and the CY74FCT162823T 18-bit bus interface register are designed for use in high-speed, low-power systems needing wide

registers and parity. 18-bit operation is achieved by connecting the control lines of the two 9-bit registers. Flow-through pinout and small shrink packaging aids in simplifying board layout. The outputs are designed with a power-off disable feature to allow live insertion of boards.

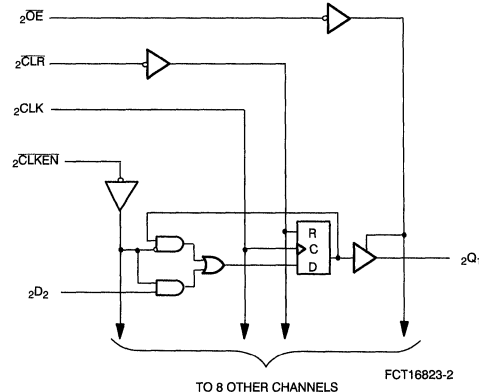
The CY74FCT16823T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162823T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162823T is ideal for driving transmission lines.

Logic Block Diagrams

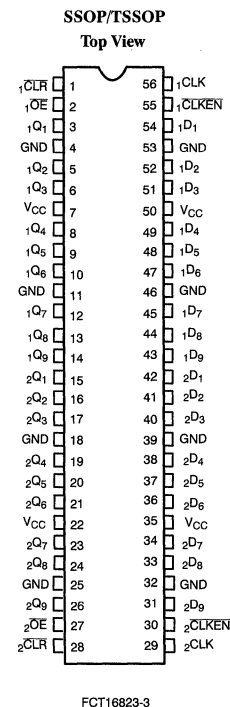


FCT16823-1



FCT16823-2

Pin Configuration



Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[8]	Max.	Unit
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[5]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =V _{CC}			±1	µA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND			±1	µA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	µA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	µA
I _{OS}	Short Circuit Current ^[6]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA
I _O	Output Drive Current ^[6]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V			1	µA

Output Drive Characteristics for CY74FCT16823T

Parameter	Description	Test Conditions	Min.	Typ. ^[8]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} =-15 mA	2.4	3.5		V
		V _{CC} =Min., I _{OH} =-32 mA	2.0	3.0		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162823T

Parameter	Description	Test Conditions	Min.	Typ. ^[8]	Max.	Unit
I _{ODL}	Output LOW Voltage ^[6]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	60	115	150	mA
I _{ODH}	Output HIGH Voltage ^[6]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-24 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =24 mA		0.3	0.55	V

Capacitance^[7] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ. ^[8]	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

Notes:

- This input is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- This parameter is guaranteed but not tested.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.

Switching Characteristics Over the Operating Range

Parameter	Description	Condition ^[14]	74FCT16823AT 74FCT162823AT		74FCT16823BT 74FCT162823BT		74FCT16823CT 74FCT162823CT		Unit	Fig. No. ^[16]
			Min. ^[15]	Max.	Min. ^[15]	Max.	Min. ^[15]	Max.		
t _{PLH} t _{PHL}	Propagation Delay CLK to Q	C _L =50 pF R _L =500Ω	1.5	10.0	1.5	7.5	1.5	6.0	ns	1, 5
		C _L =300 pF ^[17] R _L =500Ω	1.5	20.0	1.5	15.0	1.5	12.5		
t _{PHL}	Propagation Delay CLR to Q	C _L =50 pF R _L =500Ω	1.5	14.0	1.5	9.0	1.5	6.1	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time OE to Q	C _L =50 pF R _L =500Ω	1.5	12.0	1.5	8.0	1.5	5.5	ns	1, 7, 8
		C _L =300 pF ^[17] R _L =500Ω	1.5	23.0	1.5	15.0	1.5	12.5		
t _{PHZ} t _{PLZ}	Output Disable Time OE to Q	C _L =5 pF ^[17] R _L =500Ω	1.5	7.0	1.5	6.5	1.5	5.2	ns	1, 7, 8
		C _L =50 pF R _L =500Ω	1.5	8.0	1.5	7.5	1.5	6.5		
t _{SU}	Set-Up Time HIGH or LOW D to CLK	C _L =50 pF R _L =500Ω	3.0	—	3.0	—	2.0	—	ns	4
t _H	Hold Time HIGH or LOW D to CLK		1.5	—	1.5	—	1.5	—	ns	4
t _{SU}	Set-Up Time HIGH or LOW CLKEN to CLK		3.0	—	3.0	—	3.0	—	ns	9
t _H	Hold Time HIGH or LOW CLKEN to CLK		0	—	0	—	0	—	ns	9
t _W	CLK Pulse Width HIGH or LOW		6.0	—	6.0	—	3.3	—	ns	5
t _W	CLR Pulse Width LOW		6.0	—	6.0	—	3.3	—	ns	5
t _{REM}	Recovery Time CLR to CLK		6.0	—	6.0	—	6.0	—	ns	6
t _{SK(O)}	Output Skew ^[18]		—	0.5	—	0.5	—	0.5	ns	—

Notes:

14. See test circuit and waveforms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. See "Parameter Measurement Information" in the General Information Section.
17. These limits are guaranteed but not tested.
18. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.



CY74FCT16827T CY74FCT162827T

20-Bit Buffers

Features

- Low power, pin compatible replacement for ABT functions
- FCT-C speed at 4.2 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000 V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Extended commercial range of -40 °C to +85 °C
- $V_{CC} = 5V \pm 10\%$

CY74FCT16827T Features:

- 64 mA sink current (Com'1), 32 mA source current (Com'1)
- Typical V_{OLP} (ground bounce) < 1.0V at $V_{CC} = 5V, T_A = 25^\circ C$

CY74FCT162827T Features:

- Balanced output drivers: 24 mA
- Reduced system switching noise
- Typical V_{OLP} (ground bounce) < 0.6V at $V_{CC} = 5V, T_A = 25^\circ C$

Functional Description

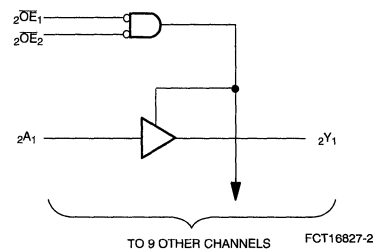
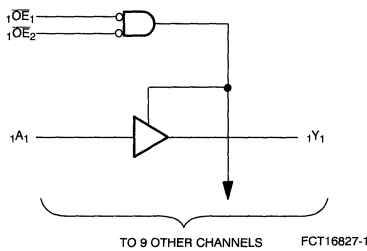
The CY74FCT16827T 20-bit buffer/line driver and the CY74FCT162827T 20-bit buffer/line driver provide high-performance bus interface buffering for wide data/address paths or buses carrying par-

ity. These parts can be used as a single 20-bit buffer or two 10-bit buffers. Each 10-bit buffer has a pair of NANDed OE for increased flexibility. The outputs are designed with a power-off disable feature to allow for live insertion of boards.

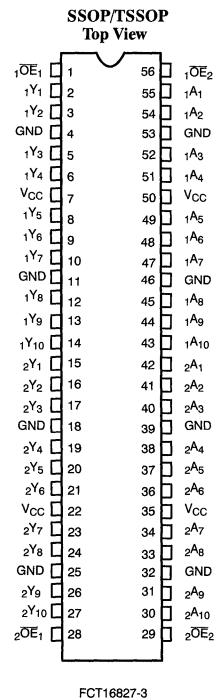
The CY74FCT16827T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162827T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162827T is ideal for driving transmission lines.

Logic Block Diagrams



Pin Configuration



Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[5]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =V _{CC}			±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND			±1	μA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	μA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	μA
I _{OS}	Short Circuit Current ^[6]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA
I _O	Output Drive Current ^[6]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V			±1	μA

Output Drive Characteristics for CY74FCT16827T

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} =-15 mA	2.4	3.5		V
		V _{CC} =Min., I _{OH} =-32 mA	2.0	3.0		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT16827T

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
I _{ODL}	Output LOW Current ^[6]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	60	115	150	mA
I _{ODH}	Output HIGH Current ^[6]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-24 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =24 mA		0.3	0.55	V

Capacitance^[5] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ. ^[4]	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

Notes:

- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order

to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range

Parameter	Description	Condition ^[11]	74FCT16827AT 74FCT162827AT		74FCT16827BT 74FCT162827BT		74FCT16827CT 74FCT162827CT		Unit	Fig. No. ^[13]
			Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay A to Y	C _L =50 pF R _L =500Ω	1.5	8.0	1.5	5.0	1.5	4.2	ns	1, 3
		C _L =300 pF ^[3] R _L =500Ω	1.5	15.0	1.5	13.0	1.5	10.0		
t _{PZH} t _{PZL}	Output Enable Time OE to Y	C _L =50 pF R _L =500Ω	1.5	12.0	1.5	8.0	1.5	5.6	ns	1, 7, 8
		C _L =300 pF ^[3] R _L =500Ω	1.5	23.0	1.5	15.0	1.5	14.0		
t _{PHZ} t _{PLZ}	Output Disable Time OE to Y	C _L =5 pF ^[3] R _L =500Ω	1.5	9.0	1.5	6.0	1.5	5.7	ns	1, 7, 8
		C _L =50 pF R _L =500Ω	1.5	10.0	1.5	7.0	1.5	6.0		
t _{SK(O)}	Output Skew ^[14]		—	0.5	—	0.5	—	0.5	ns	—

Ordering Information CY74FCT16827

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT16827CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16827CTPVC	O56	56-Lead (300-Mil) SSOP	
5.0	CY74FCT16827BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16827BTPVC	O56	56-Lead (300-Mil) SSOP	
8.0	CY74FCT16827ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16827ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162827

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT162827CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162827CTPVC	O56	56-Lead (300-Mil) SSOP	
5.0	CY74FCT162827BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162827BTPVC	O56	56-Lead (300-Mil) SSOP	
8.0	CY74FCT162827ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162827ATPVC	O56	56-Lead (300-Mil) SSOP	

Notes:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- See "Parameter Measurement Information" in the General Information Section.
- Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Document #: 38-00393

Pin Description

Name	Description
D	Data Inputs
LE	Latch Enable Input (Active HIGH)
OE	Output Enable Input (Active LOW)
O	Three-State Outputs

Function Table^[1]

Inputs			Outputs
D	LE	OE	Q
H	H	L	H
L	H	L	L
X	L	L	Q ^[2]
X	X	H	Z

Maximum Ratings^[3,4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-55°C to +125°C
DC Input Voltage	-0.5V to +7.0V

DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	-60 to +120 mA
Power Dissipation	1.0W
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
V _H	Input Hysteresis ^[6]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =V _{CC}			±1	µA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND			±1	µA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	µA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	µA
I _{OS}	Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA
I _O	Output Drive Current ^[7]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V			±1	µA

Notes:

- H = HIGH Voltage Level.
L = LOW Voltage Level.
X = Don't Care.
Z = HIGH Impedance.
- Output level before LE HIGH-to-LOW Transition.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range

Parameter	Description	Condition ^[12]	74FCT16841AT 74FCT162841AT		74FCT16841BT 74FCT162841BT		74FCT16841CT 74FCT162841CT		Unit	Fig. No. ^[14]
			Min. ^[13]	Max.	Min. ^[13]	Max.	Min. ^[13]	Max.		
t _{PLH} t _{PHL}	Propagation Delay D to Q (LE=HIGH)	C _L =50 pF R _L =500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns	1, 5
		C _L =300 pF ^[15] R _L =500Ω	1.5	13.0	1.5	13.0	1.5	13.0		
t _{PLH} t _{PHL}	Propagation Delay LE to Q	C _L =50 pF R _L =500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns	1, 5
		C _L =300 pF ^[15] R _L =500Ω	1.5	16.0	1.5	15.5	1.5	15.0		
t _{PHZ} t _{PZL}	Output Enable Time OE to Q	C _L =50 pF R _L =500Ω	1.5	11.5	1.5	8.0	1.5	6.5	ns	1, 7, 8
		C _L =300 pF ^[15] R _L =500Ω	1.5	23.0	1.5	14.0	1.5	12.0		
t _{PHZ} t _{PLZ}	Output Disable Time OE to Q	C _L =5 pF ^[15] R _L =500Ω	1.5	7.0	1.5	6.0	1.5	5.7	ns	1, 7, 8
		C _L =50 pF R _L =500Ω	1.5	8.0	1.5	7.0	1.5	6.0		
t _{SU}	Set-Up Time HIGH or LOW, D to LE	C _L =50 pF R _L =500Ω	2.5	—	2.5	—	2.0	—	ns	9
t _H	Hold Time HIGH or LOW, D to LE		2.5	—	2.5	—	1.5	—	ns	9
t _W	LE Pulse Width HIGH		4.0 ^[16]	—	4.0 ^[16]	—	4.0 ^[16]	—	ns	5
t _{SK(O)}	Output Skew ^[17]		—	0.5	—	0.5	—	0.5	ns	—

Notes:

12. See test circuit and waveform.
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. See "Parameter Measurement Information" in the General Information Section.
15. These conditions are guaranteed but not tested.
16. These limits are guaranteed but not tested.
17. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.



CY74FCT16952T CY74FCT162952T CY74FCT162H952T

16-Bit Registered Transceivers

Features

- Low power, pin-compatible replacement for ABT functions
- FCT-C speed at 6.3 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000 V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 5V \pm 10\%$

CY74FCT16952T Features:

- 64 mA sink current (Com'1), 32 mA source current (Com'1)
- Typical V_{OLP} (ground bounce) < 1.0V at $V_{CC} = 5V, T_A = 25^\circ C$

CY74FCT162952T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) < 0.6V at $V_{CC} = 5V, T_A = 25^\circ C$**

CY74FCT162H952T Features:

- **Bus hold retains last active state**
- **Eliminates the need for external pull-up or pull-down resistors**

Functional Description

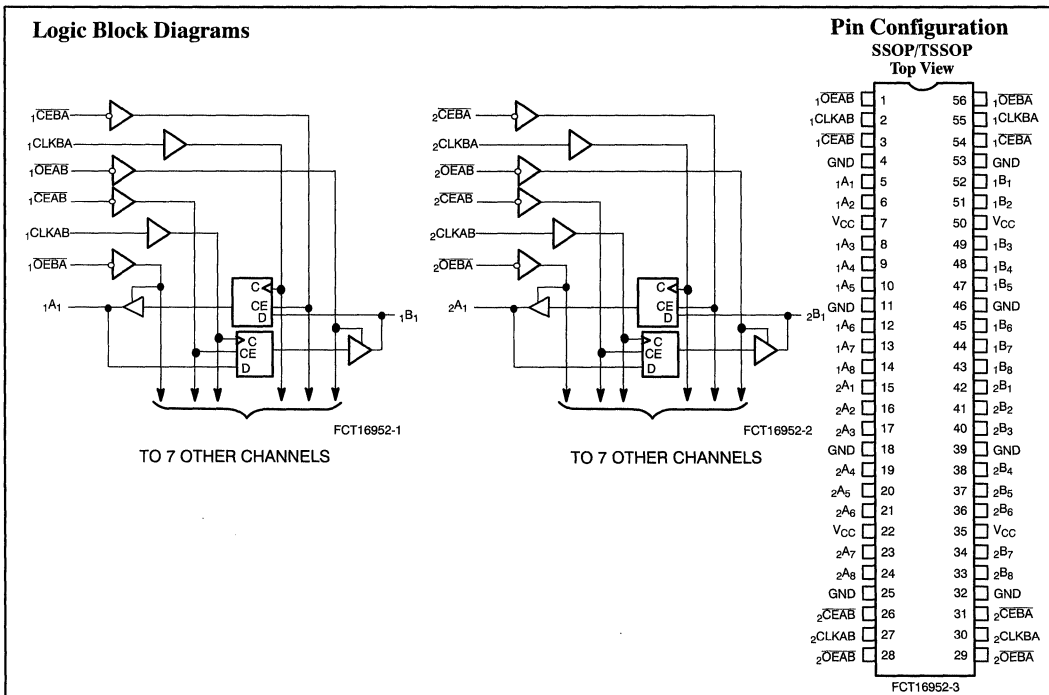
These 16-bit registered transceivers are high-speed, low-power devices. 16-bit operation is achieved by connecting the control lines of the two 8-bit registered transceivers together. For data flow from bus A-to-B, \overline{CEAB} must be LOW to allow data to be stored when CLKAB transitions from LOW-to-HIGH. The stored data will be present on the output when \overline{OEAB} is LOW. Control of data from B-to-A is similar and is controlled by

using the \overline{CEBA} , CLKBA, and \overline{OEBA} inputs. The output buffers are designed with a power-off disable feature to allow for live insertion of boards.

The CY74FCT16952T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162952T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162952T is ideal for driving transmission lines.

The CY74FCT162H952T is a 24-mA balanced output part that has "bus hold" on the data inputs. The device retains the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.



Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[10]	Max.	Unit	
V _{IH}	Input HIGH Voltage		2.0			V	
V _{IL}	Input LOW Voltage				0.8	V	
V _H	Input Hysteresis ^[7]			100		mV	
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V	
I _{IH}	Input HIGH Current	Standard	V _{CC} =Max., V _I =V _{CC}			±1	μA
		Bus Hold				±100	
I _{IL}	Input LOW Current	Standard	V _{CC} =Max., V _I =GND			±1	μA
		Bus Hold				±100	μA
I _{BBH} I _{BBL}	Bus Hold Sustain Current on Bus Hold Input ^[8]	V _{CC} =Min., V _I =2.0V	-50				μA
		V _I =0.8V	+50				
I _{BHHO} I _{BHLO}	Bus Hold Overdrive Current on Bus Hold Input ^[7]	V _{CC} =Max., V _I =1.5V			TBD	mA	
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	μA	
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	μA	
I _{OS}	Short Circuit Current ^[9]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA	
I _O	Output Drive Current ^[9]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA	
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V			±1	μA	

Output Drive Characteristics for CY74FCT16952T

Parameter	Description	Test Conditions	Min.	Typ. ^[10]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} =-15 mA	2.4	3.5		V
		V _{CC} =Min., I _{OH} =-32 mA	2.0	3.0		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162952T, CY74FCT162H952T

Parameter	Description	Test Conditions	Min.	Typ. ^[10]	Max.	Unit
I _{ODL}	Output LOW Current ^[9]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	60	115	150	mA
I _{ODH}	Output HIGH Current ^[9]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-24 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =24 mA		0.3	0.55	V

Capacitance^[7] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ. ^[10]	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

Notes:

- This parameter is guaranteed but not tested.
- Pins with bus hold are described in the Pin Description.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.

Switching Characteristics Over the Operating Range

Parameter	Description	Conditions ^[16]	74FCT16952AT 74FCT162952AT 74FCT162H952AT		74FCT16952BT 74FCT162952BT 74FCT162H952BT		74FCT16952CT 74FCT162952CT 74FCT162H952CT		Unit	Fig. No. ^[18]
			Min. ^[17]	Max.	Min. ^[17]	Max.	Min. ^[17]	Max.		
t _{PLH} t _{PHL}	Propagation Delay CLKAB, CLKBA to B, A	C _L = 50 pF R _L = 500Ω	2.0	10.0	2.0	7.5	2.0	6.3	ns	1, 5
t _{pZH} t _{pZL}	Output Enable Time OEBA, OEAB to A, B		1.5	10.5	1.5	8.0	1.5	7.0	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time OEBA, OEAB to A, B		1.5	10.0	1.5	7.5	1.5	6.5	ns	1, 7, 8
t _{SU}	Set-Up Time, HIGH or LOW A, B to CLKAB, CLKBA		2.5	—	2.5	—	2.5	—	ns	4
t _H	Hold Time, HIGH or LOW A, B to CLKAB, CLKBA		2.0	—	1.5	—	1.5	—	ns	4
t _{SU}	Set-Up Time, HIGH or LOW CEAB, CEBA to CLKAB, CLKBA		3.0	—	3.0	—	3.0	—	ns	4
t _H	Hold Time, HIGH or LOW CEAB, CEBA to CLKAB, CLKBA		2.0	—	2.0	—	2.0	—	ns	4
t _w	Pulse Width HIGH or LOW CLKAB or CLKBA ^[19]		3.0	—	3.0	—	3.0	—	ns	5
t _{SK(O)}	Output Skew ^[20]		—	0.5	—	0.5	—	0.5	ns	—

Notes:

16 See test circuits and waveforms.

17. Minimum limits are guaranteed but not tested on Propagation Delays.

18. See "Parameter Measurement Information" in the General Information Section.

19. This parameter is guaranteed but not tested.

20. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Dual 5-Bit Bus Switches

Features

- Zero propagation delay
- 2Ω switches connect inputs to outputs
- Direct bus connection when switches are ON
- High (>500 Meg Ω) resistance when switch is OFF
- Performs bidirectional translator function between 3.3V and 5.0V power supplies
- CMOS for low power dissipation
- Edge-rate control circuitry for significantly improved noise characteristics
- Inputs and outputs interface with 5.0V CMOS, TTL, or 3.3V CMOS
- ESD >2000 V
- Power-off disable

CYBUS3L384

- Low power version

Functional Description

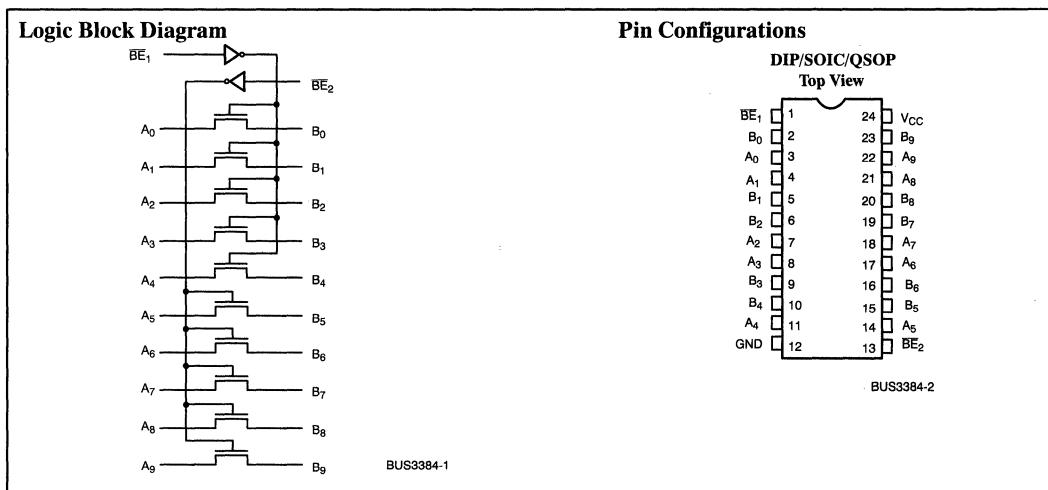
The CYBUS3384 and CYBUS3L384 are ten-bit, two-port bidirectional bus switches that allow one bus to be connected directly to, or isolated from, another without introducing additional propagation delay or ground noise. The input and output voltage levels allow direct interface with TTL and CMOS devices. Two bus enable signals, \overline{BE}_1 and \overline{BE}_2 , turn on the upper and lower five bits, respectively.

Designed with a low resistance of 2Ω , the CYBUS3384 and CYBUS3L384 are ideal for use in VME or other high DC drive applications.

The power-off disable feature enables modules and cards to be either inserted or withdrawn from operating equipment without shutting down power. Additionally, they facilitate bidirectional interfacing between 3.3V and 5V systems by placing a single diode in series with the 5V V_{CC} line and a resistor from pin 24 to ground.

The CYBUS3384 and CYBUS3L384 are also suitable for small signal analog application where crosstalk and off isolation performance of -66 dB at 50 MHz is required.

The CYBUS3L384 is a low-power version of the CYBUS3384 with a typical I_{CC} of $0.2 \mu A$.



Pin Description

Name	Description
A	Bus A, Inputs or Outputs
B	Bus B, Inputs or Outputs
$\overline{BE}_1, \overline{BE}_2$	Bus Switch Enable

Function Table^[1]

Inputs				Function
\overline{BE}_1	\overline{BE}_2	B ₀₋₄	B ₅₋₉	
H	H	High-Z	High-Z	Non-connect
L	H	A ₀₋₄	High-Z	Connect
H	L	High-Z	A ₅₋₉	Connect
L	L	A ₀₋₄	A ₅₋₉	Connect

Note:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.

Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	3	4	pF
C _{OUT}	Output Capacitance	7	8	pF

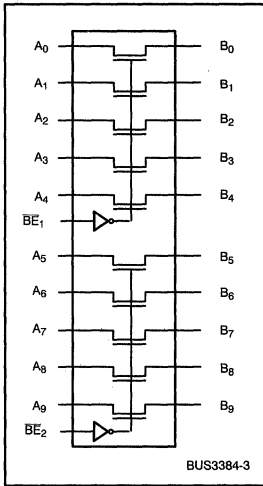
Power Supply Characteristics

Parameter	Description	Test Conditions ^[8]	Typ. ^[5]	Max.	Unit	
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤GND or V _{CC} , f=0	3384	0.1	0.2	mA
			3L384	0.2	3.0	μA
ΔI _{CC}	Quiescent Power Supply Current (Input HIGH) ^[9]	V _{CC} =Max., V _{IN} =3.4V, f=0, Per Control Input		2.0	mA	
I _{CCD}	Dynamic Power Supply Current ^[10]	V _{CC} =Max., Control Input Toggling, @ 50% Duty Cycle, A & B Pins Open		0.12	mA/MHz	
I _C	Total Power Supply Current ^[11, 12]	V _{CC} =Max., Two Control Inputs Toggling, @ 50% Duty Cycle, f ₁ =10 MHz, V _{IN} =3.4V	3384		4.6	mA
			3L384		4.4	mA

Notes:

8. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
9. Per TTL driven input (V_{IN}=3.4V); A and B pins do not contribute to I_{CC}. All other inputs at V_{CC} or GND.
10. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested but is guaranteed by design.
11. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC}D_HN_T + I_{CCD}(f₀/2 + f₁N₁)
I_{CC} = Quiescent Current with CMOS input levels

- ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
D_H = Duty Cycle for TTL inputs HIGH
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
f₀ = Clock frequency for registered devices, otherwise zero
f₁ = Input signal frequency
N₁ = Number of inputs changing at f₁
12. Note that activity on A or B inputs do not contribute to I_C. The switches merely connect and pass through activity on these pins.


Figure 1. CYBUS3384

Application Information

The CYBUS3384 is a ten-channel bidirectional solid state bus switch with a "near zero" propagation delay.

The CYBUS3384 is organized into two groups of five N-Channel MOSFETs. Each group has an independent control input for output enable (see Figure 1). Because the N-channel MOSFET is physically symmetric, the device pin can act as an input or an output.

The two enable input (\overline{BE}_1 and \overline{BE}_2) sense TTL level signals and drive the gates of the N-channel MOSFETs to V_{CC} . With the gate at V_{CC} , the output voltage will follow the input voltage up to V_{CC} minus the threshold voltage. At this point the N-channel MOSFET begins to turn off, rapidly increasing the effective resistance (R_{ON}) such that further increases to input voltage no longer increase the output voltage (see Figure 2).

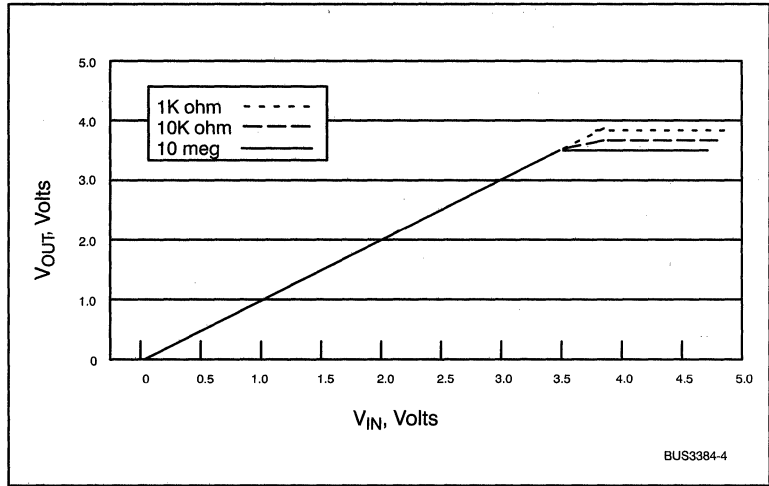
When either the input or output of the CYBUS3384 is near zero volts and the gate is at V_{CC} , the device is fully on, (low resistance) and available to pass large currents in either direction. In this condition, the CYBUS3384 inputs are directly connected to the outputs.

The CYBUS3384 provides no signal drive itself. As a result the rise and fall times of the CYBUS3384 outputs are determined by the device driving the CYBUS3384 inputs rather than the CYBUS3384 itself.

The propagation delay contributed by the CYBUS3384 is essentially zero when the N-channel gate is at V_{CC} .

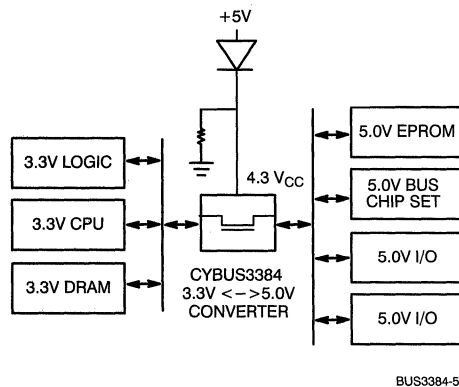
When the device is unpowered, the CYBUS3384 draws no current from the I/O or control inputs, and there is no current path from the I/O or control to the power pins. There are no back power or current drain problems when the device is unpowered.

The CYBUS3384 provides an ideal interface between 5V and 3.3V components, since the CYBUS3384 provides no signal drive, the I_{CC} demands are small, limited to AC switching of the N-channel gates, control circuitry, and a minute amount of I/O leakage. Due to the low current demands of the CYBUS3384, it


Figure 2. V_{OUT} vs. Volts

is possible to lower the CYBUS3384 V_{CC} from a standard 5.0V supply with a small, inexpensive diode and a resistor to provide a low-current full-bidirectional signal compatibility between 5V logic family signals and 3.3V logic family signals.

By adding a small, inexpensive diode and a resistor, the CYBUS3384 V_{CC} supply voltage can be shifted to 4.3V as shown in Figure 3. 5V signals will then be limited to 3.3V as they pass through the CYBUS3384. 3.3V signals will pass back through the CYBUS3384 unaltered and provide compatibility with 5V TTL input requirements. Note that the conversion is bidirectional and is limited to 3.3V independent of which side is driven to 5V. The CYBUS3384 could convert 5V signals for use on a 3.3V bus of convert a 5V bus to signals compatible with 3.3V components.


Figure 3. System with CYBUS3384 as 5V TTL to 3V Converter

the bus through the CYBUS3384s and sets the BUSY bit notifying the other bus the SRAM is not available). Processor 1 owns the bus and may now access the SRAM as needed. When finished, Processor 1 resets the OWN bit releasing the SRAM. The SRAM access sequence is identical for Processor 2. In this application, the CYBUS3384 saves 10 ns compared to using an F244 address buffer and an F245 data bus transceiver. This, in turn, allows the use of a slower, more available SRAM, resulting in lower system cost and power savings.

Selectable Termination Loads

In some applications, it is desirable to vary the characteristic termination impedance as the system configuration changes. This is a common problem in automatic test equipment applications. Because of their low ON resistance, miniature relays are often used to switch termination loads. A single CYBUS3384 can replace as many as 10 such relays resulting in faster switching operation, lower power, and significant cost savings.

Fast Latch

Figures 8 and 9 show variations of a latch having a sub 1-ns propagational delay time using the CYBUS3384 in combination with other components. This circuit has the advantage of being four

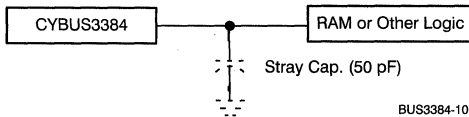


Figure 8. Latch Variation with Stray Capacitance

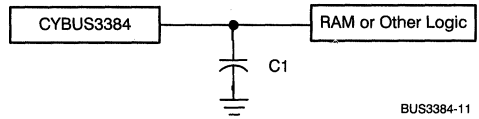


Figure 9. Latch Variation with Physical Capacitor

to ten times faster than an equivalent implementation using a 373 latch—and with no added noise. Figure 8 relies on the stray capacitance of the bus to maintain data when the CYBUS3384 opens. Assuming 50-pF stray capacitance at room temperature and a 1 microampere input leakage current, a 1 volt “droop” from the initial voltage level would take 50 microseconds. Figure 9 shows the addition of a physical capacitor if there is insufficient stray capacitance. Figure 10 shows an active bus termination capable of sustaining the programmed logic for an indefinite period of time in the presence of V_{CC} .

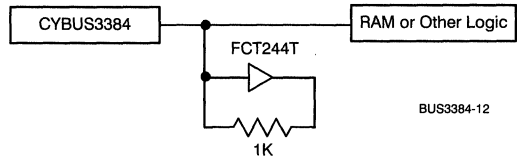


Figure 10. Active Bus Termination

Timing Technology Products	Page Number
Device	Description
CY2254	Pentium™ Processor Compatible Clock Synthesizer/Driver 10-1
CY2255	Pentium Processor Compatible Clock Synthesizer/Driver for OPTi Viper™ Chipset 10-7
CY2291	Three-PLL Clock Generator 10-13
ICD2023	PC Motherboard Clock Generator 10-19
ICD2025	Motherboard Clock Generator 10-27
ICD2027	PC Motherboard Clock Generator 10-33
ICD2028	PC Motherboard Clock Generator 10-39
ICD2042A	Dual VGA Clock Generator 10-51
ICD2051	Dual Programmable Clock Generator 10-56
ICD2053B	Programmable Clock Generator 10-64
ICD2061A	Dual Programmable Graphics Clock Generator 10-71
ICD2062B	Dual Programmable ECL/TTL Clock Generator 10-85
ICD2063	Programmable Graphics Clock Generator 10-100
ICD2093	“Super Buffer” Clock Generator 10-117
ICD6233	One-Time-Programmable Clock Oscillator 10-127
CY7B991	Programmable Skew Clock Buffer (PSCB) 10-130
CY7B992	Programmable Skew Clock Buffer (PSCB) 10-130
CY7B9910	Low Skew Clock Buffer 10-141
CY7B9920	Low Skew Clock Buffer 10-141

Pin Summary

Name	Number	Description
V _{DD}	1	Digital voltage supply
XTALIN ^[1]	2	Reference crystal input
XTALOUT ^[1]	3	Reference crystal feedback
V _{SS}	4	Ground
OE	5	Output Enable, Active HIGH
PCLK0	6	CPU output clock
PCLK1	7	CPU output clock
V _{DD}	8	Digital voltage supply
PCLK2	9	CPU output clock
PCLK3	10	CPU output clock
V _{SS}	11	Ground
S1	12	CPU clock select input, bit 1
S0	13	CPU clock select input, bit 0
V _{DD}	14	Digital voltage supply
BCLK0	15	PCI output clock
BCLK1	16	PCI output clock
V _{SS}	17	Ground
BCLK5	18	PCI output clock
BCLK4	19	PCI output clock
V _{DD}	20	Digital voltage supply
BCLK3	21	PCI output clock
BCLK2	22	PCI output clock
V _{SS}	23	Ground
24 MHz	24	Floppy disk output clock (24 MHz)
12 MHz	25	Keyboard controller clock (12 MHz)
V _{DD}	26	Digital voltage supply
REF1	27	Reference clock output (14.318 MHz)
REF0	28	Reference clock output (14.318 MHz)

Notes:

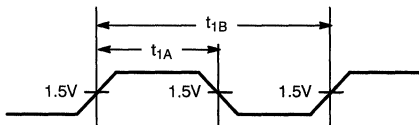
- For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.

Electrical Characteristics $V_{DD} = 3.3V \pm 5\%$, $T_C = 0^\circ C$ to $+70^\circ C$

Parameter	Description	Test Conditions	Min.	Max.	Unit	
V_{IH}	High-level Input Voltage	Except Crystal Inputs	2.0		V	
V_{IL}	Low-level Input Voltage	Except Crystal Inputs		0.8	V	
V_{OH}	High-level Output Voltage	$V_{DD} = V_{DD} \text{ Min.}$	$I_{OH} = 6 \text{ mA}$	PCLK	2.4	V
			$I_{OH} = 12 \text{ mA}$	BCLK, REF0		
			$I_{OH} = 4 \text{ mA}$	24, 12 MHz		
			$I_{OH} = 8 \text{ mA}$	REF1		
V_{OL}	Low-level Output Voltage	$V_{DD} = V_{DD} \text{ Min.}$	$I_{OL} = 6 \text{ mA}$	PCLK	0.4	V
			$I_{OL} = 12 \text{ mA}$	BCLK, REF0		
			$I_{OL} = 4 \text{ mA}$	24, 12 MHz		
			$I_{OL} = 8 \text{ mA}$	REF1		
I_{IH}	Input High Current	$V_{IH} = V_{DD} - 0.5V$	-5	+5	μA	
I_{IL}	Input Low Current	$V_{IL} = 0.5V$	-5	+5	μA	
I_{OZ}	Output Leakage Current	Three-state	-10	+10	μA	
I_{DD}	Power Supply Current	$V_{DD} = 3.465$, $V_{IN} = 0$ or V_{DD}		90	mA	

Switching Characteristics^[4]

Parameter	Output	Name	Description	Min.	Max.	Unit
t_1	All	Output Duty Cycle ^[5]	$t_1 = t_{1A} + t_{1B}$	40%	60%	
t_2	PCLK, BCLK	Output Slew Rate	0.4–2.4V	1		V/ns
t_3	REF, 24, 12 MHz	Rise Time	0.4–2.4V		4	ns
t_4	REF, 24, 12 MHz	Fall Time	2.4–0.4V		4	ns
t_5	PCLK	CPU Skew	CPU-CPU clock skew		250	ps
t_6	BCLK	PCI Skew	PCI-PCI clock skew		500	ps
t_7	PCLK, BCLK	CPU-PCI Skew	CPU to PCI clock skew (CPU leads)	1	5	ns
t_8	PCLK	Cycle-Cycle Clock Jitter	RMS clock jitter		200	ps

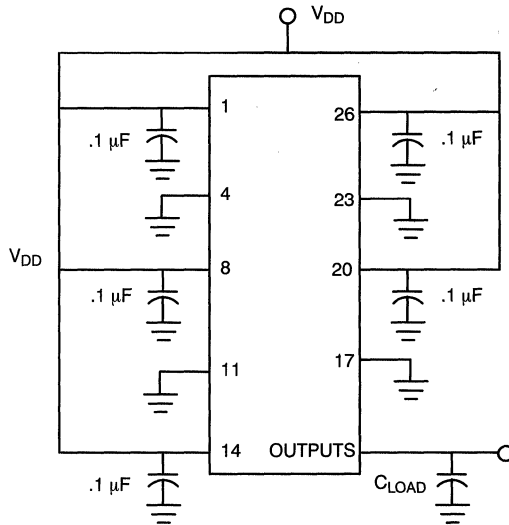
Switching Waveforms
Duty Cycle Timing


2254-3

Notes:

4. All parameters specified with outputs fully loaded.

5. Duty cycle is measured at 1.5V.

Test Circuit


Note: All capacitors should be placed as close to each pin as possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2254	S21	28-Pin SOIC	Commercial

Document #: 38-00426

Pin Summary

Name	Number	Description
V _{DD}	1	Digital voltage supply
XTALIN ^[1]	2	Reference crystal input
XTALOUT ^[1]	3	Reference crystal feedback
GND	4	Ground
OE	5	Output Enable, Active HIGH
CPUCLK0_Z	6	CPU clock output, three-stateable by OE
CPUCLK1_Z	7	CPU clock output, three-stateable by OE
V _{DD}	8	Digital voltage supply
CPUCLK2	9	CPU clock output
CPUCLK3	10	CPU clock output
GND	11	Ground
S1	12	CPU clock select input, bit 1
S0	13	CPU clock select input, bit 0
V _{DD}	14	Digital voltage supply
PCICLK0	15	PCI clock output
PCICLK1	16	PCI clock output
GND	17	Ground
PCICLK5	18	PCI clock output
PCICLK4	19	PCI clock output
V _{DD}	20	Digital voltage supply
PCICLK3	21	PCI clock output
PCICLK2	22	PCI clock output
GND	23	Ground
CPUCLK4	24	CPU clock output
ECLK	25	Early clock output, leads CPU clocks by 2 to 5 ns
V _{DD}	26	Digital voltage supply
REF1	27	Reference clock output (14.318 MHz)
REF0	28	Reference clock output (14.318 MHz)

Notes:

1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V _{OH}	HIGH-level Output Voltage	V _{DD} = V _{DD} Min.	I _{OH} = 6 mA	CPUCLK, ECLK	2.4		V
			I _{OH} = 12 mA	PCICKL, REF0			
			I _{OH} = 8 mA	REF1			
V _{OL}	LOW-level Output Voltage	V _{DD} = V _{DD} Min.	I _{OL} = 6 mA	CPUCLK, ECLK		0.4	V
			I _{OL} = 12 mA	PCICKL, REF0			
			I _{OL} = 8 mA	REF1			
V _{IH}	HIGH-level Input Voltage	Except Crystal Inputs			2.0		V
V _{IL}	LOW-level Input Voltage	Except Crystal Inputs				0.8	V
I _{IH}	Input HIGH Current	V _{IH} = V _{DD} - 0.5V			-5	+5	μA
I _{IL}	Input LOW Current	V _{IL} = 0.5V			-5	+5	μA
I _{OZ}	Output Leakage Current	Three-state outputs			-10	+10	μA
I _{DD}	Power Supply Current	V _{DD} = 3.465, V _{IN} = 0 or V _{DD}				90	mA

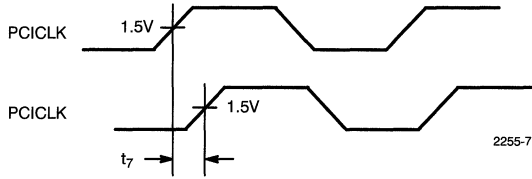
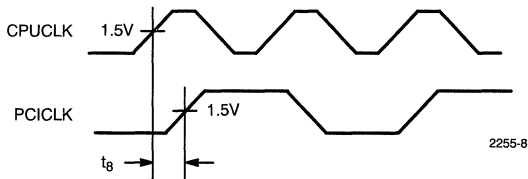
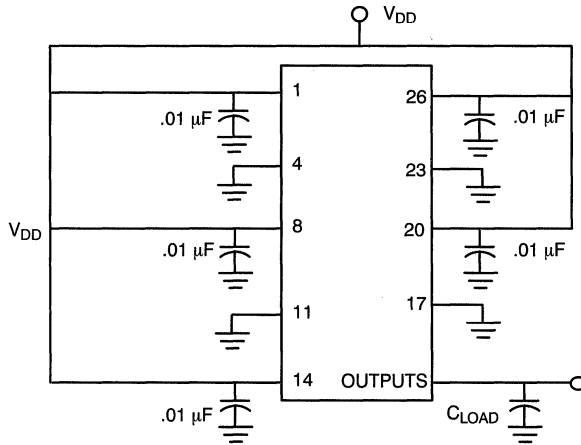
Switching Characteristics^[4]

Parameter	Output	Name	Description	Min.	Max.	Unit
t ₁	All	Output Duty Cycle ^[5]	t ₁ = t _{1A} + t _{1B}	40%	60%	
t ₂	CPUCLK, ECLK, PCICKL	Output Slew Rate	0.4–2.4V	1		V/ns
t ₃	REF0	Rise Time	20% – 80% of V _{DD}		2.5	ns
t ₃	REF1	Rise Time	20% – 80% of V _{DD}		4	ns
t ₄	REF0	Fall Time	20% – 80% of V _{DD}		2.5	ns
t ₄	REF1	Fall Time	20% – 80% of V _{DD}		4	ns
t ₅	CPUCLK	CPU Skew	CPU-CPU clock skew		250	ps
t ₆	ECLK, CPUCLK	ECLK Skew	Early-CPU clock skew (ECLK leads)	2	5	ns
t ₇	PCICKL	PCI Skew	PCI-PCI clock skew		500	ps
t ₈	CPUCLK, PCICKL	CPU-PCI Skew	CPU to PCI clock skew (CPU leads)		750	ps
t ₉	CPUCLK	Cycle-Cycle Clock Jitter	Clock jitter		250	ps

Notes:

4. All parameters specified with outputs fully loaded.

5. Duty cycle is measured at 1.5V.

Switching Waveforms (continued)
PCI-PCI Clock Skew

CPU-PCI Clock Skew

Test Circuit


Note: All capacitors should be placed as close to each pin as possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2255	S21	28-Pin SOIC	Commercial

Pin Summary

Name	Number	Description
32XOUT	1	32.768 kHz crystal feedback
32K	2	32.768 kHz output (always active if V_{BATT} is present)
CLKC	3	Configurable clock output C
V_{DD}	4	Voltage supply to I/O
GND	5	Ground
XTALIN ^[1, 2]	6	Reference crystal input
XTALOUT ^[1, 2]	7	Reference crystal feedback
XBUF	8	Buffered reference clock output
CLKD	9	Configurable clock output D
CPUCLK	10	CPU frequency clock output
CLKB	11	Configurable clock output B
CLKA	12	Configurable clock output A
FLOPPYCLK	13	Floppy clock output (24 or 32 MHz)
S0	14	CPU clock select input, bit 0
S1	15	CPU clock select input, bit 1
V_{DD}	16	Analog voltage supply to core
S2/SUSPEND	17	CPU clock select input, bit 2. Optionally enables suspend feature when LOW.
SHUTDOWN/OE	18	Places outputs in three-state ^[3] condition and shuts down chip when LOW. Optionally, only places outputs in three-state ^[3] condition and does not shut down chip when LOW.
V_{BATT}	19	Battery supply for 32.768 kHz circuit
32XIN	20	32.768 kHz crystal input

Operation

The CY2291 is a third-generation Clock Generator, upwardly compatible with the industry standard ICD2023 and ICD2028. The CY2291 continues the tradition of these parts by providing a high level of customizable features to meet the diverse clock generation needs of modern multi-function motherboards and other synchronous systems.

The CY2291 provides a highly configurable set of clocks for PC motherboard applications. Each of the four configurable clock outputs can be assigned 1 of 30 frequencies in any combination. Multiple outputs configured for the same frequency will have low (≤ 500 ps) skew, in effect providing on-chip buffering for heavily loaded signals.

The CY2291 includes two independent power-saving modes for Green PC or laptop applications. Shutdown mode, controlled by the SHUTDOWN/OE pin, shuts down all of the active circuitry on the chip except for the 32 kHz oscillator. The resulting current draw on the V_{DD} pins is typically less than 10 μ A. Suspend mode, controlled by the S2/SUSPEND pin, shuts down a customizable set of outputs and/or PLLs when they are not needed. In addition to these two modes, most configurations support disabling unused outputs and PLLs.

The CY2291 can be configured for either 5V or 3.3V operation. The internal ROM tables use EPROM technology, allowing

Notes:

- For best accuracy, use a parallel-resonant crystal.
- Assume $C_{LOAD} \approx 17$ pF.

factory configuration for operation at non-standard frequencies. The reference oscillator has been designed for 10 MHz to 25 MHz crystals, providing additional flexibility. All configurations are factory programmable, providing short sample and production lead times.

Output Configuration

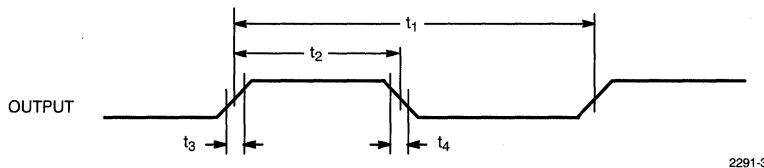
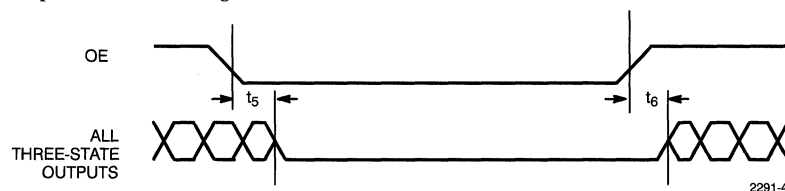
The CY2291 has five independent frequency sources on chip. These are the 32 kHz oscillator, the reference oscillator, and three Phase Locked Loops (PLLs). Each PLL has a specific function. The SYSCLK PLL drives the FLOPPYCLK output and provides the fixed frequencies on the configurable outputs. The CPU PLL responds to the select inputs (S0–S2) to provide eight user selectable frequencies with smooth slewing between frequencies. The Utility PLL is available to provide miscellaneous frequencies not provided by the other frequency sources.

The CY2291 has four fixed frequency outputs (32K, XBUF, FLOPPYCLK, and CPUCLK) and four configurable outputs (CLKA–CLKD). Each of these configurable outputs has an identical set of 30 output frequency options. The list of frequency options includes frequencies derived from four of the five sources on the chip. Please refer to the application note “Understanding the 2291” for information on configuring the part.

- The CY2291 has weak pull-downs on all outputs (except 32K). Hence, when a three-state condition is forced on the outputs, the output pins are pulled LOW.

Switching Characteristics^[7]

Parameter	Name	Description	Min.	Typ.	Max.	Unit
t ₁	Output Period	Clock output range, 5V operation	10 (100 MHz)		5000 (200 KHz)	ns
t ₁	Output Period	Clock output range, 3.3V operation	12.5 (80 MHz)		5000 (200 KHz)	ns
	Output Duty Cycle ^[8]	Duty cycle for outputs, defined as $t_2 \div t_1$ ^[9]	40%	50%	60%	
t ₃	Rise time	Output clock rise time ^[10]			5	ns
t ₄	Fall time	Output clock fall time ^[10]			4	ns
t ₅	Output Disable Time	Time for output to enter three-state mode after SHUTDOWN/OE goes LOW			15	ns
t ₆	Output	Time for output to leave three-state mode after SHUTDOWN/OE goes HIGH			15	ns
t ₇	Skew	Skew delay between any identical or related outputs, as measured @ TTL V _{th} ^[11]		< 0.25	0.5	ns
t ₈	CPUCLK Slew	Frequency transition rate	2.0		20.0	MHz/ ms
t _{9A}	Clock Jitter	Peak-to-peak period jitter (t _{9A} max. - t _{9A} min.) percent of clock period		< 2	5	%
t _{9B}	Clock Jitter	Peak-to-peak period jitter (f _{OUT} ≥ 16 MHz)			700	ps
t _{9C}	Clock Jitter	±3σ jitter (CPUCLK @ ≥ 50 MHz)			250	ps
t ₁₀	Lock Time	Time for VCO to settle between changes		5	50	ms
	Slew Limits		4		100 (5V) 80 (3.3V)	MHz

Switching Waveforms
All Outputs Duty Cycle and Rise/Fall Time

Output Three-State Timing^[3]

Note:

7. Guaranteed by design, not 100% tested.
8. XBUF duty cycle depends on XTALIN duty cycle.
9. Measured at 1.4V.
10. Measured between 0.4V and 2.4V.

11. "Related" outputs are defined as having identical sources internally. Generally they are multiples of each other. To meet the skew guarantee, outputs must have identical capacitive loads.



CY2291 CONFIGURATION REQUEST FORM

Customer _____ Contact _____ FAE/Sales _____

Phone # _____ Fax # _____ Date _____

1. OPERATING VOLTAGE (circle one) 3.3V 5.0V

2. INPUT REFERENCE FREQUENCY
Default reference = 14.318 MHz. If a different reference is desired, please enter value between 10 and 25 MHz.

3. PLL FREQUENCIES
Harmonics will result at the outputs if two or more PLLs run at frequencies which are integral multiples of each other. Note: "Off" is a valid frequency for any PLL.

	Select			Requested	Actual		
	S2	S1	S0				
CPLL (CPU PLL) <i>If suspend option chosen, then request frequencies only for S2 = 1</i>	0	0	0	<input type="text"/>	<input type="text"/>		
	0	0	1	<input type="text"/>	<input type="text"/>		
	0	1	0	<input type="text"/>	<input type="text"/>	<i>shaded areas for Cypress use only</i>	
	0	1	1	<input type="text"/>	<input type="text"/>		
	1	0	0	<input type="text"/>	<input type="text"/>		
	1	0	1	<input type="text"/>	<input type="text"/>		
		1	1	0	<input type="text"/>	<input type="text"/>	
		1	1	1	<input type="text"/>	<input type="text"/>	
UPLL (UTILITY PLL)				<input type="text"/>	<input type="text"/>	<i>shaded areas for Cypress use only</i>	
SPLL (SYSCLK PLL) <i>Default frequency is 96 MHz @ 5V, 48 MHz @ 3.3V</i>				<input type="text"/>	<input type="text"/>	<i>shaded areas for Cypress use only</i>	

4. OUTPUT CONFIGURATION

Available Output Options

- | | | | | | |
|----------|------------|------------|-------------|-------------|--------------|
| 1. Ref | 6. CPLL/2 | 11. UPLL/4 | 16. SPLL/4 | 21. SPLL/12 | 26. SPLL/40 |
| 2. Ref/2 | 7. CPLL/4 | 12. UPLL/8 | 17. SPLL/5 | 22. SPLL/13 | 27. SPLL/48 |
| 3. Ref/4 | 8. CPLL/8 | 13. SPLL | 18. SPLL/6 | 23. SPLL/20 | 28. SPLL/52 |
| 4. Ref/8 | 9. UPLL | 14. SPLL/2 | 19. SPLL/8 | 24. SPLL/24 | 29. SPLL/96 |
| 5. CPLL | 10. UPLL/2 | 15. SPLL/3 | 20. SPLL/10 | 25. SPLL/26 | 30. SPLL/104 |

CLKA (select 1–30, off)

CLKB (select 1–30, off)

CLKC (select 1–30, off)

CLKD (select 1–30, off)

for CLKD, Ref/8 is replaced with Ref/3

CPUCLK (select 5 or off)

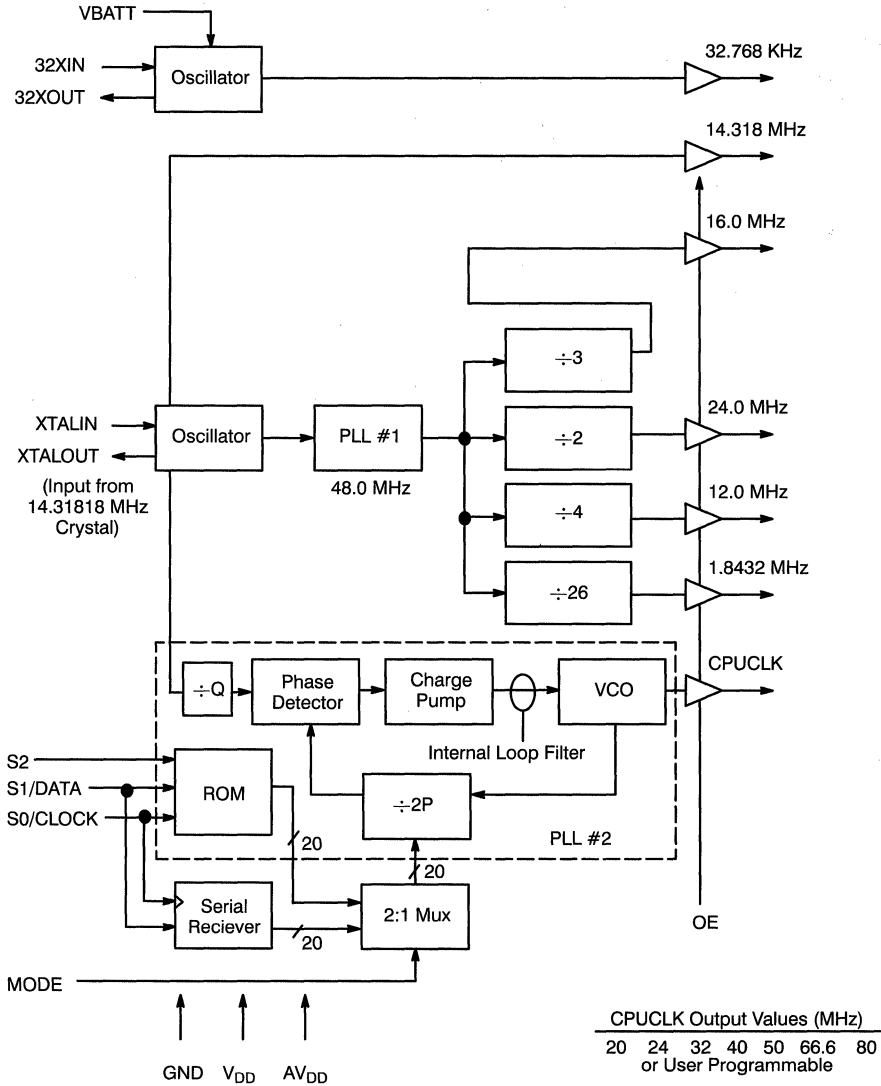
FLOPPYCLK (select 14, 15, 16, or off)

XBUF (select 1 or off)

- 5. SHUTDOWN OPTION (circle one)** Y N
- 6. SUSPEND OPTION (circle one)** Y N
If Yes, assign resources by circling any of the following: Suspending a PLL automatically suspends its outputs.
- | | | |
|------|-----------|------|
| CPLL | XBUF | CLKA |
| UPLL | CPUCLK | CLKB |
| SPLL | FLOPPYCLK | CLKC |
| | | CLKD |

7. FOR CYPRESS / IC DESIGNS USE ONLY

Customer Configuration	Marking
Date	Quantity

Logic Block Diagram


ICD2023-2

CPUCLK Programmable Oscillator: Selection Mode

CPUCLK offers a programmable output based on two modes of operation. The first mode uses three select lines to select one of eight different preset frequencies, while the other mode allows the user to program any desired frequency between 10 MHz and 80 MHz. The two different modes are controlled by the MODE signal.

When MODE=1, the select lines can be changed to choose different frequencies. When this occurs, PLL #2 will immediately seek the newly selected frequency as shown in the following table. During the transition period, the CPUCLK output will not glitch.

Table 2. CPUCLK Output with MODE=1

S2	S1	S0	Desired Freq. (MHz)	Actual Freq. (MHz)	PPM Error
0	0	0	20.000	20.0454	2272
0	0	1	24.000	23.9746	1058
0	1	0	32.000	32.0455	1422
0	1	1	40.000	40.0909	2272
1	0	0	50.000	49.9923	154
1	0	1	66.667	66.5962	57
1	1	0	80.000	80.1818	2272
1	1	1	100.000 ^[8]	99.8182	1818

CPUCLK Programmable Oscillator: Serial Mode

When MODE=0, CPUCLK enters its programmable mode. Signals S0 (clock) and S1 (data) become a serial interface, allowing a 20-bit number to be shifted in. In ICD2023 programmable oscillator (CPUCLK) requires a 20-bit programming word (W). This word contains 4 fields:

Table 3. Programming Word Bit Fields

Field	# of Bits
Index (I) ^[9]	4
P Counter value (P)	7
Mux (M)	3
Q Counter Value (Q) ^[10]	6

If a signal S2=1 and MODE=0, then the reference frequency (14.31818 MHz) is multiplexed to the CPUCLK output. This enables a glitch-free transition to the reference frequency while the VCO stabilizes.

The frequency of the programmable oscillator f_{VCO} is determined by these fields as follows:

$$P' = P - 3 \quad Q' = Q - 2$$

$$f_{VCO} = 2 \times f_{(REF)} \times P/Q$$

where $f_{(REF)}$ = Reference frequency = 14.31818 MHz.

The value of f_{VCO} should be kept between 40 MHz and 80 MHz. Therefore, for output frequencies below 40 MHz, f_{VCO} must be multiplied up into the required range. The mux bits allow a post-divide of the higher VCO to bring the output to those desired values below 40 MHz.

Notes:

- Duty cycle specs not guaranteed above 80 MHz.
- MSB (Most Significant Bits).

Table 4. Mux Bits M₀–M₁

M ₁	M ₀	Divisor
0	0	16
0	1	4
1	0	2
1	1	1

The M2 mux bit is used to select which one of the two Phase-Locked Loops is to be utilized in the CPUCLK output. Normally, the PLL #2 section (see Logic Block Diagram) is used. However, if the desired output frequency requires f_{VCO} to be set to 48 MHz, then PLL #1 section should be used. This both reduces power consumption (since only one VCO is activated) and eliminates the possibility of jitter which can arise when two VCOs of the same frequency beat (heterodyne) against each other.

Table 5. Mux Bits M₂

M ₁	CPUCLK
0	PLL #2
1	PLL #1 (48 MHz)

The Index field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from Table 6. (Note that this table is referenced to the VCO frequency f_{VCO} , rather than to the desired output frequency.)

Table 6. Index Field (I)

I	f_{VCO} MHz
0001	40.0–47.5
0010	47.5–52.2
0011	52.2–56.3
0100	56.3–61.9
0101	61.9–65.0
0110	65.0–68.1
0111	68.1–80.0
1111	Turn off VCO

If the desired VCO frequency lies on a boundary in the table (if it is exactly the upper limit of one entry and the lower limit of the next) then either index value may be used (since both limits are tested), but we recommend using the higher one.

To assist with these calculations, Cypress/IC Designs provides *BitCalc* (Part #ICD/BCALC), a Windows™ program which automatically generates the appropriate programming words from the user's reference input and desired output frequencies, as well as assembling the program words for such things as control and power-down registers. Contact your local Cypress representative for more information.

- LSB (Least Significant Bits).

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V _{BATT}	Backup Battery Voltage	Typical=3.0 Volts	2.0	5.0	V
V _{OH}	Output HIGH Voltage	I _{OH} = - 4.0mA	2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 4.0 mA		0.4	V
V _{OH-32}	32.768 kHz Output HIGH				V
V _{OL-32}	32.768 kHz Output LOW				V
V _{IL}	Input LOW Voltage	Except crystal inputs		0.8	V
V _{IH}	Input HIGH Voltage	Except crystal inputs	2.0		V
I _{IH}	Input HIGH Current	V _{IH} = V _{DD} -0.5V		150	μA
I _{IL}	Input LOW Current	V _{IL} = +0.5V		-250.0	μA
I _{OZ}	Output Leakage Current	(Three-state)		10	μA
I _{DD}	Supply Current	V _{DD} = Max., fully loaded output, typical = 40 ^[11]	25	65.0	mA
I _{BATT}	Backup Battery Current	V _{BATT} = 3V, fully loaded output, typical = 8 μA		50	μA

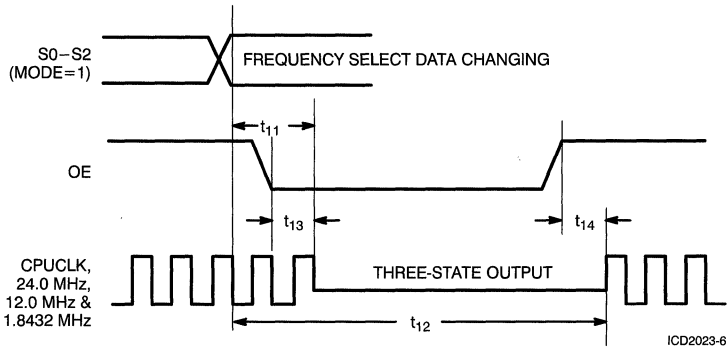
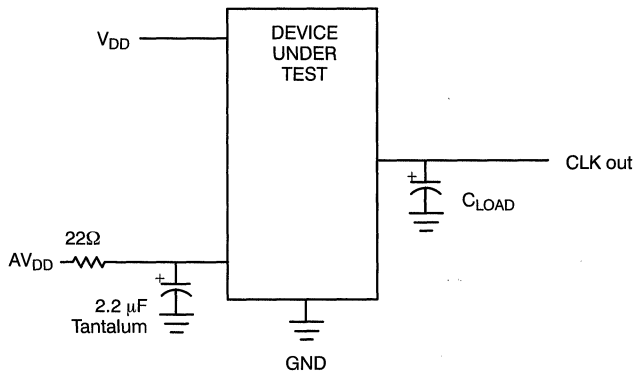
Switching Characteristics Over the Operating Range^[12]

Parameter	Description	Test Conditions	Min.	Max.	Unit
	CPUCLK	Clock Output	10	80	MHz
t ₁	Ref Frequency	Reference Oscillator nominal value		14.318	MHz
t ₂	Duty Cycle	Duty cycle for the outputs defined as t _{2A} ÷ t _{2B}	40%	60%	
t ₃	Rise Time	Rise time for the outputs into a 25 pF load		4	ns
t ₄	Fall Time	Fall time for the outputs into a 25 pF load		4	ns
t ₅	Set-Up Time	Delay required after MODE goes LOW prior to starting the S0 clock line		0	ns
t ₆	Cycle Time	Minimum cycle time for the S0 clock	200		ns
t ₇	Set-Up Time	Time required for the data to be valid prior to the rising edge of S0/CLOCK	10		ns
t ₈	Hold Time	Time required for the data to remain valid prior to the rising edge of S0/CLOCK	5		ns
t ₉	Clk Unstable	Time CPUCLK remains valid after MODE signal goes LOW		0	ns
t ₁₀	Clk Stable	Time required for the CPUCLK to become valid after last S0/clock edge		10	msec
t ₁₁	Clk Unstable	Time the output oscillators remain valid after the S0, S1 or S2 select signals change value		0	ns
t ₁₂	Clk Stable	Time required for the outputs to become valid after the S0, S1, or S2 signals change value		10	msec
t ₁₃	Three-State	Time for the output to go into three-state mode after OE signal assertion		12	ns
t ₁₄	Clk Valid	Time for the outputs to recover from three-state mode after OE signal goes HIGH		12	ns

Notes:

 11. CPUCLK = 66 MHz and inputs at GND or V_{DD}.

12. Input capacitance is typically 10 pF, except for the crystal pads.

Switching Waveforms (continued)
State Timing

Test Circuit

Ordering Information^[13]

Ordering Code	Package Name	Package Type	Operating Range
ICD2023	S5	20-Pin SOIC	Commercial ^[14]

Note:

13. Please contact your local Cypress representative.

14. 0°C to +70°C

Document #: 38-00397

Windows is a trademark of Microsoft Corporation.

Pin Summary

Name	Number	Description
SYSBUS	1	Buffered 14.31818 MHz crystal output (z)
SYSClk	2	System clock output (see <i>Table 2</i>)
OE	3	Output Enable three-states output when signal is LO. (pin has internal pull-up)
GND	4	Ground
f _{REF} / XTALIN ^[1]	5	Reference Oscillator input for all internal phase-locked loops (nominally from a parallel-resonant 14.31818 MHz crystal). Optionally PC System Bus Clock.
XTALOUT ^[1]	6	Oscillator output to a reference crystal.
C0	7	CPUClk Select signal—Bit 0 (internal pull-up)
S0	8	SYSClk Clock Select signal—Bit 0 (internal pull-up)
S1	9	SYSClk Select signal—Bit 1 (internal pull-up)
C1	10	CPUClk Select signal—Bit 1 (internal pull-up)
C2	11	CPUClk Select signal—Bit 2 (internal pull-up)
S2	12	SYSClk Select signal—Bit 2 (internal pull-up)
VDD	13	+5V to I/O Ring
C3	14	CPUClk Select signal—Bit 3 (internal pull-down)
CPUClk	15	CPU Clock Output (See CPUClk Selection Table)
AVDD	16	+5V to Analog Core

Available Frequencies (MHz)

SYSClk	CPUClk
1.843	16.000
3.686	20.000
8.000	25.000
12.000	32.000
18.432	33.333
20.000	40.000
24.000	50.000
32.000	66.667
	80.000
	100.000

Note:

- For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Input Voltage -0.5V to $V_{DD} + 0.5V$
 Storage Temperature -65°C to +150°C
 Max soldering temperature (10 sec) 260°C

Junction temperature 125°C

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
$0^{\circ}C \leq T_{AMBIENT} \leq 70^{\circ}C$	$5V \pm 5\%$

Electrical Characteristics Over the Operating Range

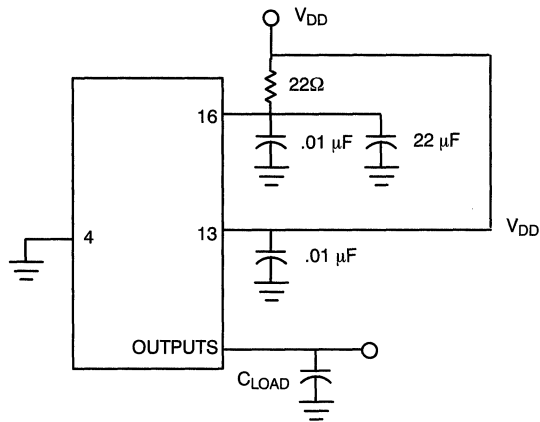
Parameter	Description	Test Conditions	ICD2025		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	$I_{OH} = -4.0mA$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 4.0 mA$		0.4	V
V_{IH}	Input HIGH Voltage	Except crystal inputs	2.0		V
V_{IL}	Input LOW Voltage	Wcept crystal inputs		0.8	V
I_{IH}	Input HIGH Current	$V_{IH} = V_{DD} - 0.5V$		150	μA
I_{IL}	Input LOW Current	$V_{IL} = 0.5V$		-250	μA
I_{OZ}	Output Leakage Current	(Three-state)		10	μA
I_{DD}	Power Supply Current	Inputs @ V_{DD} or GND		60	mA
I_{ADD}	Analog Power Supply Current			6	mA

Switching Characteristics Over the Operating Range^{2]}

Parameter	Name	Description	Min.	Typ.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference Oscillator nominal value	4	14.318	26	MHz
$t_{(REF)}$	Ref Clock Period	$1 \div f_{(REF)}$	38.5	69.8	2500	ns
t_1	Input Duty Cycle	Duty cycle for the inputs defined as $t_1 \div t_{(REF)}$	25%	50%	75%	
t_2	Output Period	CPUCLOCK output value	10 100 MHz		544 1.84 MHz	ns
t_3	Output Duty Cycle	Duty cycle for the outputs defined as $t_3 \div t_2$ (measured at 2.5V)	40%		60%	
t_4	Rise Time	Rise time for the outputs into a 25 pF load			4	ns
t_5	Fall Time	Fall time for the outputs into a 25 pF load			4	ns
t_6	Three-State	Time for the outputs to go into three-state mode after OE signal assertion			12	ns
t_7	Clk Valid	Time for the outputs to recover from three-state mode after OE signal goes HIGH			12	ns
t_{MURF}	Clk Stable	Time required for the outputs to become valid after C0-C3 or S0-S2 select signals change value	3.4	5	6.9	msec
t_{freq1}	freq1 Output	Old frequency output				
t_{freq2}	freq2 Output	New frequency output				
t_8	$f_{(REF)}$ Mux Time	Time clock output remains HIGH while output muxes to reference frequency	$\frac{t_{(REF)}}{2}$		$3 \frac{t_{(REF)}}{2}$	ns
t_9	t_{freq2} Mux Time	Time clock output remains HIGH while output muxes to new frequency value	$\frac{t_{freq2}}{2}$		$3 \frac{t_{freq2}}{2}$	ns

Note:

2. Input capacitance is typically 10 pF, except for the crystal pads.

Test Circuit


Note: All capacitors should be placed as close to each pin as possible.

Ordering Information^[3]

Ordering Code	Package Name	Package Type	Operating Range
ICD2025	S1	16-Pin SOIC	Commercial ^[4]

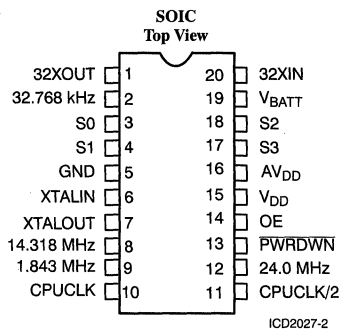
Note:

3. Contact your local Cypress representative.

4. 0°C to +70°C

Example: order ICD2025SC for the ICD2025, 16-pin plastic SOIC, commercial temperature range device.

Document #: 38-00398

Pin Configuration

Pin Summary

Name	Number	Description
32XOUT ^[1]	1	Oscillator output to a 32.768 kHz parallel-resonant crystal
32.768 kHz	2	32.768 kHz clock output
S0	3	Input select line 0 for CPUCLK (pin has internal pull-down)
S1	4	Input select line 1 for CPUCLK (pin has internal pull-down)
GND	5	Ground
XTALIN ^[1]	6	Reference Oscillator input for all internal phase-locked loops (nominally from a parallel-resonant 14.31818 MHz crystal). Optionally PC System Bus Clock.
XTALOUT ^[1]	7	Oscillator Output to a reference crystal.
14.318 MHz	8	14.31818 MHz clock output
1.8432 MHz	9	1.8432 MHz clock output
CPUCLK	10	CPUCLK programmable clock output (See <i>Table 1</i> for values.)
CPUCLK/2	11	Half the frequency of CPUCLK. Output is phase-coherent with the CPUCLK output.
24.0 MHz	12	24.0 MHz clock output
PWRDWN	13	Puts device in Power-Down mode when signal is pulled LOW (pin has internal pull-down)
OE	14	Output Enable three-states output when signal is LOW (pin has internal pull-up)
V _{DD}	15	+5V to I/O ring
AV _{DD}	16	+5V to analog core
S3	17	Input select line 3 for CPUCLK (pin has internal pull-down)
S2	18	Input select line 2 for CPUCLK (pin has internal pull-down)
V _{BATT}	19	+2 to +5V for battery backup operation
32XIN ^[1]	20	Oscillator input from 32.768 kHz crystal

Note:

1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Input Voltage -0.5V to $V_{DD} + 0.5V$
 Storage Temperature -65°C to +150°C
 Max soldering temperature (10 sec) 260°C

Junction temperature 125°C

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
$0^{\circ}\text{C} \leq T_{\text{AMBIENT}} \leq 70^{\circ}\text{C}$	$5V \pm 5\%$

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{BATT}	Backup Battery Voltage	Typical = 3.0V	2.0	5.0	V
V_{IH}	Input HIGH Voltage	Except Crystal Inputs	2.0		V
V_{IL}	Input LOW Voltage	Except Crystal Inputs		0.8	V
V_{OH}	Output HIGH Voltage	$I_{OH} = -4.0\text{ mA}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 4.0\text{ mA}$		0.4	V
I_{IH}	Input HIGH Current	$V_{IH} = 5.25V$		150	μA
I_{IL}	Input LOW Current	$V_{IL} = 0V$		-250	μA
I_{OZ}	Output Leakage Current	(Three-state)		10	μA
I_{DD}	Power Supply Current	Inputs @ V_{DD} or GND	20	65	mA
I_{DD-PD}	Soft Power-Down Current			7.5	mA
I_{BATT}	Backup Battery Current	Typical = 5 μA		15	μA

Switching Characteristics^[6]

Parameter	Name	Description	Min.	Typ.	Max.	Unit
f_{REF}	Reference Frequency	Reference input normal value		14.318		MHz
$t_{(REF)}$	Reference Period	$1 + f_{(REF)}$		69.8		ns
t_1	Duty Cycle	Duty cycle for the output clock defined as $t_{1A} + t_{1B}$	40%		60%	
t_2	Rise Time	Rise time for the outputs into a 25-pF load			4	ns
t_3	Fall Time	Fall time for the outputs into a 25-pF load			4	ns
t_4	Three-state	Time for the outputs to go into three-state mode after OE signal assertion			12	ns
t_5	clk Valid	Time for the outputs to recover from three-state mode after OE signal goes HIGH			12	ns
t_6	CPUCLK/2 Skew	Skew delay between CPUCLK and CPUCLK/2 outputs		1	2	ns
t_{freq1}	freq1 Output	Old frequency output				
t_{freq2}	freq2 Output	New frequency output				
t_7	$f_{(REF)}$ Mux Time	Time clock output remains HIGH while output muxes to reference frequency	$t_{(REF)}/2$		$3(t_{(REF)}/2)$	ns
t_8	t_{freq2} Mux Time	Time clock output remains HIGH while output muxes to new frequency value	$t_{freq2}/2$		$3/(t_{freq2}/2)$	ns
t_{MUXREF}		Time for VCO to settle between changes			6.2	msec

Note:

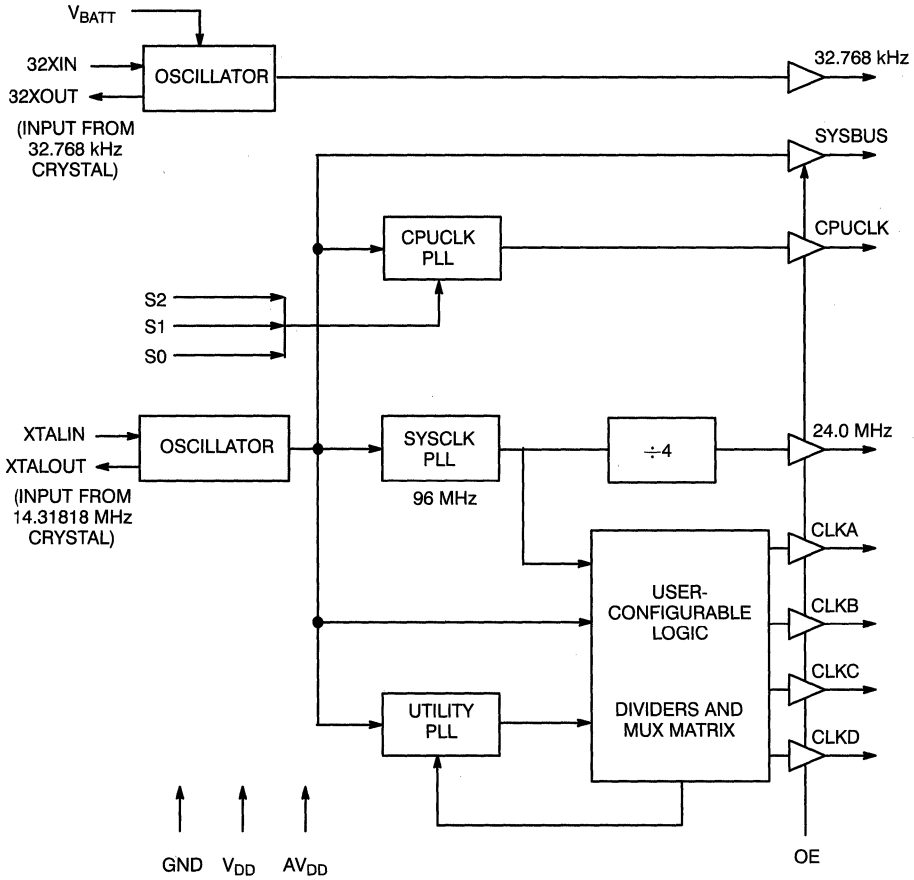
6. Input capacitance is typically 10 pF, except for the crystal pads.

Ordering Information

Ordering Code	Package Name	Package Type	Temperature Range	CPUCLK ROM Option
ICD2027	S5	20-Pin SOIC	C=Commercial=0°C to +70°C	1

Example: Order ICD2027SC-1 for the ICD2027, 20-pin plastic SOIC, commercial temperature range device which uses the standard CPUCLK ROM Option 1 table of frequency decodes. Custom CPUCLK ROM decodes are available by special order. Please call your local Cypress representative.

Document #: 38-00399

Block Diagram


ICD2028-2

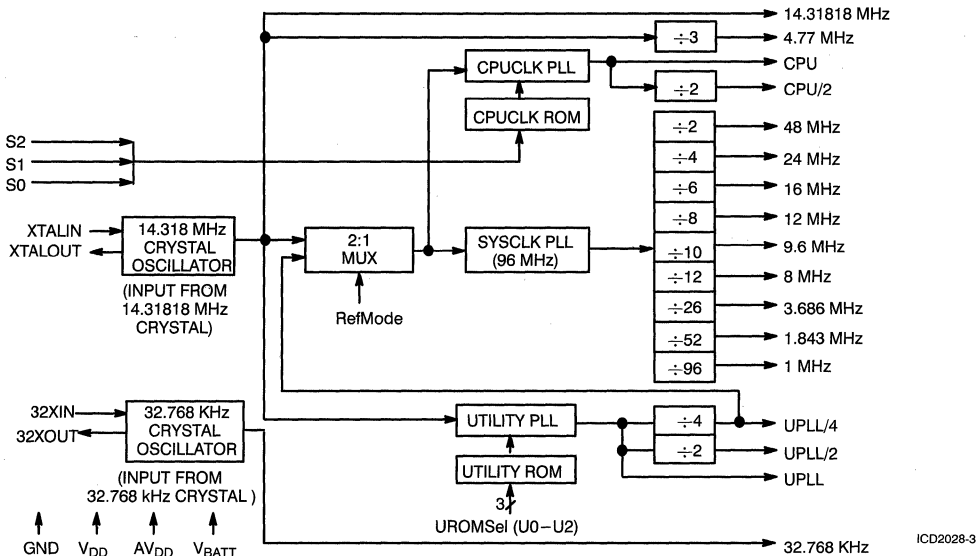
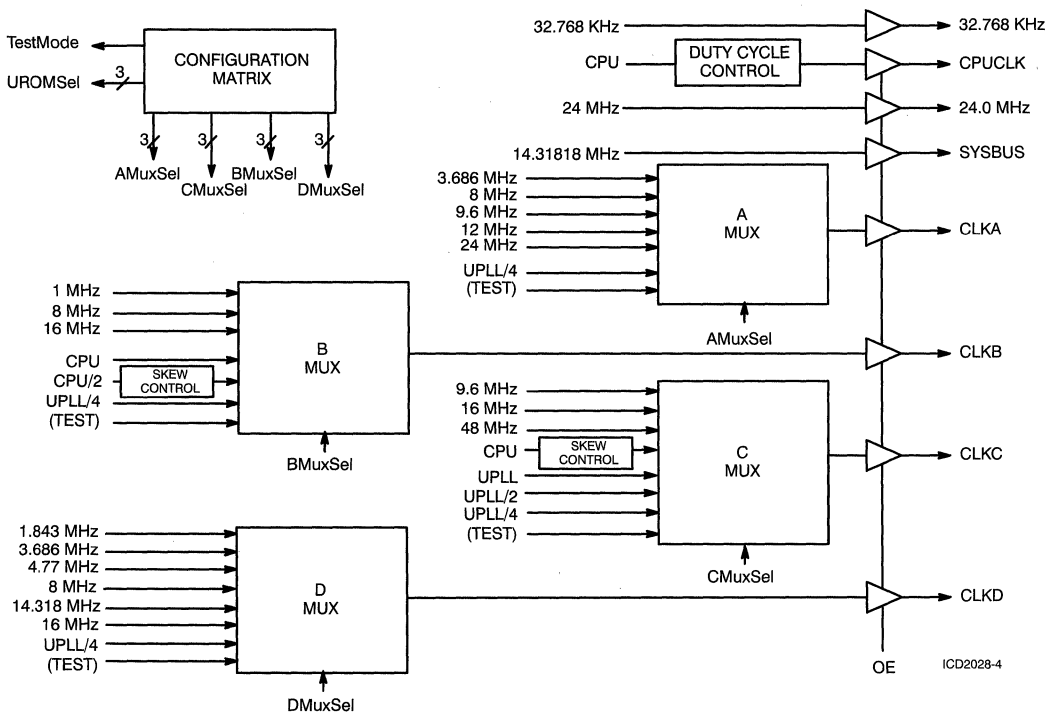

Figure 1. Inputs

Figure 2. Outputs

Table 2. Utility PLL Options

Clock Function	ROM Source ^[2]	Desired Freq. (MHz)	Actual Freq. (MHz)	Error (PPM)	Clock Source ^[3]	Available on Pin (s)			
						CLKA	CLKB	CLKC	CLKD
Alt. Comm. Port	A & B	18.432	18.431	62	Utility PLL/4	X	X	X	X
	A & B	36.864	36.862	62	Utility PLL/2			X	
	A & B	73.728	73.723	62	Utility PLL			X	
Custom	A & B	14.746	14.748	144	Utility PLL/4	X	X	X	X
	A & B	29.492	29.495	144	Utility PLL/2			X	
	A & B	58.984	58.991	144	Utility PLL			X	
Custom	A & B	19.200	19.199	32	Utility PLL/4	X	X	X	X
	A & B	38.400	38.399	32	Utility PLL/2			X	
	A & B	76.800	76.798	32	Utility PLL			X	
Super I/O-1	B	32.000	31.997	102	Utility PLL/4	X	X	X	X
	B	64.000	63.994	102	Utility PLL/2			X	
	B	128.000	127.987	102	Utility PLL			X	
Super I/O-2	B	16.000	16.003	167	Utility PLL/4	X	X	X	X
	B	32.000	32.005	167	Utility PLL/2			X	
	B	64.000	64.011	167	Utility PLL			X	
Shut VCO	A & B	-	-	-	-				
	A & B	-	-	-	-				
	A & B	-	-	-	-				

Notes:

2. Refers to the two currently available ROM Options: A and B.
3. Each clock function outputs three separate frequencies: UPLL, UPLL/2 and UPLL/4.

Table 6. Standard Configurations^[4]

Signal Name	Pin #	-2 Configuration	-4 Configuration	-5 Configuration
Reference Crystal	-	14.318 MHz	14.318 MHz	14.318 MHz
Utility PLL	-	(Off)	(Off)	32.000 MHz
CPUCLK Duty Cycle	-	50%	50%	50%
ROM Option	-	A	B	B
CPUCLK	10	Available	Available	Available
SYSBUS	8	Available	Available	Available
24.0 MHz	13	Available	Available	Available
CLKA	12	12.000 MHz	12.000 MHz	12.000 MHz
CLKB	11	CPUCLK/2	CPUCLK/2	CPUCLK/2
CLKC	3	16.000 MHz	16.000 MHz	32.000 MHz (UPLL/4)
CLKD	9	1.843 MHz	1.843 MHz	1.843 MHz
32.768 kHz	2	Available	Available	Available

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Input Voltage -0.5V to $V_{DD} + 0.5V$
 Storage Temperature -65°C to +150°C
 Max soldering temperature (10 sec) 260°C
 Junction temperature 125°C

Power dissipation 750 mW

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
$0^{\circ}C \leq T_{AMBIENT} \leq 70^{\circ}C$	$5V \pm 5\%$

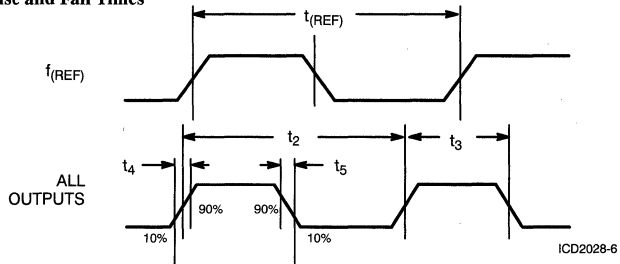
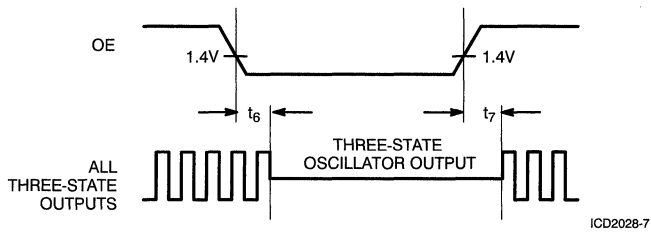
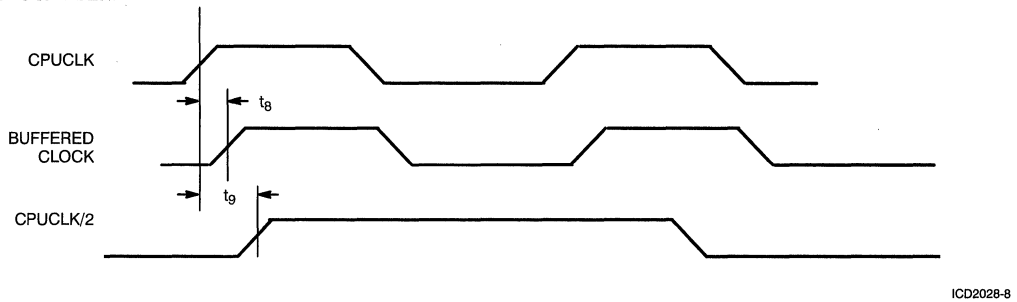
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{BATT}	Backup Battery Voltage	Typical = 3.0 Volts	2.0	5.25	V
V_{OH}	Output HIGH Voltage	$I_{OH} = -4.0$ mA	$V_{DD} - 0.5$		V
V_{OL}	Output LOW Voltage	$I_{OL} = 4.0$ mA		0.4	V
V_{OH-32}	32.768 kHz Output HIGH	$I_{OH} = -0.5$ mA	$V_{BATT} - 0.5$		V
V_{OL-32}	32.768 kHz Output LOW	$I_{OL} = 0.5$ mA		0.4	V
V_{IH}	Input HIGH Voltage	Except crystal inputs	2.0	$V_{DD} + 0.3$	V
V_{IL}	Input LOW Voltage	Except crystal inputs	-0.3	0.8	V
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD} - 0.5V$		150	μA
I_{IL}	Input LOW Current	$V_{IN} = +0.5V$		-250	μA
I_{OZ}	Output Leakage Current	(Three-state)		10	μA
I_{DD}	Power Supply Current	$V_{DD} = \text{Max.}$, fully loaded output, typical = 35 ^[5]	20	85	mA
I_{BATT}	Backup Battery Current	$V_{BATT} = 3V$, fully loaded output, typical = 5 μA		15	μA

Notes:

4. -2 Compatible with most 486 chip sets, while adding skew-free CPUCLK/2 support.
- 4 Supports Pentium™ processor requirements.
- 5 Provides 486 support and Super I/O (32 MHz) support.
5. CPUCLK = 66 MHz and inputs at GND or V_{DD} .

Pentium is a trademark of Intel Corporation.

Switching Waveforms (continued)
Rise and Fall Times

Three-State Timing

CPUCLK Skew


ICD2028 Custom Configuration Order Form

Company Name _____ Contact _____
 Telephone _____ Fax _____

Output Signals

(All frequencies in MHz unless otherwise noted)

(Circle one in each line, or fill in the blanks.)

 Operating Voltage (V_{DD} & AV_{DD}): 5V

Dedicated Pins: 32.768 KHz 24.000

Reference Xtal & SYSBUS Output: 14.31818

CPUCLK (Select desired ROM Option line below.)

ROM Opt. A	[20.0	24.0	32.0	40.0	50.0	66.6	80.0	100.0]
ROM Opt. B	[20.0	24.0	60.0	40.0	50.0	66.6	80.0	100.0]

CPUCLK: Duty Cycle _____% Load _____ pF Frequency _____ MHz
 (default) (50%) (25 pF) (10–100 MHz)

UtilityPLL/4	18.432	14.746	20.000	19.2000	32.000	16.000 ^[1]	OFF
CLKA	3.692	8.000	9.600	12.000	24.000	–	UPLL/4
CLKB	1.000	8.000	16.000	–	CPU ^[2]	CPU/2 ^[2]	UPLL/4
CLKC	9.600	16.000	48.000	CPU ²	UPLL	UPLL/2	UPLL/4
CLKD	1.843	3.686	4.770	8.000	14.318	16.000	UPLL/4

IC Designs Assignment Configuration Code _____
 (For IC Designs use only)

Notes:

1. Only available with ROM Option B.
2. Skew-controlled to CPUCLK output.

Pin Summary

Name	Number	Description
XBUF	1	Buffered reference frequency output (14.318 MHz)
MCLK	2	Memory Clock output (see <i>Table 1</i>)
OE	3	Output Enable, three-states output when signal is LOW (pin has internal pull-up)
GND	4	Ground
$f_{(REF)}/$ XTALIN ^[1]	5	Reference Oscillator input for all internal phase-locked loops (nominally from a parallel-resonant 14.318-MHz crystal).
XTALOUT ^[1]	6	Oscillator output to a reference crystal. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.)
P0	7	Pixel Clock Select input—Bit 0 (internal pull-up)
M0	8	Memory Clock Select input—Bit 0 (internal pull-up)
M1	9	Memory Clock Select input—Bit 1 (internal pull-up)
P1	10	Pixel Clock Select input—Bit 1 (internal pull-up)
P2	11	Pixel Clock Select input—Bit 2 (internal pull-up)
M2	12	Memory Clock Select input—Bit 2 (internal pull-up)
V _{DD}	13	+5V to I/O Ring
P3	14	Pixel Clock Select input—Bit 3 (internal pull-down)
PCLK	15	Pixel Clock Output
AV _{DD}	16	+5V to Analog Core (special order: bond V _{DD} to AV _{DD} internally)

General Considerations
Design Recommendations

The ICD2061A, with its ability to program the output frequencies, is recommended for designs in which a fixed ROM would be inconvenient and/or the desired volume does not warrant a custom ROM.

The ICD2042A is currently a custom order only.

Pixel and Memory Clock Oscillator Selection

The output frequency value of the Pixel clock oscillator (PCLK) is selected by the four Pixel clock selection inputs: P0, P1, P2, and P3. This feature allows the ICD2042A to support different video configurations. The output frequency value of the Memory clock oscillator (MCLK) is selected by the three Memory clock selection inputs: M0, M1, and M2. The selection table is shown in *Table 1*.

At any time during operation, the select lines can be changed to select a different frequency. When this occurs, the internal phase-locked loop will immediately seek the newly selected frequency. During the transition period, the clock output will multiplex glitch-free to the reference signal until the PLL settles to the new frequency.

Normally, the MCLK select lines are hard-wired during manufacturing to correspond to the desired memory speed. A different memory clock frequency output may be generated by changing the memory select lines of the ICD2042A. The timing for this transition is shown in AC Characteristics.

Note:

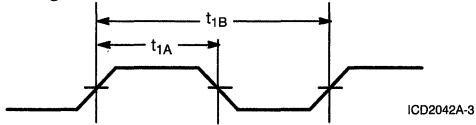
- For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.

Table 1. Memory Clock ROM Decode Options

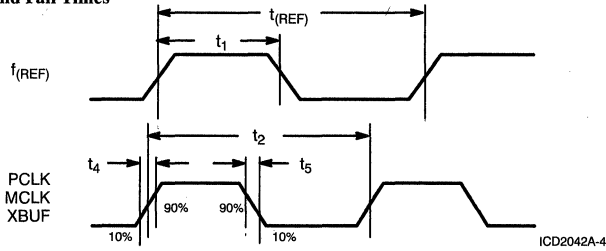
M2	M1	M0	Word	2042-23	2042-24	2042-27
				Frequencies in MHz		
0	0	0	0	48.000	48.000	40.000
0	0	1	1	39.800	39.800	41.000
0	1	0	2	66.000	66.000	41.500
0	1	1	3	50.000	50.000	42.000
1	0	0	4	56.644	56.644	42.500
1	0	1	5	32.200	32.000	43.000
1	1	0	6	44.000	44.000	44.000
1	1	1	7	39.800	39.800	48.000

Three-State Output Operation

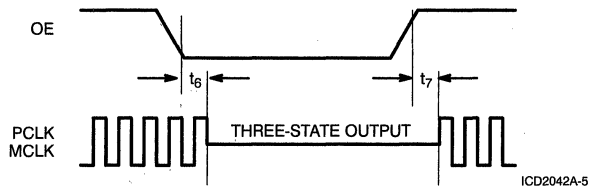
The OE signal, when pulled LOW, will three-state the MCLK, PCLK, and XBUF output lines. This supports procedures such as automated testing, where the clock must be disabled. The OE signal contains an internal pull-up but should be tied to V_{DD} if not used.

Switching Waveforms
Duty Cycle Timing


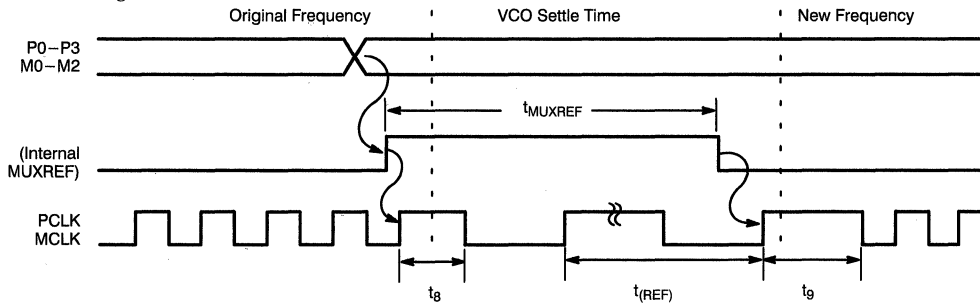
ICD2042A-3

Rise and Fall Times


ICD2042A-4

Three-State Timing


ICD2042A-5

Selection Timing


ICD2042A-6

Dual Programmable Clock Generator

Features

- Two independent clock outputs ranging from 320 kHz to 100 MHz
- Individually programmable PLLs use 22-bit serial word
- Low-skew $\div 1$, $\div 2$, and $\div 4$ CLKA outputs
- Phase-locked loop oscillator input derived from external low-frequency reference clock (1 MHz – 25 MHz) or external crystal (2 MHz – 24 MHz)
- Sophisticated internal loop-filter requires no external components or manufacturing tweaks as commonly required with external filters

- Three-state control disables outputs for test purposes (optional)
- 5V operation
- Low-power, high-speed CMOS technology
- Available in 16-pin SOIC package

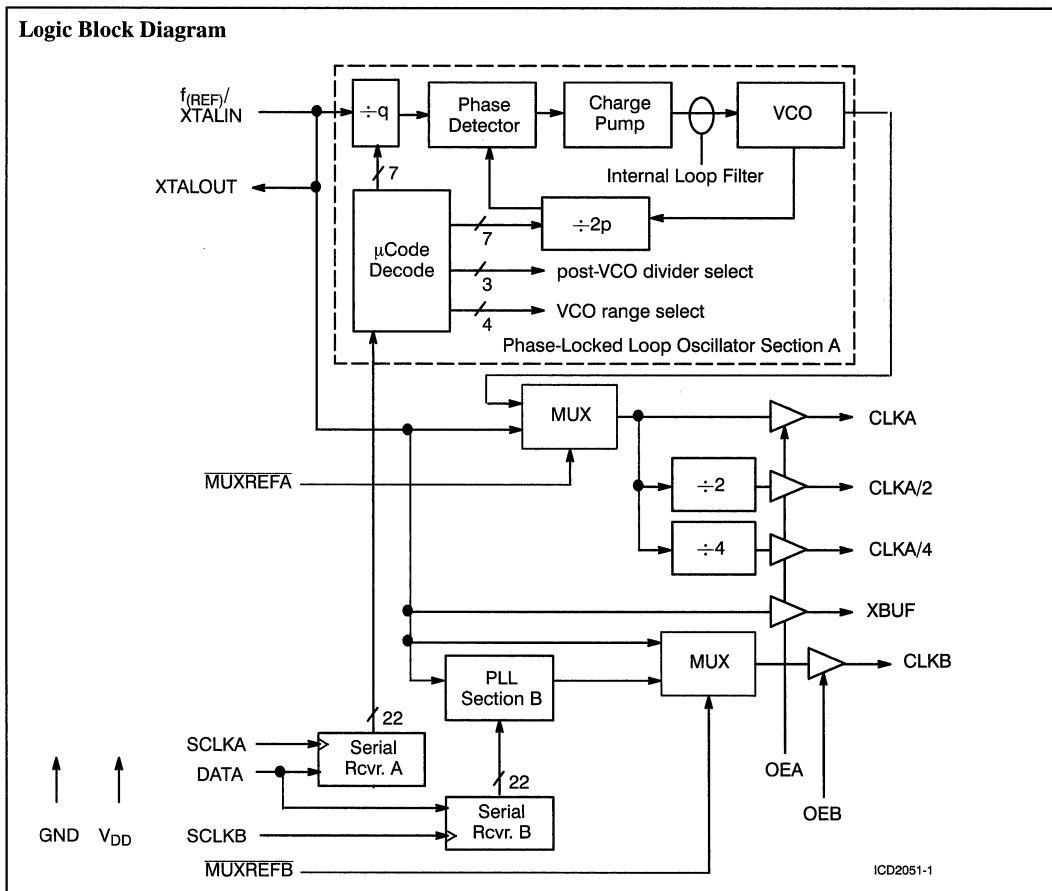
Functional Description

The ICD2051 Programmable Clock Generator offers two fully user-programmable phase-locked loops in a single package. The outputs may be changed "on the fly" to any desired frequency value between 320 kHz and 100 MHz. The ICD2051 is ideally suited for any design where one or more multiple or varying frequencies are

required, thus replacing more expensive metal can oscillators.

The capability to dynamically change the output frequency adds a whole new degree of freedom for the electrical engineer. Some examples of the uses for this device include: laptop computers, in which slowing the speed of operation can mean less power consumption or speeding it up can mean faster operation; graphics board dot clocks to allow dynamic synchronization with different brands of monitors or display formats; and on-board test strategies where the ability to skew a system's desired frequency (for example $\pm 10\%$) allows worst case evaluations.

Logic Block Diagram



General Considerations

Programming the ICD2051

The desired output frequency is defined via a serial interface, with a 22-bin number shifted in. The ICD2051 has two programmable PLLs (CLKA and CLKB), requiring a 22-bit programming word (W) to be loaded into each channel independently. This word contains 5 fields:

Table 1. Programming Word Bit Fields

Field	# of bits	Notes
Index (I)	4	MSB (Most Significant Bits)
P Counter value (P')	7	
Reserved (R)	1	normally set to logic 1
Mux (M)	3	
Q Counter value (Q')	7	LSB (Least Significant Bits)

The frequency of the programmable oscillator $f_{(VCO)}$ is determined by these fields as follows:

$$P' = P - 3$$

$$Q' = Q - 2$$

$$f_{(VCO)} = 2 \times f_{(REF)} \times P/Q$$

where $f_{(REF)}$ = Reference frequency (between 1 MHz – 25 MHz)

The value of $f_{(VCO)}$ must remain between 40 MHz and 120 MHz. Therefore, for output frequencies below 40 MHz, $f_{(VCO)}$ must be multiplied up into the required range. To accomplish this, a post-VCO Divisor is selected by setting the values of the Mux field (M) as follows:

Table 2. Mux Field (M)

M	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The Index field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from Table 3. (Note that this table is referenced to the VCO frequency $f_{(VCO)}$, rather than to the desired output frequency.)

Table 3. Index Field (I)

I	$f_{(VCO)}$ (MHz)
0000	40.0 – 42.5
0001	42.5 – 471.5
0010	47.5 – 53.5
0011	53.5 – 58.5
0100	58.5 – 62.5
0101	62.5 – 68.5
0110	68.5 – 69.0
0111	69.0 – 82.0
1000	82.0 – 87.0
1001	87.0 – 92.0
1010	92.0 – 92.1
1011	92.1 – 105.0
1100	105.0 – 115.0
1101	115.0 – 120.0
1110	115.0 – 120.0
1111	115.0 – 120.0

If the desired VCO frequency lies on a boundary in the table (if it is exactly the upper limit of one entry and the lower limit of the next) then either index value may be used (since both limits are tested), but we recommend using the higher one.

To assist with these calculations, Cypress/IC Designs provides *BitCalc* (Part #ICD/BCALC), a Windows™ program which automatically generates the appropriate programming words from the user's reference input and desired output frequencies. The software also assembles the program words for control and power-down registers. Contact your local Cypress representative for more information.

Programming Constraints

There are five primary programming constraints the user must be aware of:

Table 4. Programming Constraints

Parameter	Minimum	Maximum
$f_{(REF)}$	1 MHz	25 MHz
$f_{(REF)}/Q$	200 kHz	1 MHz
$f_{(VCO)}$	40 MHz	120 MHz
Q	3	129
P	4	130

The constraints have to do with trade-offs between optimum speed and lowest noise, VCO stability and factors affecting the loop equation. The factors are listed for completeness sake; however, by using the *BitCalc* program all of these constraints become transparent.

ICD2051 Programming Example

The following is an example of the calculations *BitCalc* performs: Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency:

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Input Voltage -0.5V to $V_{DD} + 0.5V$
 Storage Temperature -65°C to +150°C
 Max soldering temperature (10 sec) 260°C
 Junction temperature 125°C

Package power dissipation 525 mWatts

Operating Range

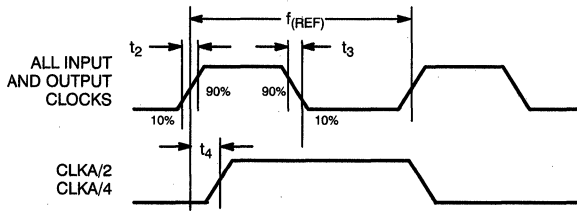
Ambient Temperature	V_{DD} & AV_{DD}
$0^{\circ}C \leq T_{AMBIENT} \leq 70^{\circ}C$	$5V \pm 5\%$

Operating Conditions

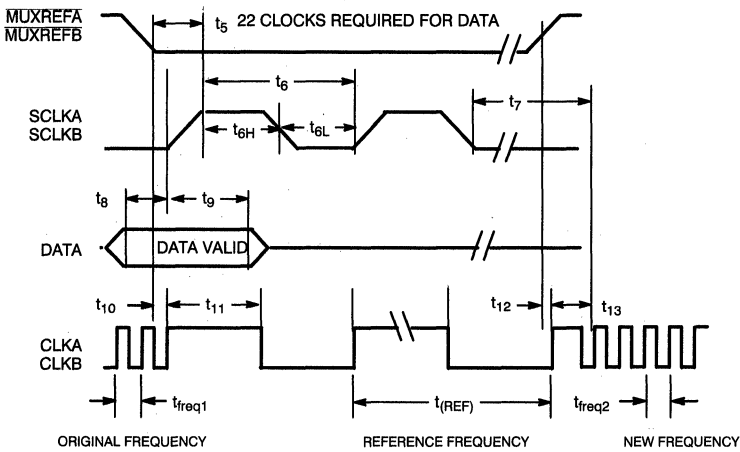
Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	4.75	5.25	V
T_A	Ambient Operating Temperature	0	70	°C
C_L	Load Capacitance		25	pF

Electrical Characteristics Over the Operating Range

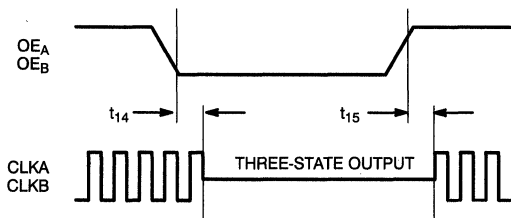
Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -4.0mA$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 4.0 mA$		0.4	V
V_{IH}	Input HIGH Voltage	Except XTALIN pins	2.0		V
V_{IL}	Input LOW Voltage	Except XTALIN pins		0.8	V
I_{IH}	Input HIGH Current	$V_{IN} = 5.25V$		150	μA
I_{IL}	Input LOW Current	$V_{IN} = 0V$		-250	μA
I_{OZ}	Output Leakage Current	Three-state outputs		10	μA
I_{DD}	Power Supply Current	$V_{DD} = V_{DD} \text{ max.}, 100 \text{ MHz}, V_{IN} = V_{DD} \text{ or } 0V$	15	100	mA

Switching Waveforms (continued)
Rise and Fall Times


ICD2051-4

Serial Programming Timing


ICD2051-5

Three-State Timing


ICD2051-6

Programmable Clock Generator
Features

- Clock outputs ranging from 391 kHz to 100 MHz (TTL levels) or 90 MHz (CMOS levels)
- 2-wire serial interface facilitates programmable output frequency
- Phase-Locked Loop oscillator input derived from external reference clock (1 MHz to 25 MHz) or External Crystal (2 MHz to 24 MHz)
- Three-State output control disables output for test purposes
- Sophisticated internal loop filter requires no external components or manufacturing tweaks as commonly required with external filters

- Low power consumption makes device ideal for power- and space-critical applications
- 8-pin 150-mil packaging achieves minimum footprint for space-critical applications
- 5V operation
- High-speed CMOS technology

Functional Description

The ICD2053B Programmable Clock Generator offers a fully user-programmable phase-locked loop in a single 8-pin package. The output may be changed "on the fly" to any desired frequency value between 391 kHz and 100 MHz (90 MHz at

CMOS levels). The ICD2053B is ideally suited for any design in which package size, power, and/or frequency programmability are important design issues.

The ability to dynamically change the output frequency adds a whole new degree of freedom for the designer. Some examples of the uses for this device include: laptop computers, in which slowing the speed of operation can mean less power consumption; graphics board dot clocks to allow dynamic synchronization of different brands of monitors or display formats; on-board test strategies where the ability to skew a system's desired frequency (e.g., $\pm 10\%$) allows worst-case evaluation.

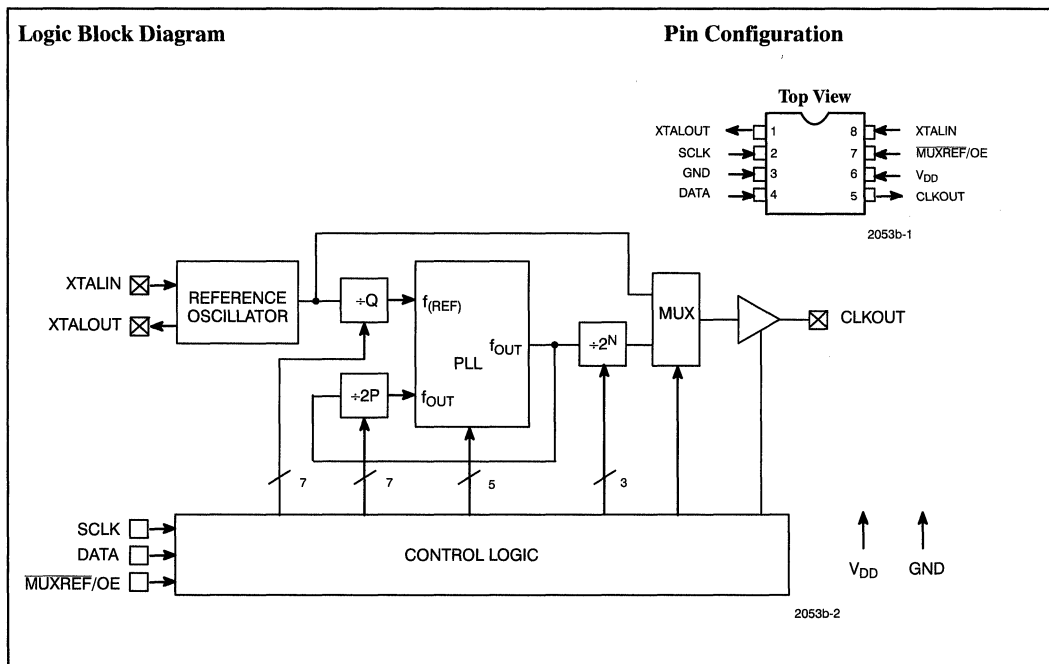


Table 1. Control Register

Bit	Definition
RESERVED	For future use. Set to 0.
Duty Cycle Adjust	Set to 1 to reduce duty cycle by approximately 0.7 ns. Normally set to 1.
Pin 7 Usage	Definition of whether pin 7 is MUXREF or OE input pin 0 = Pin 7 is OE input (default) 1 = Pin 7 is MUXREF input
MUXREF Control	Allows internal control of MUXREF. If enabled, this feature automatically multiplexes the reference frequency to the CLKOUT output. This is used to change output glitch-free to new frequencies. 0 = CLKOUT is VCO frequency (default) 1 = CLKOUT is $f_{(REF)}$
OE Control	Forces the CLKOUT output into a three-state mode 0 = CLKOUT is VCO frequency or $f_{(REF)}$ (default)(depending on current MUXREF state) 1 = CLKOUT is three-stated
Enable Program Word	Enable Program word loading into Program register. When enabled, the Program word may be shifted in. This permits changing the Control register without disturbing Program register data. 0 = Program register is disabled from loading (default) 1 = Program register is enabled to receive data

Program Register

The Program register can be loaded with a 22-bit programming word, the fields of which are defined in Table 2.

Table 2. Program Register

Field	# of Bits	Notes
P Counter value (P')	7	MSB (Most Significant Bits)
Duty Cycle Adjust Up (D)	1	Set to logic 1 to increase duty cycle by approx. 0.7 ns. Normally set to 1.
Mux (M)	3	
Q Counter value (Q')	7	
Index (I)	4	LSB (Least Significant Bits)

The VCO frequency, $f_{(VCO)}$, is determined by the following relation:

$$f_{(VCO)} = (2 * f_{(REF)} * P/Q)$$

$$\text{where } P' = P - 3$$

$$Q' = Q - 2$$

$$f_{(REF)} = \text{Reference frequency (1 MHz to 25 MHz)}$$

The value of $f_{(VCO)}$ must remain between 50 MHz and 150 MHz. Therefore, for output frequencies below 50 MHz, $f_{(VCO)}$ must be brought into range. To accomplish this, a post-VCO Divisor is selected by setting the values of the Mux field (M) as follows:

Mux Field (M)

M	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The index field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from Table 3. (Note that this table is referenced to the VCO frequency $f_{(VCO)}$ rather than to the desired output frequency and that only the MSB is significant.)

Table 3. Index Field (I)

I	$f_{(VCO)}$ @ 5V
0000	50 to 80 MHz
1000	80 to 150 MHz

To assist with these calculations, Cypress/IC Designs provides the BITCALC program. BITCALC is a Windows™ program for the IBM PC which automatically generates the appropriate programming word from the user's reference input and desired output frequencies.

VCO Programming Constraints

There are seven primary programming constraints the user must be aware of:

Table 4. Programming Constraints

Parameter	Minimum	Maximum
$f_{(REF)}$	1 MHz	25 MHz
$f_{(REF)}/Q$	200 kHz	1 MHz
$f_{(VCO)}$	50 MHz	150 MHz
divisor	1	128
f_{OUT}	50 MHz/128	100 MHz
Q	3	129
P	4	130

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability and factors affecting the loop equation. The factors are listed for completeness sake; however, by using the above-mentioned BITCALC program, these constraints become transparent.

Operating Conditions

Parameter	Description	Min.	Max.	Unit
V _{DD}	Supply Voltage	4.5	5.5	V
T _A	Ambient Operating Temperature	0	70	°C
C _L	Load Capacitance		25	pF

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V _{OH}	HIGH-level Output Voltage	I _{OH} = 4.0 mA	2.4		V
V _{OL}	LOW-level Output Voltage	I _{OL} = 4.0 mA		0.4	V
V _{IH}	HIGH-level Input Voltage	Except XTALIN pins	2.0		V
V _{IL}	LOW-level Input Voltage	Except XTALIN pins		0.8	V
V _{IH}	HIGH-level Reference Input Voltage, when DC coupled ^[4]	XTALIN pin only	V _{DD} -0.8		V
V _{IL}	LOW-level Reference Input Voltage, when DC coupled ^[4]	XTALIN pin only		0.8	V
I _{IH}	Input HIGH Current	V _{IN} = 5.0V, except SCLK		100	μA
I _{IL}	Input LOW Current	V _{IN} = 0.5V, except SCLK		-250	μA
I _{IH}	Input HIGH Current	V _{IN} = 5.0V, SCLK only		250	μA
I _{IL}	Input LOW Current	V _{IN} = 0.5V, SCLK only		-100	μA
I _{OZ}	Output Leakage Current	Three-state		10	μA
I _{DD}	Power Supply Current	V _{DD} =V _{DD} max., 100 MHz, V _{IN} =V _{DD} or 0V	13	50	mA

Capacitance

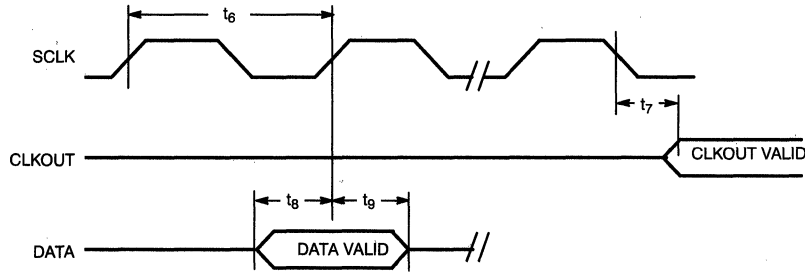
Parameter	Description	Max.	Unit
C _{IN}	Input Capacitance, except XTALIN pin	10	pF
C _{IN}	Input Capacitance, XTALIN pin	34	pF

Switching Characteristics Over the Operating Range

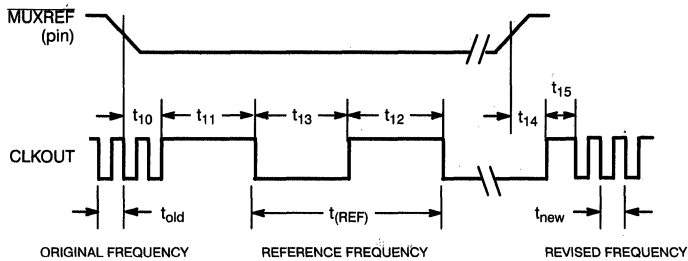
Parameter	Name	Description	Min.	Max.	Unit
f _(REF)	Reference Frequency	Reference Oscillator nominal value ^[4]	1	25	MHz
t _(REF)	Reference Clock Period	t _(REF) = 1/f _(REF)	40	1000	ns
t ₁	Reference Clock HIGH Time	Input pulse width HIGH for reference. Measured at V _{DD} /2, DC coupled. ^[4]	16		ns
t ₂	Output Period	CLKOUT period (frequency), TTL levels	10 (100 MHz)	2560 (391 kHz)	ns
		CLKOUT period (frequency), CMOS levels	11.1 (90 MHz)	2560 (391 kHz)	
t ₃	Output Duty Cycle (t ₀ /t ₂)	Duty cycle of CLKOUT measured at 1.4V (TTL) threshold	f _(OUT) < 50 MHz AND post-divide ≥ 2	45%	55%
			f _(OUT) > 50 MHz OR post-divide = 1	40%	60%
		Duty cycle of CLKOUT measured at V _{DD} /2 (CMOS) threshold	post-divide ≥ 2	45%	55%
			post-divide = 1	40%	60%
t ₄	Rise Time	Rise time for the clock output into a 25 pF load	TTL 0.4V to 2.4V		3
			CMOS, 0.1V _{DD} to 0.9V _{DD}		6

Note:

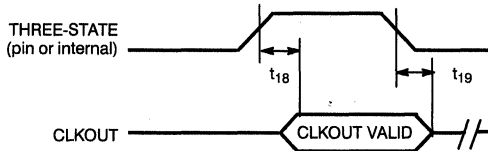
4. See *Externally Driven Crystal Oscillator* Application Note. For AC coupling, use an input duty cycle near 50%.

Switching Waveforms (continued)
Serial Programming Timing


2053b-4

MUXREF Timing^[7]


2053b-5

Three-State Timing


2053b-6

Ordering Information

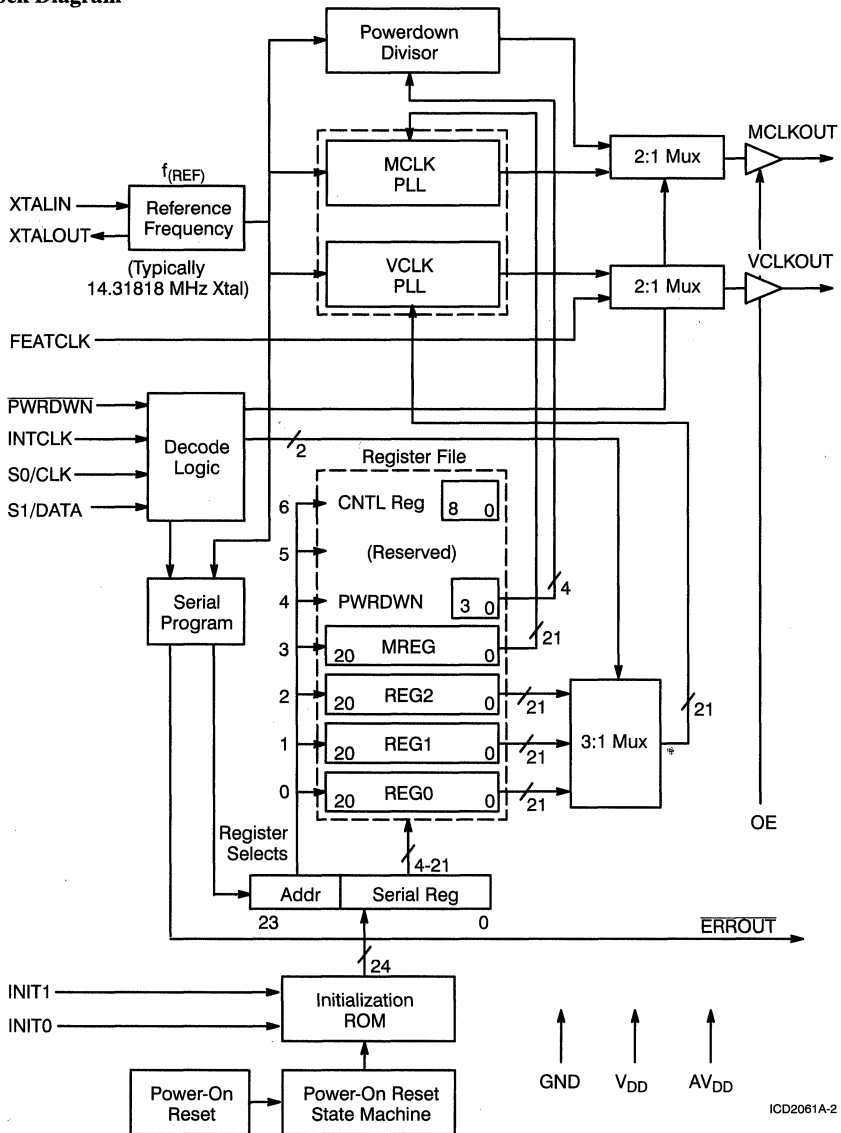
Ordering Code	Package Name	Package Type	Operating Range
ICD2053B	S8	8-Pin (150-Mil) SOIC	Commercial ^[8]

Notes:

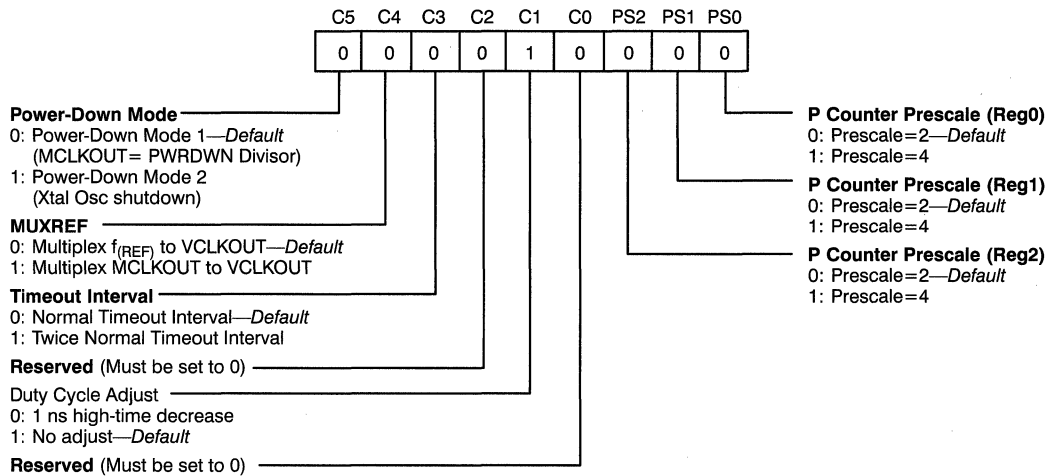
7. Identical behavior is exhibited when the internal MUXREF bit in the Control register is HIGH.
8. 0°C to +70°C

Document #: 38-00412

Windows is a trademark of Microsoft Corporation.

Logic Block Diagram


ICD2061A-2


Figure 1. Control Register Definition

ICD2061A-3

Register Selection

The Video Clock output is controlled not only by the S0 and S1 bits, but also by the PWRDWN and OE signals. Additionally, the clock synthesizer is multiplexed with an external frequency input (FEATCLK) which corresponds to the IBM VGA Feature Clock standard. *Table 3* shows the VCLKOUT selection criteria.

Table 3. VCLKOUT Selection

OE	PWRDWN	INTCLK	S1	S0	VCLKOUT
0	X	X	X	X	High-Z
1	0	X	X	X	Forced High
1	1	X	0	0	REG0
1	1	X	0	1	REG1
1	1	0	1	0	FEATCLK
1	1	1	1	X	REG2
1	1	X	1	1	REG2

The Memory Clock output is controlled by the PWRDWN and OE signals as indicated in *Table 4*.

Table 4. MCLKOUT Selection

OE	PWRDWN	MCLKOUT
0	X	High-Z
1	1	MREG
1	0	PWRDWN ^[3]

Note:

3. Power-Down Mode (1 or 2) is determined by the setting of bit C5 in the CNTL Reg. See *1. Control Register Definition*.

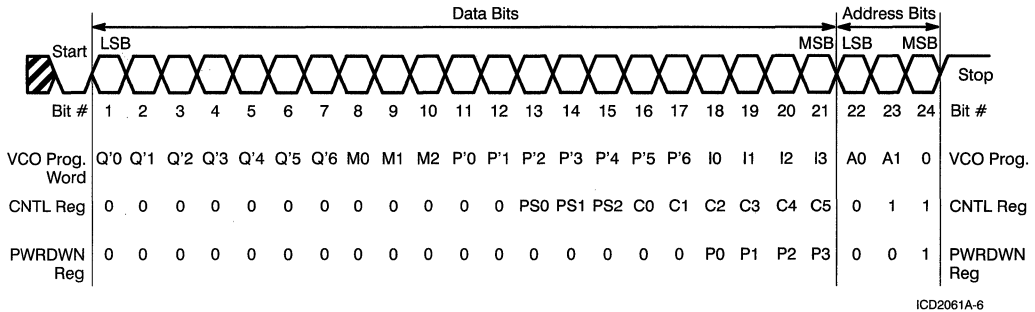
The Clock Select pins S0 and S1 have a dual purpose. When these pins are performing serial download, the VCLKOUT signal remains unchanged (unless the currently selected register is the one being programmed). When the pins S0 and S1 are functioning as register selects, a timeout interval is required to determine whether the user desires register select or serial programming. At the end of the timeout interval, new register selection occurs. At this point, the VCLKOUT signal will be multiplexed to the reference signal f_{REF} for an additional timeout interval to give the VCO time to settle to its new value. [The timeout interval in both cases is approximately 5 nsec—see the timeout interval spec in *Switching Characteristics*.]

When a new frequency is being set for MCLK, or if the active VCLK register is programmed, a glitch-free multiplexing to the Reference Frequency is performed. Once the STOP bit is sent after the MCLK or active VCLK Programming Word, the appropriate output signal will be multiplexed to the reference signal f_{REF} for an extra timeout interval (See *Switching Characteristics* for further details).

Control Register Definition

The Control Register (CNTL Reg) allows the user to adjust various internal options. Most of these options are for special cases, and should have no applicability to standard graphics usage. The register word is defined in *Figure 1*.

Duty Cycle Adjust—This control bit causes a 1 ns decrease in the output waveform high time. The default is no adjustment. In situations in which the capacitive load is beyond device specifications, or where the threshold voltage V_{TH} is to be changed from CMOS to TTL levels, this adjustment can sometimes bring the output closer to 50% duty cycle.


Figure 4. Serial Data Timing

2. The complement of the data bit must be sampled on the previous falling edge of CLK.
3. The Set-Up and Hold Time requirements must be met on both CLK edges.
4. The unlock sequence, start, and stop bits are not Manchester-encoded.

For specifics on timing, see the "Serial Programming Timing" section in the switching waveforms..

The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit (which also functions as a load strobe to transfer the data from the Serial Reg into the desired register). For the VCO registers (REG0, REG1, REG2, MREG), the data is made up of 4 fields: D[20:17] = Index; D[16:10]=P'; D[9:7]=Mux; D[6:0]=Q'. (See the *Programming the ICD2061A* section for more details on the VCO data word.) For the other registers with fewer than 21 bits (PWRDWN, CNTL Reg), the upper bits are used (starting with the MSB). A total of 24 bits must always be loaded into the Serial Data Register (or an error is issued). Undefined bits should always be set to zero to maintain software compatibility with future enhancements.

Following the entry of the last data bit, a stop bit or Load command is issued by bringing data HIGH and toggling CLK HIGH-to-LOW and LOW-to-HIGH. The unlocking mechanism then automatically rearms itself following the load. Only when the watchdog timer has timed out are the S0 and S1 selection pins permitted to return to their normal register select function.

Note that the Serial Data register (Serial Reg) that receives the address and data bits is exactly the correct length to accept the data being sent. The stop bit is used as a load command that passes the Serial Reg contents on to the register file location indicated by the address bits. If a stop bit is not received after the Serial Data register has been filled, but rather more valid encoded data is received, then all of the received serial data is ignored, the unlocking mechanism rearmed, and an error is issued. The device counts the serial data clock edges to know exactly when the serial buffer is full, and thus to know which bit is the stop bit. Following the stop bit, the unlocking mechanism rearms itself. If corrupt data is detected (i.e., incorrectly

Manchester-encoded data), then the unlocking mechanism is rearmed, the serial counter reset, all received data ignored, and **ERRROUT** is asserted.

ERRROUT Operation

The **ERRROUT** signal is used to report when a program error has been detected internally by the ICD2061A. The signal stays active until the next unlock sequence.

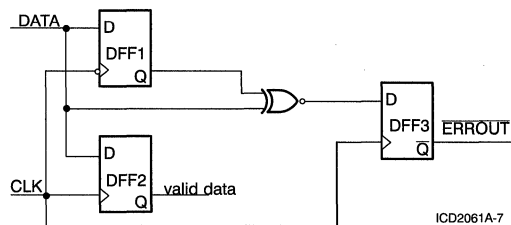
Figure 5 shows the basic mechanism used to detect valid and erroneous serial data. Note that the circuit must have different values on the rising and falling edge when sampling the falling edge first. Valid data is read on the rising edge of CLK.

The **ERRROUT** signal is invoked for any of the following error conditions: incorrect Manchester encoding; incorrect length of data word; incorrect stop bit; timeout.

Note that if there is no input pin available on the target VGA controller chip to monitor **ERRROUT**, a software routine which counts VSYNC pulses in order to measure output frequency may be used as a determination of programming accuracy.

Programming the ICD2061A

The desired output frequency is defined via a serial interface, with a 24-bit number shifted in. The ICD2061A has two programmable oscillators, requiring a 24-bit programming word (W) to be loaded into each channel's respective registers independently. This word contains 4 fields:


Figure 5. Serial Data Timing

Programming Example—Prescaling=2 (default)

The following is an example of the calculations *BitCalc* performs:

Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz < 50 MHz, double it to 79.0 MHz. Set D to 001. Set I to 1000. The result:

$$f_{(VCO)} = 79.0 = (2 \times 14.31818 \times P/Q)$$

$$P/Q = 2.7587$$

Table 9. P&Q Value Pairs

P	Q	f _(VCO) (MHz)	Error (PPM)
69	25	79.0363	460
80	29	78.9969	40
91	33	78.9669	419

Choose (P, Q)=(80,29) for best accuracy (40 PPM).

Therefore:

$$P' = P - 3 = 80 - 3 = 77 = 1001101 \text{ (4dH)}$$

$$Q' = Q - 2 = 29 - 2 = 27 = 0011011 \text{ (1bH)}$$

and the full programming word, W is:

$$W = I, P', M, Q' = 1000, 1001101, 001, 0011011$$

$$= 100010011010010011011 \text{ (11349bH)}$$

The programming word W is then sent as a serial bit stream, LSB first. Appropriate start and stop bits must also be included as defined in the Serial Programming Scheme section.

Programming Example—Prescaling=4

Assume the desired VCLKOUT frequency is 100 MHz. *Table 10* compares the results of using the default prescaling value of 2 and the optional prescaling value of 4.

Table 10. Prescale Values

Prescale	Actual Frequency (MHz)	P	Q	Error (PPM)
2	99.84028	129	37	1600
4	99.99998	110	63	0

But this precision has its price, namely that the user now has to set and reset the Prescale Bits PS0-2 (corresponding to REG0-2), which involves loading a Control Word (taking care to preserve the current values of the other Control Bits), before the VCO Program Word can be loaded. Once the appropriate Prescale Bits are set, then frequency programming can proceed as before, unless and until it is desired to program a new frequency without prescaling, at which point a new Control Word must first be loaded with the proper bits set, and observing the precautions noted above.

To summarize, the sequence is:

1. Set the Prescale bits (load a Control Word)
2. Program the VCO (load a Program Word)

Note that care must be taken not to change the Prescale Bit of the currently active register: the results will be unpredictable at best, and it could cause the VCO to go out of lock.

Power Management Issues
Power-Down Mode 1

The ICD2061A contains a mechanism to reduce the quiescent power when stand-by operation is desired. In Power-Down Mode 1 (invoked by pulling the PWRDWN signal low and having the proper CNIL Reg bit set to zero), both VCOs are shut down, the VCLKOUT output is forced high, and the MCLKOUT output is set to a user-defined low-frequency value to refresh dynamic RAM.

The power-down MCLKOUT value is determined by the following equation:

$$MCLKOUT_{\text{Power-Down}} = f_{(REF)} \div (\text{PWRDWN Reg Divisor Value})$$

The Power-Down register divisor is determined according to the following 4-bit word programmed into the PWRDWN register. (See *Table 11*.)

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Input Voltage -0.5V to $V_{DD} + 0.5V$
 Storage Temperature -65°C to +150°C
 Max soldering temperature (10 sec) 260°C

Junction temperature 125°C

Operating Range

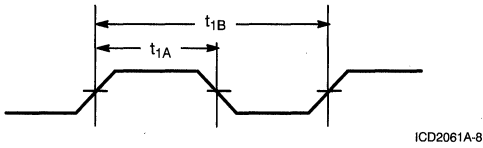
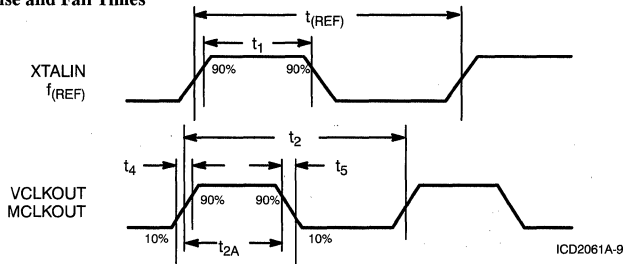
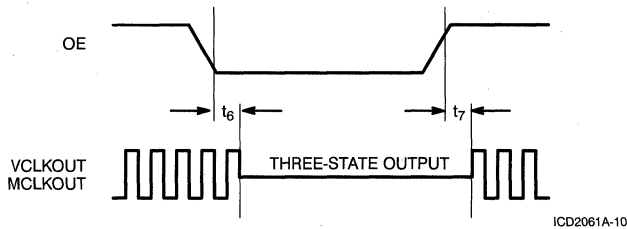
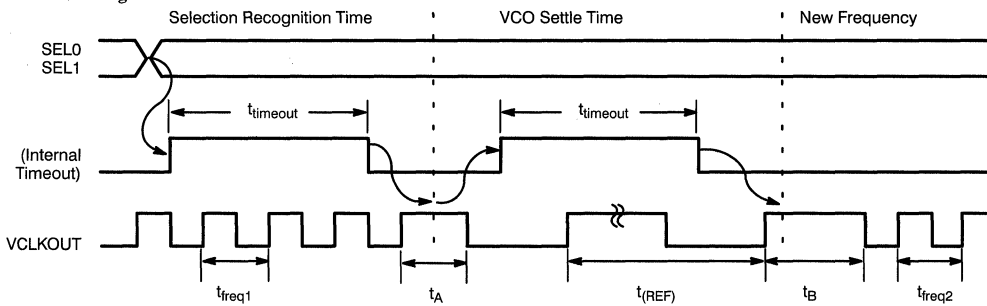
Ambient Temperature	V_{DD} & ΔV_{DD}
$0^{\circ}\text{C} \leq T_{\text{AMBIENT}} \leq 70^{\circ}\text{C}$	$5V \pm 5\%$

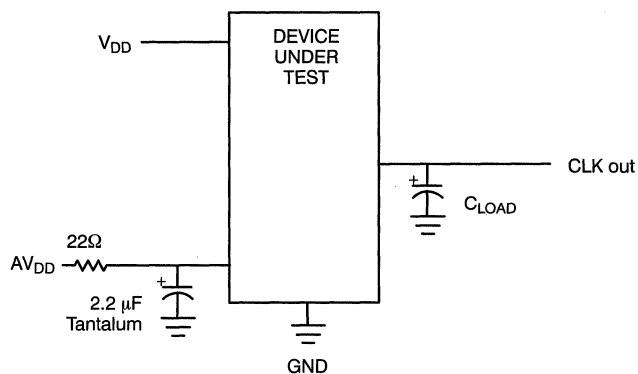
Electrical Characteristics Over the Operating Range^[6]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -4.0\text{mA}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 4.0\text{mA}$		0.4	V
V_{IH}	Input HIGH Voltage	Except on Crystal Pins	2.0		V
V_{IL}	Input LOW Voltage	Except on Crystal Pins		0.8	V
I_{IH}	Input HIGH Current	$V_{IH} = V_{DD} - 0.5$		105.0	μA
I_{IL}	Input LOW Current	$V_{IL} = +0.5V$		-250.0	μA
I_{OZ}	Output Leakage Current	(Three-state)		10	μA
I_{DD}	Supply Current	Inputs @ V_{DD} and GND	15	85.0	mA
I_{ADD}	Analog Power Supply Current			10	mA
I_{PD1}	Power-Down Current (Mode 1)			7.5	mA
I_{PD2}	Power-Down Current (Mode 2)			50	μA

Note:

6. Input capacitance is typically 10 pF, except for the crystal pins.

Switching Waveforms
Duty Cycle Timing

Rise and Fall Times

State Timing

Selection Timing


Test Circuit

Ordering Information^[10]

Ordering Code	Package Name	Package Type	Operating Range
ICD2061A	S1	16-Pin SOIC	Commercial ^[11]

Notes:

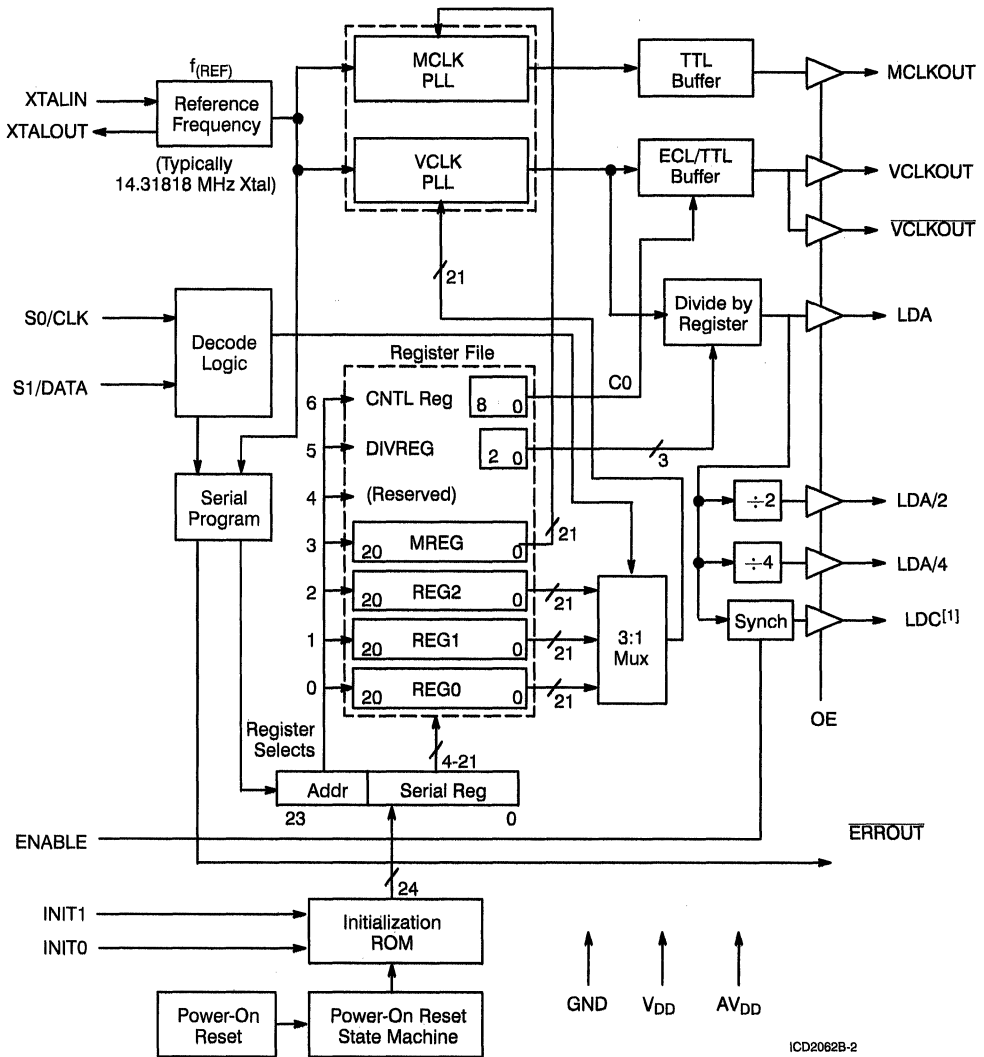
10. Please call your local Cypress representative.

11. 0°C to +70°C

Example: order ICD2061ASC-1 for the ICD2061A, 16-pin plastic SOIC, commercial temperature range device with the initial frequencies shown in *Table 2*.

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Logic Block Diagram

Note:

1. If ENABLE = 1, then LDC = synch. copy of LDA, else LDC = 0.

The Clock Select pins S0 and S1 have a dual purpose. When these pins are performing serial download, the VCLKOUT signal remains unchanged (unless the currently selected register is the one being programmed). When the pins S0 and S1 are functioning as register selects, a timeout interval is required to determine whether the user desires register select or serial programming. At the end of the timeout interval, new register selection occurs. At this point, the VCLKOUT signal will be multiplexed to the reference signal f_{REF} for an additional timeout interval to allow the VCO to settle to its new value. (The timeout interval in both cases is approximately 5 msec—see the timeout interval spec in *Switching Characteristics*.)

When a new frequency is being set for MCLK, or if the active VCLK register is being programmed, then a glitch-free multiplexing to the Reference Frequency is performed. Once the STOP bit is sent after the MCLK or active VCLK Programming Word, the appropriate output signal will be multiplexed to the reference signal f_{REF} for an extra timeout interval (See *Switching Characteristics* for further details).

Control Register Definition

The Control Register (CNTL Reg) allows the user to adjust various internal options. Most of these options are for special cases, and should have no applicability to standard graphics usage. The register word is defined in *Figure 1*.

MUXREF—This control bit determines which clock is multiplexed to the VCLKOUT output during frequency changes. While the VCLK VCO changes to a different frequency, a known clock is multiplexed to the output. The default is to multiplex the f_{REF} reference frequency, but some graphics controllers cannot run as slow as f_{REF} . This bit, when set, allows the MCLK to be used as an alternative frequency.

Timeout Interval—The timeout interval is normally defined as in the *Switching Characteristics*. It is derived from the MCLK VCO, and if this VCO is programmed to certain extremes, then the timeout may be too short. If this control bit is set, then the timeout interval is doubled.

RAMDAC Reset—This control bit, when set, will cause the ICD2062B to issue a RAMDAC reset sequence, which is

required by some specific RAMDACs (such as the Bt457/458). For more specifics on this operation, refer to the section *Internal RESET Sequence*. NOTE: This operation will only take place the first time this bit is set.

Duty Cycle Adjust—This control bit causes a 1 ns decrease in the output waveform high time. The default is no adjustment. In situations in which the capacitive load is beyond device specifications, or where the threshold voltage V_{TH} is to be changed from CMOS to TTL levels, this adjustment can sometimes bring the output closer to 50% duty cycle.

VCLKOUT Pad—This control bit determines whether the VCLKOUT Pad is at ECL or TTL levels. The default is ECL levels. When in TTL mode, the VCLKOUT Pad is nonfunctional, and remains three-stated.

P Counter Prescale (REG0, REG1, REG2)—These control bits determine whether or not to prescale the P Counter value, which allows fine tuning the output frequency of the respective register. Prescaling is explained in more detail later in this datasheet.

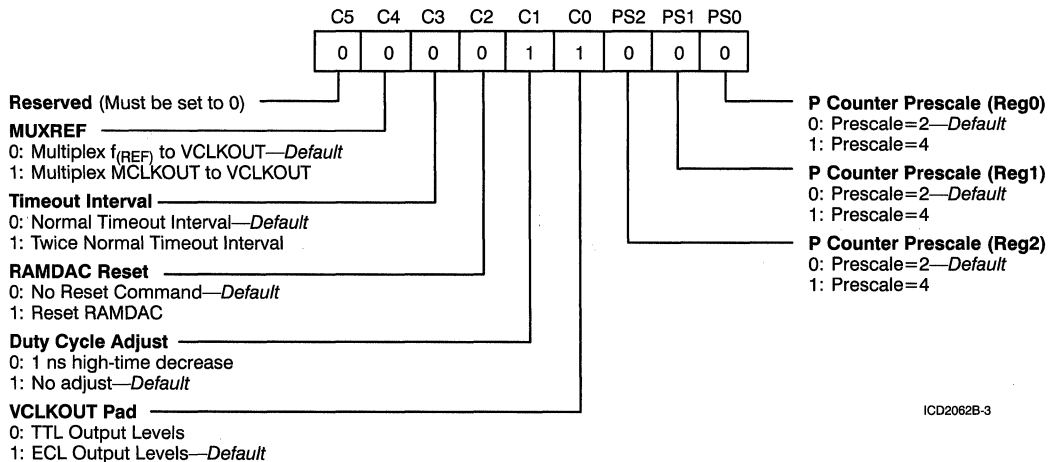
Divide Register Definition

The output signals LDA, LDA/2, LDA/4, and LDC are all a function of the VCLK VCO value divided by the division factor stored in the Divide Register (DIVREG). The maximum LDA and LDC output is 100 MHz.

Table 4. DIVREG Division Factors

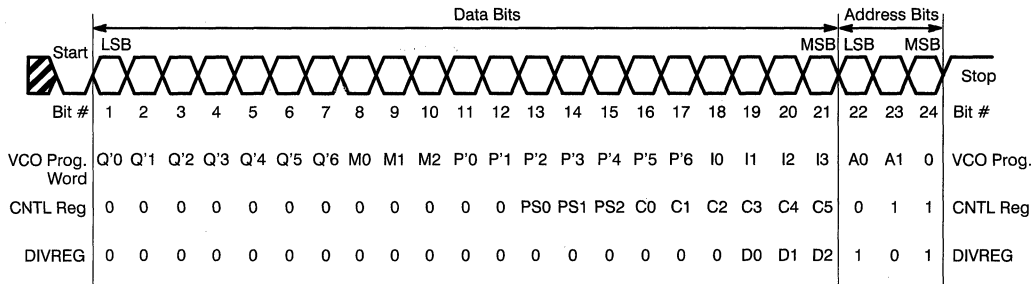
D2	D1	D0	Division Factor	Clock LOW (cycles)	Clock HIGH (cycles)	Device Version
1	0	X	÷1	1/2	1/2	A&B
1	1	X	÷2	1	1	A&B
0	0	0	÷3	1	2	B
0	0	1	÷4	2	2	B ^[3]
0	1	0	÷5	2	3	B
0	1	1	÷8	4	4	B

Note:
3. Default on power-up.



ICD2062B-3

Figure 1. Control Register Definition


Figure 4. Serial Data Timing

ICD2062B-6

3. The Set-Up and Hold Time requirements must be met on both CLK edges.
4. The unlock sequence, start, and stop bits are not Manchester-encoded.

For specifics on timing, see the “Serial Programming Timing” section in the switching waveforms.

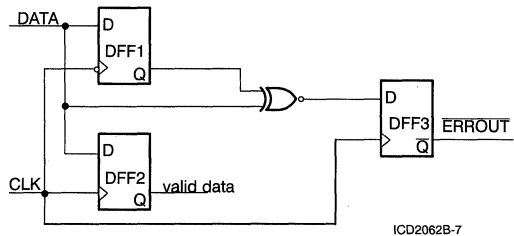
The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit (which also functions as a load strobe to transfer the data from the Serial Reg into the desired register). For the VCO registers (REG0, REG1, REG2, MREG), the data is made up of 4 fields: D[20:17] = Index; D[16:10]=P'; D[9:7]=Mux; D[6:0]=Q'. (See the *Programming the ICD2062B* section for more details on the VCO data word.) For the other registers with fewer than 21 bits (DIVREG, CNTL Reg), the upper bits are used (starting with the MSB). A total of 24 bits must always be loaded into the Serial Data register (or an error is issued). Undefined bits should always be set to zero to maintain software compatibility with future enhancements.

Following the entry of the last data bit, a stop bit or Load command is issued by bringing DATA HIGH and toggling CLK HIGH-to-LOW and LOW-to-HIGH. The unlocking mechanism then automatically rearms itself following the load. Only when the watchdog timer has timed out are the S0 and S1 selection pins permitted to return to their normal register select function.

Note that the Serial Data register that receives the address and data bits is exactly the correct length to accept the data being sent. The stop bit is used as a load command that passes the Serial Data Reg contents on to the register file location indicated by the address bits. If a stop bit is not received after the Serial Data register has been filled, but rather more valid encoded data is received, then all of the received serial data is ignored, the unlocking mechanism rearmed, and an error is issued. The device counts the serial data clock edges to know exactly when the serial buffer is full, and thus to know which bit is the stop bit. Following the stop bit, the unlocking mechanism rearms itself. If corrupt data is detected (i.e., incorrectly Manchester-encoded data), then the unlocking mechanism is rearmed, the serial counter reset, all received data ignored, and ERRROUT is asserted.

ERRROUT Operation

The ERRROUT signal is used to announce when a program error has been detected internally by the ICD2062B. The signal remains LOW until the next unlock sequence.


Figure 5. Modified Manchester Decoder Circuit

ICD2062B-7

Figure 5 shows the basic mechanism used to detect erroneous serial data. Note that the circuit must have different values on the rising and falling edge when sampling the falling edge first. Valid data is read on the rising edge of CLK.

The ERRROUT signal is invoked for any of the following error conditions: incorrect start bit, incorrect Manchester encoding; incorrect length of data word; incorrect stop bit.

Note that if there is no input pin available on the target VGA controller chip to monitor ERRROUT, a software routine which counts VSYNC pulses in order to measure output frequency may be used as a determination of programming success.

Programming the ICD2062B

The desired output frequency is defined via a serial interface, with a 21-bit number shifted in. The ICD2062B has two programmable oscillators, requiring a 21-bit programming word (W) to be loaded into each channel's respective registers independently. This word contains 4 fields, as shown in Table 6.

Table 6. Programming Word Bit Fields

Field	# of bits	Notes
Index (I)	4	MSB (Most Significant Bits)
P Counter value (P')	7	
Mux (M)	3	
Q Counter value (Q')	7	LSB (Least Significant Bits)

Table 10. P&Q Value Pairs

P	Q	f _(VCO) (MHz)	Error (PPM)
69	25	79.0363	460
80	29	78.9969	40
91	33	78.9669	419

Choose (P, Q)=(80,29) for best accuracy (40 PPM).

Therefore:

$$P' = P - 3 = 80 - 3 = 77 = 1001101 \text{ (4dH)}$$

$$Q' = Q - 2 = 29 - 2 = 27 = 00111011 \text{ (1bH)}$$

and the full programming word, W is obtained by concatenating:

$$I = 0010, P' = 1001101, M = 001, Q' = 0011011$$

$$= 001010011010011011 \text{ (05349bH)}$$

The programming word W is then sent as a serial bit stream, LSB first. Appropriate start and stop bits must also be included as defined in the Serial Programming Architecture section.

Programming Example—Prescaling=4

Assume the desired VCLKOUT frequency is 100 MHz. *Table 10* compares the results of using the default prescaling value of 2 and the optional prescaling value of 4.

Table 11. Prescale Values

Prescale	Actual Frequency (MHz)	P	Q	Error (PPM)
2	99.84028	129	37	1600
4	99.99998	110	63	0

But this precision has its price, namely that the user now has to set and reset the Prescale Bits PS0–2 (corresponding to REG0–2), which involves loading a Control Word (taking care to preserve the current values of the other Control Bits), before the VCO Program Word can be loaded. Once the appropriate

Prescale Bits are set, then frequency programming can proceed as before, unless and until it is desired to program a new frequency without prescaling, at which point a new Control Word must first be loaded with the proper bits set, and observing the precautions noted above.

To summarize, the sequence is:

1. Set the Prescale bits (load a Control Word)
2. Program the VCO (load a Program Word)

Note that care must be taken not to change the Prescale Bit of the currently active register: The results will be unpredictable at best, and it could cause the VCO to go out of lock.

RAMDAC/VRAM Interface

Interfacing to the RAMDAC

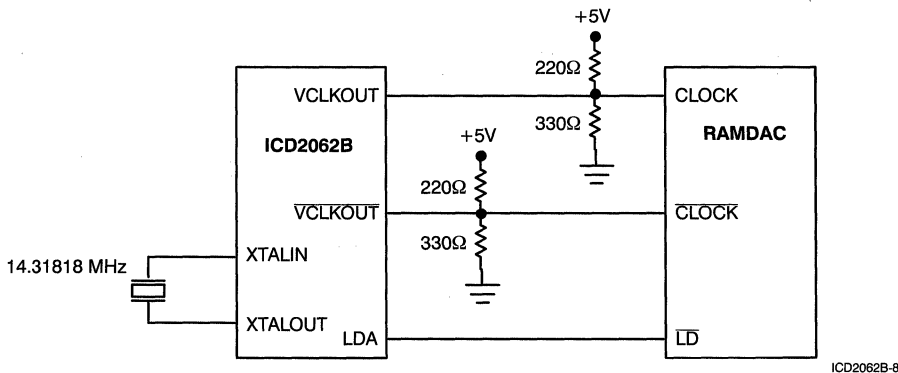
Figure 6 shows how to interface the ICD2062B to a RAMDAC. The part should be located as close to the RAMDAC as possible. Termination resistors are needed on the VCLKOUT outputs, and should be located as close as possible to the RAMDAC. For specific information, please refer to the Cypress/IC Designs application note *ECL Outputs*.

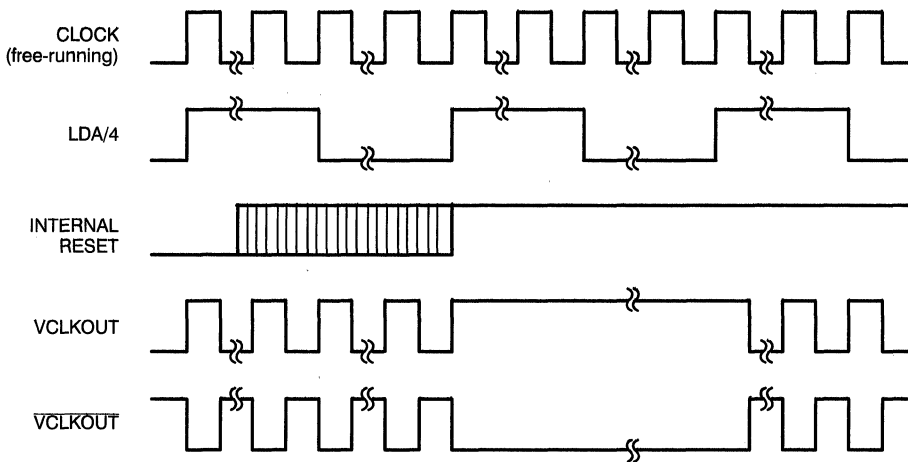
The ICD2062B may drive the CLOCK inputs of up to four RAMDACs, if they are located physically adjacent to each other. In this case, only 2 sets of termination resistors should be used, and these should be located closest to the farthest RAMDAC from the ICD2062B.

Typical ICD2062B Usage

The DIVREG register holds the divisor, which can be 1, 2, 3, 4, 5, or 8, by which the pixel clock is divided to generate the load signals: LDA, LDA/2, and LDA/4.

The ENABLE input is synchronized internally to LDA; it may be used to start and stop the LDC output synchronously. When ENABLE is LOW, LDC is held LOW. When ENABLE is HIGH, then LDC will be free-running and in phase with LDA. This allows the video DRAM shift registers to be non-clocked during the retrace intervals. Note that for fanouts greater than 4, LDC needs to be buffered.


Figure 6. ICD2062B to RAMDAC Interface Example



ICD2062B-11

Figure 9. Internal RESET Timing

Power Management Issues

Estimating Total Current Drain

Actual current drain is a function of frequency and of circuit loading. The operating current of a given output is given by the equation: $I = C \cdot V \cdot f$, where

I = current,

C = load capacitance (max. 25 pF),

V = output voltage (usually 5V for TTL pads, 1.5V for ECL pads),

f = output frequency (in MHz).

To calculate total operating current, sum the following:

- MCLKOUT $\Rightarrow C \cdot V \cdot f_{(MCLKOUT)}$
- VCLKOUT $\Rightarrow C \cdot V \cdot f_{(VCLKOUT)}$; (ECL pad, $V=1.5V$)
- VCLKOUT $\Rightarrow C \cdot V \cdot f_{(VCLKOUT)}$; (ECL pad, $V=1.5V$)
- LDA $\Rightarrow C \cdot V \cdot f_{(LDA)}$
- LDA/2 $\Rightarrow C \cdot V \cdot f_{(LDA/2)}$
- LDA/4 $\Rightarrow C \cdot V \cdot f_{(LDA/4)}$
- LDC $\Rightarrow C \cdot V \cdot f_{(LDC)}$
- Internal $\Rightarrow 12 \text{ mA}$

This gives an approximation of the actual operating current. For unconnected output pins, one can assume 5 to 10 pF loading, depending on package type.

Table 12. Typical Values

Frequency	Capacitive Load	Current (mA)
LOW	LOW	15
HIGH	LOW	50
HIGH	HIGH	100

Output Enable Pin

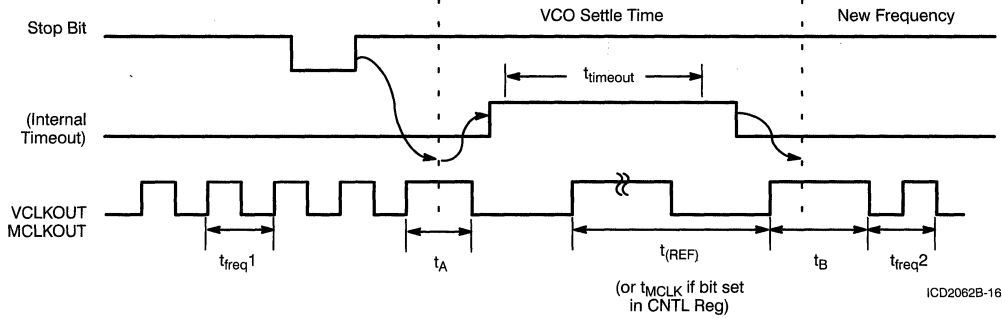
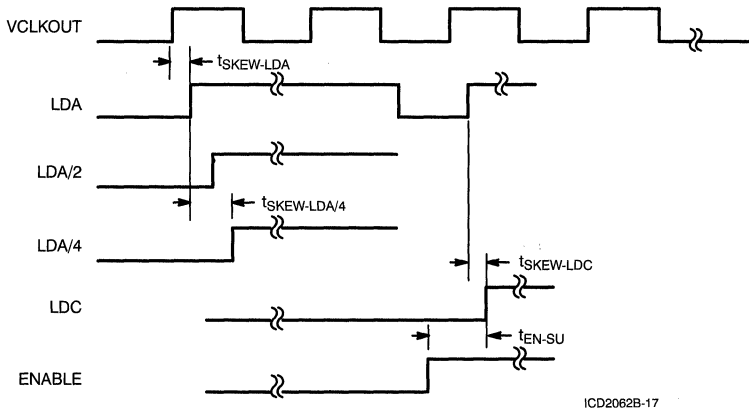
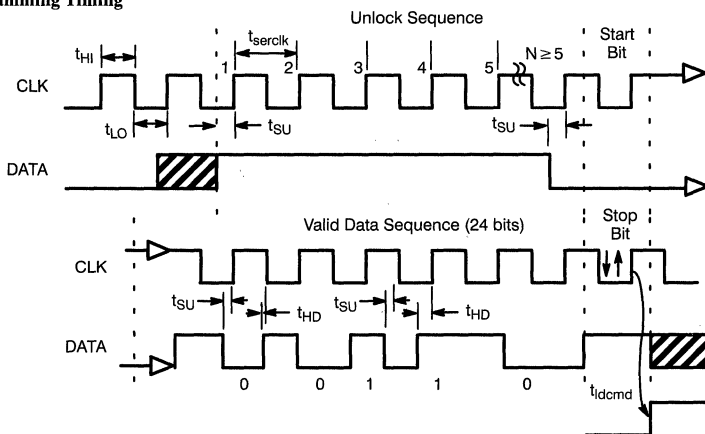
When the OE pin is asserted (active HIGH), all the output pins except XTALOUT and ERRROUT enter a high-impedance mode, to support automated board testing.

Switching Characteristics Over the Operating Range

Parameter	Name	Description	Min.	Typ.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference Oscillator nominal value (Note: for references of other than 14.318 MHz, the pre-loaded ROM frequencies will not be accurate.)	1	14.318	25	MHz
$t_{(REF)}$	Reference Clock Period	$1 \div f_{(REF)}$	40		1000	ns
t_1	Input Duty Cycle	Duty cycle for the inputs defined as $t_{1A} \div t_{1B}$	25%	50%	75%	
t_2	Output Clock Periods	Output values	ECL	6.1 165 MHz	1970 508 kHz	ns
			TTL	8.3 120 MHz	1970 508 kHz	
t_3	Output Duty Cycle	Duty cycle for the outputs ^[7]	40%		60%	
t_4	Rise Times	Rise time for the outputs into a 25-pF load			4	ns
t_5	Fall Times	Fall time for the outputs into a 25-pF load			4	ns
$t_{skew-ECL}$		Skew between the VCLKOUT complementary outputs			1	ns
t_{freq1}	freq1 Output	Old frequency output				
t_{freq2}	freq2 Output	New frequency output				
t_A	$f_{(REF)}$ Mux Time	Time clock output remains HIGH while output muxes to reference frequency	$t_{(REF)}/2$		$3(t_{(REF)}/2)$	ns
$t_{timeout}$	Timeout Interval	Internal interval for serial programming and for VCO changes to settle ^[8]	2	5	10	msec
t_B	t_{freq2} Mux Time	Time clock output remains HIGH while output muxes to new frequency value	$t_{freq2}/2$		$3/(t_{freq2}/2)$	ns
t_6	Three-state	Time for the outputs to go into three-state mode after OE signal assertion	0		12	ns
t_7	CLK Valid	Time for the outputs to recover from three-state mode after OE signal goes HIGH	0		12	ns
t_{LD}	Load Clock Period	Maximum LDA and LDC period	10			ns
$t_{SKEW-LDA}$		VCLKOUT to LDA output skew	2		6	ns
$t_{SKEW-LDA/2}$		LDA to LDA/2 output skew	0	1	2	ns
$t_{SKEW-LDA/4}$		LDA to LDA/4 output skew	0	1	2	ns
$t_{SKEW-LDC}$		LDA to LDC output skew	0	1	2	ns
t_{EN-SU}		ENABLE set-up time to LDA	12			ns
t_{EN-HD}		ENABLE hold time to LDA	0			ns
t_{serclk}		Clock period of serial clock	$2 \times t_{(REF)}$		2	msec
t_{HI}		Minimum HIGH time of serial clock	$t_{(REF)}$			ns
t_{LO}		Minimum LOW time of serial clock	$t_{(REF)}$			ns
t_{SU}		Set-Up time	20			ns
t_{HD}		Hold time	10			ns
t_{ldcmd}		Load command	0		$t_1 + 30$	ns

Notes:

- For non-ECL outputs, duty cycle is measured at CMOS threshold levels. At 5V, $V_{TH}=2.5V$.
- If the interval is too short, see the Timeout Interval section in the Control register definition.

Switching Waveforms (continued)
MCLK and Active VCLK Register Programming Timing

RAMDAC/VRAM Interface Timing

Serial Programming Timing


Programmable Graphics Clock Generator

Features

- **Second generation dual PLL graphics clock generator**
- **Compatible with the ICD2061A**
- **2 independent clock outputs:**
 - **VCLK Output**—390 kHz – 135 MHz (100 MHz at 3.3V)
 - **MCLK Output**—312 kHz – 100 MHz (80 MHz at 3.3V)
- **Individually programmable PLLs using a highly reliable, Manchester-encoded, 21-bit serial data word**
- **2-pin serial programming interface allows direct connection to most graphics chip sets with no external hardware required**
- **2 advanced power-down capabilities**
- **Three-state oscillator control disables outputs for test purposes**
- **Phase-locked loop oscillator input derived from single 14.318 MHz crystal**
- **3.3V and 5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 16-pin SOIC package configuration**

Functional Description

The ICD2063 Dual Programmable Graphics Clock Generator features a fully programmable set of clock oscillators which can handle all frequency requirements of most graphics systems. The ICD2063 offers the selection ease of ROM-based clock chips and the versatility of serially programmable frequency

synthesizers. It features both 3.3V and 5V operation with advanced power-down capabilities, making it ideally suited for the portable computer market.

The ICD2063 Dual Programmable Graphics Clock Generator offers two fully user-programmable phase-locked loops in a single package. The outputs may be changed “on the fly” to any desired frequency value between limits which depend on selected modes and operating voltage. The ICD2063 is ideally suited for any design where multiple or varying frequencies are required, replacing more expensive metal can oscillators or less functional ROM-based clock synthesizers.

While primarily designed for the graphics subsystem market, the programming versatility of the ICD2063 makes it ideal wherever two variable, yet highly accurate clock sources are required.

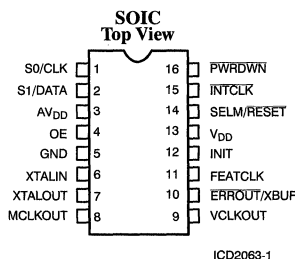
ICD2063 Changes from the ICD2061A

The ICD2063 revision of the ICD2061A is a complete mask redesign which includes many feature enhancements. The following major modifications have been implemented:

- **3.3V Operation**—The ICD2063 supports 3.3V operation in addition to 5V operation.
- **Expanded Register Set**—There are now 4 Video registers and 2 Memory registers. This allows better support for Windows NT drivers.
- **Expanded VCO Range**—The upper frequency limit has been increased to 135 MHz.

- **No Index Field Required**—The Serial Word now treats the Index Field (Mode Field) as a “Don’t Care” bit region, for complete software compatibility with the ICD2061A.
- **Buffered Crystal Output (Optional)**—XBUF Output may be specified, replacing the ERR0UT signal.
- **Smooth Frequency Transition**—The two phase-locked loops now transition smoothly from one frequency to another.
- **No MUXREF Required**—The necessity for the MUXREF procedure has been eliminated by the smooth frequency transition. For compatibility with the ICD2061A, there is an option which multiplexes a known output during frequency transitions. New to the ICD2063 is that the VCLK VCO is multiplexed to the MCLK output. See the *MUXREF Option* section for details.
- **Very High Frequency Resolution**—The MCLK Phase-Locked Loop Output can be multiplexed to the VCLK PLL Reference Input, thus enabling very high frequency resolution, at the expense of slightly higher jitter. See the *Extended VCLK Frequency Precision* section.
- **Reduced Register Initialization ROM**—The former INIT2 pin now selects between the 2 memory registers MREG0 and MREG1.
- **Hardware Reset (Optional)**—A hardware reset is available as an option, replacing the memory selection signal.

Pin Configuration



Pin Summary

Name	Number	Description
S0/CLK	1	Bit 0 (LSB) of frequency select logic, used to select PLL frequencies. Clock Input in serial programming mode. (Internal pull-down allows no-connect.)
S1/DATA	2	Bit 1 (MSB) of frequency select logic, used to select PLL frequencies. Data Input in serial programming mode. (Internal pull-down allows no-connect.)
AV _{DD}	3	+5V or 3.3V to Analog Core
OE	4	Output Enable. Three-states output when pulled LOW. (Internal pull-up allows no connect.)
GND	5	Ground
XTALIN ^[1]	6	Reference Oscillator input for all phase-locked loops (nominally from a parallel-resonant 14.31818 MHz crystal). Optionally PC System Bus Clock.
XTALOUT ^[1]	7	Oscillator Output to a reference crystal. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.)
MCLKOUT	8	Memory Clock output
VCLKOUT	9	Video Clock output
ERR _{OUT} / XBUF	10	Error Output: a LOW signals an error during serial programming –OR– Buffered Crystal Reference Output (selectable via configuration option)
FEATCLK	11	External clock input (Feature Clock) (Internal pull-up allows no-connect.)
INIT	12	Selects state of initialization ROM during power-up. See Table 2. (This pin has no internal pull-up or pull-down; it <i>must</i> be tied HIGH or LOW externally.)
V _{DD}	13	+5V or 3.3V to I/O Ring
SELM/RESET	14	Selectable via configuration option: SELM—Selects 1 of 2 Memory Clock Output (MCLKOUT) frequencies (see Register Selection subsection <i>MCLKOUT</i>) RESET—Hardware RESET control signal (see the <i>Power-On Reset, RESET, and Register Initialization</i> section)
INTCLK	15	Selects the Feature Clock external clock input as VCLKOUT output (Internal pull-up allows no-connect.) (See Table 3.)
PWRDWN	16	Power-down pin (active LOW) (Internal pull-up allows no-connect if power-down operation not required. See <i>Power Management Issues</i> for specific details concerning the use of this pin.)

Register Definitions
Register File

The Register File consists of the following registers and their respective addresses in the Serial Data register:

Table 1. Register Addressing^[2]

A2	A1	A0	Register	Usage
0	0	0	25.175 MHz	Fixed Video Clock Frequency
0	0	1	28.322 MHz	Fixed Video Clock Frequency
0	1	0	VREG0	Programmable Video Clock Register 0
0	1	1	MREG0	Programmable Memory Clock Register 0
1	0	0	PWRDWN	Divisor for Power-Down mode
1	0	1	VREG1	Programmable Video Clock Register 1
1	1	0	CNTL	Control Register
1	1	1	MREG1	Programmable Memory Clock Register 1

Notes:

- For best accuracy, use a parallel-resonant crystal, assume C_{LOAD}=17 pF.
- All register values are preserved in power-down mode.

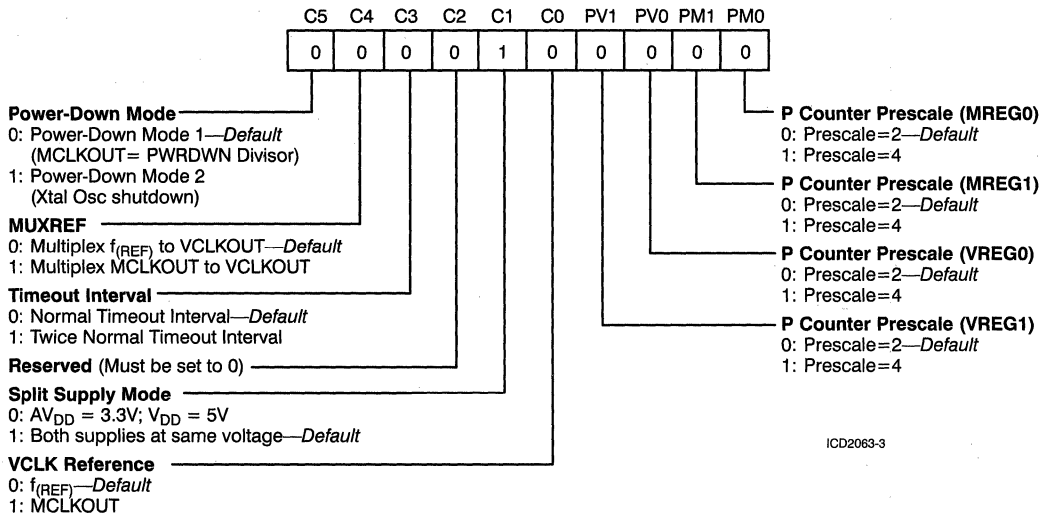


Figure 1. Control Register Definition

Control Register Definition

The Control Register (CNTL) allows the user to adjust various internal options. Most of these options are for special cases, and should have no applicability to standard graphics usage. The register word is defined in *Figure 1*.

VCLK Reference—This control bit determines whether the VCLK VCO uses $f_{(REF)}$ or the MCLK output as a reference. Refer to the *Extended VCLK Frequency Precision* section for more details.

Split Supply Mode—This control bit allows mixing 3.3V (AV_{DD}) and 5V (V_{DD}) supplies. The default is for both to be the same (5V or 3.3V). The alternative is $AV_{DD} = 3.3V$, $V_{DD} = 5V$. See the *3.3 Volt and 5 Volt Issues* section for more details. The purpose is to maintain duty cycle 50%.

Timeout Interval—The timeout interval is normally defined as in the *Switching Characteristics*. It is derived from the MCLK VCO, and if this VCO is programmed to certain extremes, then the timeout may be too short. If this control bit is set, then the timeout interval is doubled.

MUXREF (MUXREF Mode only)—This control bit determines which clock is multiplexed to the VCLKOUT output during frequency changes. While the VCLK VCO changes to a different frequency, a known clock is multiplexed to the output. The default is to multiplex the $f_{(REF)}$ reference frequency, but some graphic controllers cannot run as slow as $f_{(REF)}$. This bit, when set, allows the MCLK to be used as an alternative frequency.

Power-Down Mode—This control bit determines which Power-Down Mode the PWRDWN pin will implement. The default (Power-Down Mode 1) forces the MCLKOUT signal to be a function of the PWRDWN register. Power-Down Mode 2 turns off the crystal oscillator and disables all outputs. There is a more detailed description in the section entitled *Power Management Issues*.

P Counter Prescale (VREG0, VREG1, MREG0, MREG1)—These control bits determine whether or not to prescale the P

Counter value, which allows fine tuning the output frequency of the respective register. Prescaling is explained in more detail in the *Prescaling* section.

Serial Programming Architecture

The ICD2063 programming scheme is simple, yet impenetrable to accidental access. Because the only common denominator between most VGA and 8514 controllers is a few clock select pins, these have to perform the dual functions of clock selection and serial programming. The Serial Program Block (See ICD2063 Logic Block Diagram) contains several components: a Serial Unlock Decoder (containing the unlocking mechanism and Manchester decoder), a watchdog timer, the Serial Data register and a Demultiplexer to the Register File (see *Figure 2*).

Unlocking Mechanism

The Unlocking Mechanism watches for an initial break sequence, detailed in *Figure 3*.

The initial unlock sequence consists of at least five LOW-to-HIGH transitions of CLK with DATA HIGH, followed immediately by a single LOW-to-HIGH transition of CLK with DATA LOW. Following this unlock sequence, the encoded serial data is clocked into the Serial Data register.

Note that the ICD2063 may not be serially programmed when in Power-Down Mode.

Watchdog Timer

Following any transition of CLK or DATA, the watchdog timer is reset and begins counting. Throughout the entire programming process, the watchdog timer ensures that there is a transition on CLK or DATA within the timeout specification (of 2 msec—see *Switching Characteristics*.) If a timeout does occur, the lock mechanism is rearmed and the current data in the Serial Data register is ignored.

Since the VCLK registers are selected by the S0 or S1 bits, and since any change in their state may affect the resultant output frequency, new data input on the Selection Bits is only permitted

issued). Undefined bits should always be set to zero to maintain software compatibility with future enhancements.

Following the entry of the last data bit, a stop bit or Load command is issued by bringing data HIGH and toggling CLK HIGH-to-LOW and LOW-to-HIGH. The unlocking mechanism then automatically rearms itself following the load. Only when the watchdog timer has timed out are the S0 and S1 selection pins permitted to return to their normal register select function.

Note that the Serial Data register that receives the address and data bits is exactly the correct length to accept the data being sent. The stop bit is used as a load command that passes the Serial Data register contents on to the register file location indicated by the address bits. If a stop bit is not received after the Serial Data register has been filled, but rather more valid encoded data is received, then all of the received serial data is ignored, the unlocking mechanism rearmed, and an error is issued. The device counts the serial data clock edges to know exactly when the serial buffer is full, and thus to know which bit is the stop bit. Following the stop bit, the unlocking mechanism rearms itself. If corrupt data is detected (i.e., incorrectly Manchester-encoded data), then the unlocking mechanism is rearmed, the serial counter reset, all received data ignored, and **ERROUT** is asserted.

ERROUT Operation

The **ERROUT** signal is used to report when a program error has been detected internally by the ICD2063. The signal stays active until the next unlock sequence.

Figure 5 shows the basic mechanism used to detect valid and erroneous serial data. Note that the circuit must have different values on the rising and falling edge when sampling the falling edge first. Valid data is read on the rising edge of CLK.

The **ERROUT** signal is invoked for any of the following error conditions: incorrect start bit, incorrect Manchester encoding; incorrect length of data word; incorrect stop bit; timeout.

Note that if there is no input pin available on the target VGA controller chip to monitor **ERROUT**, a software routine which counts VSYNC pulses in order to measure output frequency may be used as a determination of programming accuracy.

Note also that the **ERROUT** signal is an order option. If the XBUF option is chosen instead, then **ERROUT** is not available, and the user may want to implement the above technique to verify that the desired programming did indeed take place.

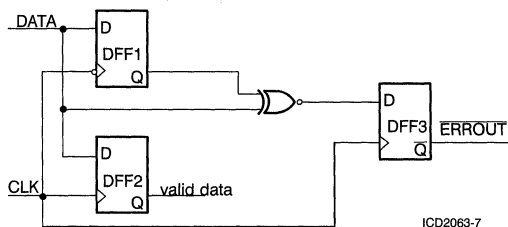


Figure 5. Serial Data Timing

Programming the ICD2063

The desired output frequency is defined via a serial interface, with a 21-bit number shifted in. The ICD2063 has two programmable oscillators, requiring a 21-bit programming word (W) to be loaded into each channel's respective registers independently. This word contains 4 fields:

Table 6. Programming Word Bit Fields

Field	# of bits	Notes
Mode (I)	4	MSB (Most Significant Bits)
P Counter value (P')	7	
Post-VCO Divisor (M)	3	
Q Counter value (Q')	7	LSB (Least Significant Bits)

The frequency of the Programmable Oscillator $f_{(VCO)}$ is determined by these fields as follows:

$$P' = P - 3$$

$$Q' = Q - 2$$

$$f_{(VCO)} = (\text{Prescale} \times f_{(REF)} \times P/Q)$$

where $f_{(REF)}$ = Reference frequency (between 1 MHz – 60 MHz; typically 14.31818 MHz) and Prescale = 2 or 4 (default is 2, defined by CNTL Reg).

Note that if a reference frequency other than 14.31818 MHz is used, then the initially loaded ROM frequencies will not be correct.

Table 7 lists the various limits for $f_{(VCO)}$.

Table 7. VCO Frequency Ranges

	5 Volt Operation	3.3 Volt Operation
VCLK PLL	50 MHz – 135 MHz	50 MHz – 100 MHz
MCLK PLL	40 MHz – 100 MHz	40 MHz – 80 MHz

For lower output frequencies, $f_{(VCO)}$ must be brought into range. To accomplish this, a post-VCO divisor is selected by setting the values of the Post-VCO Divider field (M). See Table 8.

Table 8. Post-VCO Divider (M)

M	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The Mode Field (I), formerly the Index Field, is included for historical reasons to preserve software compatibility with the ICD2061A. In the ICD2063, it is only used for a few special circumstances, as detailed in the following paragraphs.

Table 12. Effects of Prescaling

Prescale	Desired Freq. (MHz)	Actual Freq. (MHz)	P	Q	Error (PPM)
2	100	99.84028	129	37	1600
4	100	99.99998	110	63	0

But this precision has its price, namely that the user now has to set and reset the Prescale Bits PS0–2 (corresponding to REG0–2), which involves loading a Control Word (taking care to preserve the current values of the other Control Bits), before the VCO Program Word can be loaded. Once the appropriate Prescale Bits are set, then frequency programming can proceed as before. However, if it is desired to program a new frequency without prescaling, a new Control Word must first be loaded with the proper bits set, with the precautions noted above.

To summarize, the sequence is:

1. Set the Prescale bits (load a Control Word)
2. Program the VCO (load a Program Word)

Note that care must be taken not to change the Prescale Bit of the currently active register: The results will be unpredictable at best, and it could cause the VCO to go out of lock.

Extended VCLK Frequency Precision

An optional mode set in the CNTL register allows the VCLK PLL to use the MCLK PLL as its reference frequency instead of $f_{(REF)}$. The advantage is that, by proper tuning of the input reference, *very* fine frequency control is possible on the output of VCLK.

Just about any desired value can be achieved with worst-case precision of less than 5 ppm.

The reference frequency oscillator is used to drive the MCLK PLL, which is then fed internally to the VCLK PLL to generate the desired signal. However, please note the following:

- **No usable MCLK output**—This method essentially uses two PLLs to derive a single output, so that the MCLK output will probably be meaningless. Therefore, this method is probably not suited to normal VGA graphics applications.
- **Some increased jitter**—The trade-off associated with deriving the VCLK PLL reference from another PLL is that the MCLK+VCLK combination will tend to exhibit more jitter than a single PLL with a crystal-controlled reference—but the jitter should stay below 1 ns.
- **More challenging programming model**—Another trade-off of having 21 bits each to define both the reference frequency and the output is that it makes finding the optimum 2 programming words an iterative process. To aid in these calculations, Cypress/IC Designs strongly recommends using *BitCalc*, a utility designed to help in this analysis.

Power Management Issues

Power-Down Mode 1

The ICD2063 contains a mechanism to reduce the quiescent power when stand-by operation is desired. In Power-Down Mode 1 (invoked by pulling the PWRDWN signal LOW and having the proper CNTL register bit set to zero), both VCOs are shut down, the VCLKOUT output is forced LOW, and the MCLKOUT output is set to a user-defined low-frequency value to refresh dynamic RAM.

The power-down MCLKOUT value is determined by the following equation:

$$MCLKOUT_{Power-Down} = f_{(REF)} \div (PWRDWN \text{ Reg Divisor Value})$$

The Power-Down register divisor is determined according to the following 4-bit word programmed into the PWRDWN register. (See *Table 11*.)

Table 13. PWRDWN Register Programming

PWRDWN bits				PWRDWN Register Value (Hex)	Power-Down Divisor	MCLKOUT _{Power-Down} ($f_{(REF)} = 14.31818 \text{ MHz}$)
P3	P2	P1	P0			
0	0	0	0	0	N/A	N/A
0	0	0	1	1	32	447.4 kHz
0	0	1	0	2	30	477.3 kHz
0	0	1	1	3	28	511.4 kHz
0	1	0	0	4	26	550.7 kHz
0	1	0	1	5	24	596.6 kHz
0	1	1	0	6	22	650.8 kHz
0	1	1	1	7	20	715.9 kHz
1	0	0	0	8	18 (default)	795.5 kHz
1	0	0	1	9	16	894.9 kHz
1	0	1	0	A	14	1.023 MHz
1	0	1	1	B	12	1.193 MHz
1	1	0	0	C	10	1.432 MHz
1	1	0	1	D	8	1.790 MHz
1	1	1	0	E	6	2.386 MHz
1	1	1	1	F	4	3.580 MHz

Table 15. Driving other Devices with the ICD2063

ICD2063	Other Device	Status
5V	5V	OK
3.3V	5V	OK if driving TTL inputs; if driving CMOS inputs, then ICD2063 output will appear to have a low duty cycle.
5V	3.3V	Potential latch-up problems with other devices; will work if other device's input will accept $V_{IH} = V_{DD} + 2V$.
3.3V	3.3V	OK

Table 16. Driving the ICD2063 with Other Devices

Other Device	ICD2063	Status
5V	5V	OK
3.3V	5V	OK
5V	3.3V	TTL outputs only; input to ICD2063 must not exceed $V_{DD} + 0.3V$
3.3V	3.3V	OK

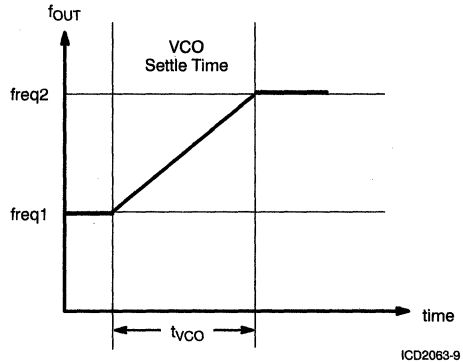
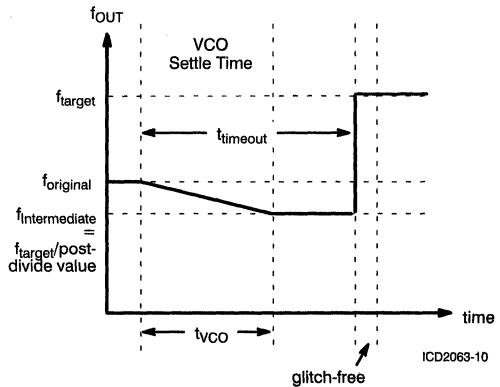
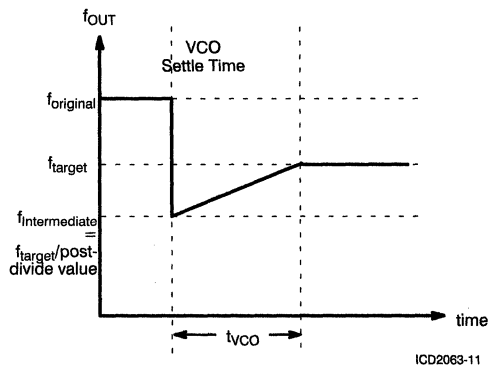
Frequency Transition Options

The ICD2063 may be configured for one of two frequency transition options: the Smooth Transition Option or the MUXREF Option (for compatibility with the ICD2061A).

Smooth Transition Option

Upon changing VCLK or MCLK, either by reprogramming the active register or by selecting a new register, the output will transition in one of two basic ways, depending on the post-divide values (Post-divide is used to divide down the VCO output to frequencies below the normal VCO operating range):

- **Normal Operation**—If the post-divide value (M) is the same for both frequencies (original and target), then the output will transition smoothly and linearly from the original to the target frequency, with no overshoot (see Figure 7).
- **Post-Divide Operation**—If the post-divide value (M) differs between the original and target frequencies, then the output behaves somewhat differently, but will never exceed the greater of the original and target frequencies.
 1. If the post-divide value decreases then, first, a smooth transition occurs to an intermediate frequency (equal to target frequency \div post divider value); second, the post-divide is changed to the new value, resulting in an instantaneous transition to the target frequency (see Figure 8).
 2. If the post-divide value increases then, first, the post-divide value is changed to the new value, resulting in an instantaneous transition to an intermediate frequency (equal to the target frequency \div post divider value); second there is a smooth transition from this frequency to the target frequency (see Figure 9).


Figure 7. Frequency Transition—Smooth Mode: Normal Operation

Figure 8. Frequency Transition—Post-Divide Value Decreases

Figure 9. Frequency Transition—Post-Divide Value Increases

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Input Voltage -0.5V to V_{DD} +0.5V
 Storage Temperature -65°C to +150°C
 Max soldering temperature (10 sec) 260°C

Junction temperature 125°C

Operating Range

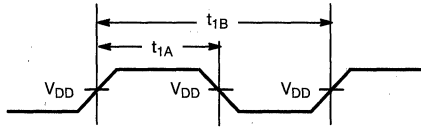
Ambient Temperature	V _{DD} & AV _{DD}
0°C ≤ T _{AMBIENT} ≤ 70°C	5V ± 5% 3.3V ± 10%

Electrical Characteristics Over the Operating Range^{4]}

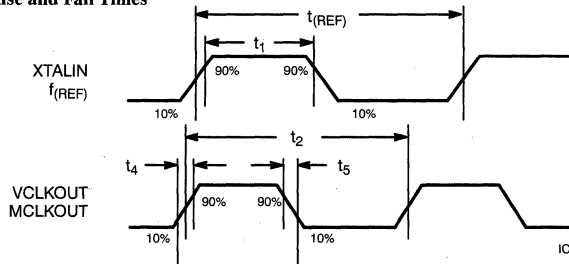
Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V _{DD} & AV _{DD}	Supply Voltage Relative to GND ^[5] 390 kHz – 100 MHz 390 kHz – 120 MHz 390 kHz – 135 MHz	VCLK specs shown (MCLK low end = 312 kHz)	3.0 4.5 4.75		3.6 5.5 5.5	V
V _{OH}	Output HIGH Voltage	I _{OH} = -4.0mA	V _{DD} -0.5			V
V _{OL}	Output LOW Voltage	I _{OL} = 4.0 mA			0.4	V
V _{IH}	Input HIGH Voltage	Except on Crystal Pins	2.0		V _{DD} +0.3	V
V _{IL}	Input LOW Voltage	Except on Crystal Pins	-0.3		0.8	V
I _{IH}	Input HIGH Current	V _{IH} = V _{DD} -0.5			150	μA
I _{IL}	Input LOW Current	V _{IL} = +0.5V			-250	μA
I _{OZ}	Output Leakage Current	(Three-state)			10	μA
I _{DD}	Power Supply Current	5V/3.3V, Inputs @ V _{DD} or GND	15/10		65/44	mA
I _{DD-TYP}	Power Supply Current	5V/3.3V (60 MHz)		35/24	80/50	mA
I _{ADD}	Analog Power Supply Current				10	mA
I _{PD1}	Power-Down Current (Mode 1)	5V/3.3V		6/4	7.5/5.0	mA
I _{PD2}	Power-Down Current (Mode 2)	5V/3.3V		25/20	50/35	μA

Notes:

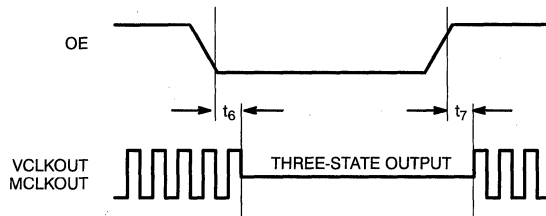
- Input capacitance is typically 10 pF, except for the crystal pins.
- For transition between 3.3V and 5V operation, refer to the *3.3 Volt and 5 Volt Issues* section.

Switching Waveforms
Duty Cycle Timing


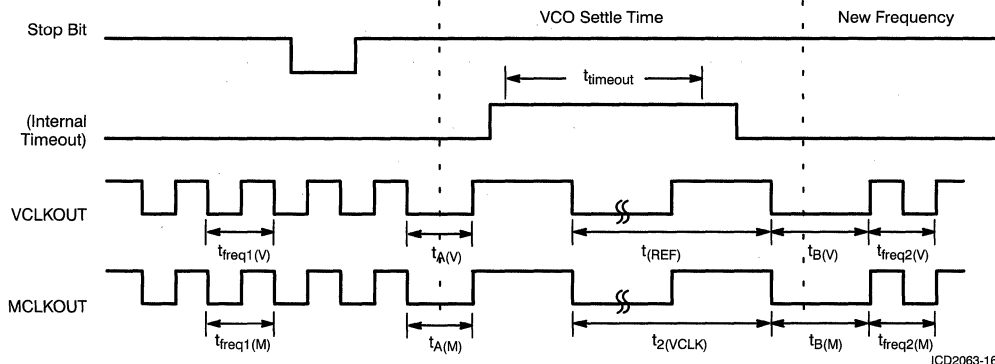
ICD2063-13

Rise and Fall Times


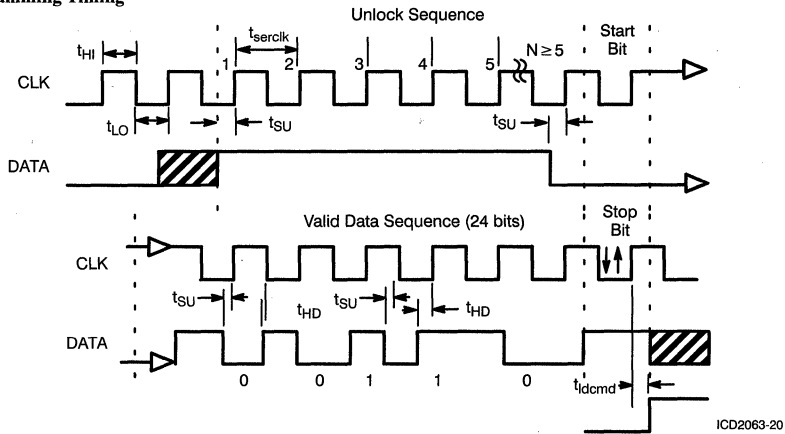
ICD2063-14

Three-State Timing


ICD2063-15

Active MCLK and VCLK Register Programming Timing (MUXREF Mode)


ICD2063-16

Switching Waveforms (continued)
Serial Programming Timing

Configuration Options

Option	Choices	-1	-2	-3
Pin 10 Function	ERROUT or XBUF	XBUF	ERROUT	ERROUT
Pin 14 Function	RESET or SELM	SELM	RESET	SELM
Frequency Transition	Smooth or MUXREF	Smooth	MUXREF	Smooth

Ordering Information^[10]

Ordering Code	Package Name	Package Type	Operating Range	Chip Options
ICD2063	S1	16-Pin SOIC	Commercial ^[11]	-1, -2, -3

Notes:

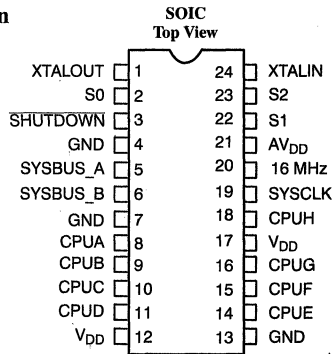
10. Please call your local Cypress representative.

11. 0°C to +70°C

Example: order ICD2063SC-1 for the ICD2063, 16-pin plastic SOIC, commercial temperature range device with the initial frequencies shown in Table 3.

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Pin Configuration


ICD2093-2

Pin Summary

Name	Number	Description
XTALOUT ^[1]	1	Oscillator output to a 14.318 MHz parallel-resonant crystal
S0	2	CPU Clock ROM Select Line—Bit 0 (LSB)
SHUTDOWN (OE)	3	When pulled LOW, shuts down oscillator, PLL, and all dynamic logic. Can be made three-state Output Enable via configuration option. Internal pull-up allows for no-connect if shutdown operation is not needed.
GND	4	Ground
SYSBUS_A	5	14.31818 MHz Output
SYSBUS_B	6	14.31818 MHz Output
GND	7	Ground
CPUA	8	CPU Clock Output A (1X or 2X) ^[2]
CPUB	9	CPU Clock Output B (1X or 2X) ^[2]
CPUC	10	CPU Clock Output C (1X or 2X) ^[2]
CPUD	11	CPU Clock Output D (1X or 2X) ^[2]
V _{DD}	12	+5V to I/O Ring
GND	13	Ground
CPUE	14	CPU Clock Output E (1X or 2X) ^[2]
CPUF	15	CPU Clock Output F (1X or 2X) ^[2]
CPUG	16	CPU Clock Output G (1X or 2X) ^[2]
V _{DD}	17	+5V to I/O Ring
CPUH	18	CPU Clock Output H (1X or 2X) ^[2]
SYSClk	19	24 MHz or 32 MHz Output (factory configurable)
16 MHz	20	16 MHz Output
AV _{DD}	21	+5V to Analog Core
S1	22	CPU Clock ROM Select Line—Bit 1
S2	23	CPU Clock ROM Select Line—Bit 2 (MSB)
XTALIN ^[1]	24	Oscillator input from a 14.31818 MHz crystal

Notes:

- For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF
- All the CPU outputs can be 1X, 2X, or any mix of the two (the outputs of each type are contiguous).

Termination

The ICD2093 provides fast rise and fall times on its outputs to drive large loads, which require the PCB designer to observe proper transmission line techniques. There are three principal techniques for proper termination. The optimum choice depends on individual requirements.

Series Termination

The main drawback of this technique is that C_L adversely affects rise and fall times (see Figure 1).

Parallel Termination

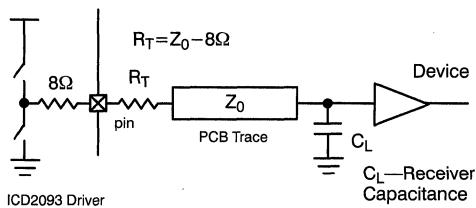
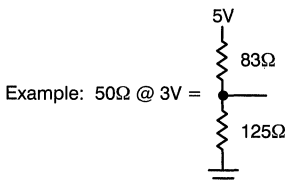
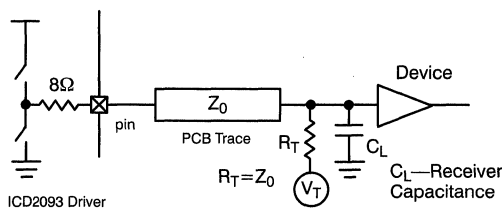
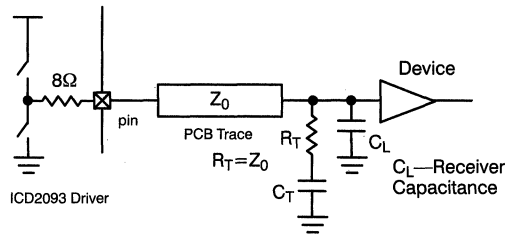
The main drawback of this technique is that it consumes power. $V_T = V_{DD} \div 2$ for minimum power. (Note that V_T should not equal receiver threshold. TTL systems often set V_T at 3V using Thévenin equivalent circuit.) See example divider in Figure 2.

AC Termination

The main drawback of this technique is that it is not as good at high frequencies (see Figure 3).

Power Calculation

Actual current drain is a function of frequency and circuit loading. The operating current of a given output is given by the


Figure 1. Series Termination

Figure 2. Parallel Termination

Figure 3. AC Termination

equation $I = C \cdot V \cdot f$, where I =current, C =load capacitance, V =output voltage in Volts (usually 5V for rail-to-rail CMOS pads) and f =output frequency in MHz.

To calculate total operating current, sum the following:

- $I_{\text{SYSBUS_A}} \Rightarrow C_{14} \cdot V \cdot 14.318$
- $I_{\text{SYSBUS_B}} \Rightarrow C_{24} \cdot V \cdot 14.318$
- $I_{\text{CPUA}} \Rightarrow C_{\text{CLKA}} \cdot V \cdot f_{\text{CLKA}}$
- $I_{\text{CPUB}} \Rightarrow C_{\text{CLKB}} \cdot V \cdot f_{\text{CLKB}}$
- $I_{\text{CPUC}} \Rightarrow C_{\text{CLKC}} \cdot V \cdot f_{\text{CLKC}}$
- $I_{\text{CPUD}} \Rightarrow C_{\text{CLKD}} \cdot V \cdot f_{\text{CLKD}}$
- $I_{\text{CPUE}} \Rightarrow C_{\text{CLKE}} \cdot V \cdot f_{\text{CLKE}}$
- $I_{\text{CPUF}} \Rightarrow C_{\text{CLKF}} \cdot V \cdot f_{\text{CLKF}}$
- $I_{\text{CPUG}} \Rightarrow C_{\text{CLKG}} \cdot V \cdot f_{\text{CLKG}}$
- $I_{\text{CPUH}} \Rightarrow C_{\text{CLKH}} \cdot V \cdot f_{\text{CLKH}}$
- $I_{\text{(Internal)}} \Rightarrow .06 \text{ A (60 mA)}$

This yields an approximation of the actual operating current. For unconnected output pins, one can assume 5–10 pF loading, depending on the package type.

Some typical values are displayed in Table 5.

Table 4. Operating Current Typical Values

Frequency	Capacitive Load	Current (in mA)
66.6 MHz	30 pF	115

General Considerations
Power-Down Operation

In the power-down state, the oscillator, PLL, and all dynamic logic is shut down.

Note that, during shutdown, the internal PLLs are turned off. Upon restarting, there will be a 5-msec interval during which the VCOs stabilize. See *Power-Down Timing* in the *Switching Waveforms* section for further timing information.

Three-State Output Operation

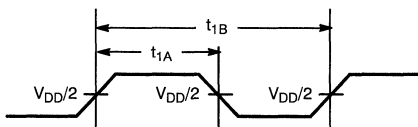
If the OE configuration is chosen, then the **SHUTDOWN** pin becomes an OE pin, which, when pulled LOW, will three-state all the clock output lines. This supports Wired-OR connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The OE signal contains an internal pull-up; it can be left unconnected if three-state operation is not required. The output pads contain weak pull-down resistors.

Switching Characteristics^[5]

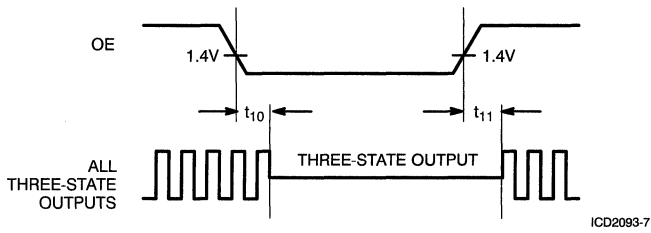
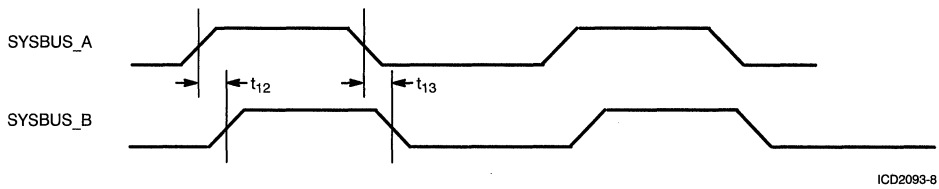
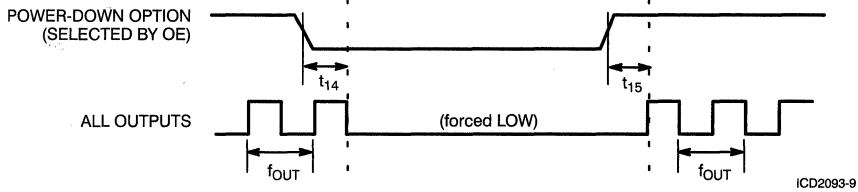
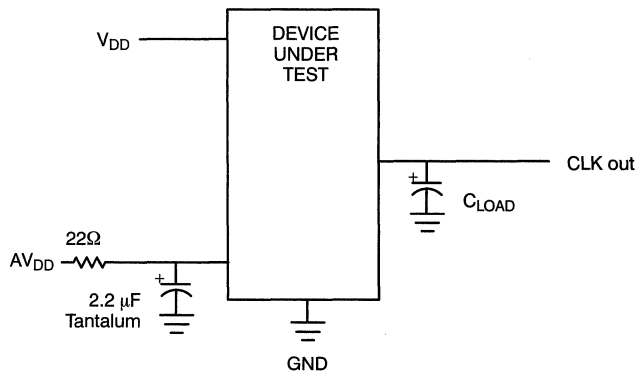
Parameter	Name	Description	Min.	Typ.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference input normal value		14.318		MHz
$t_{(REF)}$	Reference Clock Period	$1 + f_{(REF)}$		69.84		ns
t_1	Input Duty Cycle	Duty cycle for the input oscillator defined as $t_1 = t_{1A} + t_{1B}$	25%	50%	75%	
t_2	Output Period		10 100 MHz		100 10 MHz	ns
t_3	Output Duty Cycle	Duty cycle for the outputs, measured @ CMOS V_{TH} of $V_{DD} + 2$ (special screening required for 100 MHz) $t_3 = t_{1A} + t_{1B}$	40%		60%	
t_4	Rise Times	Rise time of clock outputs (50-pF load @ 10 MHz)			3.5	ns
t_5	Fall Times	Fall time of clock outputs (50-pF load @ 10 MHz)			4	ns
t_6	Skew	Leading edge skew between 1X and 2X outputs and $C_L = 50$ pF			500	ps
t_8	Skew	Leading edge skew between 1X and 1X or 2X and 2X outputs and $C_L = 50$ pF			250	ps
t_{VCO}	VCO Settle Time	Time for VCO to transition smoothly and monotonically from the original to the new frequency			3	msec
t_{10}	Three-state Time	Time for the outputs to go into three-state mode after OE signal goes LOW			20	ns
t_{11}	Clock Enable Time	Time for the outputs to recover from three-state mode after OE signal goes HIGH			20	ns
t_{12}	SYSBUS Skew	Leading edge skew between SYSBUS outputs			500	ps
t_{13}	SYSBUS Skew	Trailing edge skew between SYSBUS outputs			500	ps
t_{14}	Power-Down	Time to invoke power-down option			20	ns
t_{15}	Power-Up	Time to revoke power-down option			20	ns

Note:

5. Input capacitance is typically 10 pF, except for the crystal pads.

Switching Waveforms
Duty Cycle Timing


ICD2093-3

Switching Waveforms (continued)
Three-State Timing

SYSBUS Skew

Power-Down Timing

Test Circuit


Configuration Options

Signal/Pin	Option -1	Option -2
CPUA	÷2	÷2
CPUB	÷2	÷2
CPUC	÷2	÷1
CPUD	÷2	÷1
CPUE	÷2	÷1
CPUF	÷2	÷1
CPUG	÷2	÷1
CPUH	÷1	÷1
Pin 3	OE	SHUTDOWN
SYSCLK	24 MHz	24 MHz

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Clock Output Options
ICD2093	S13	24-Pin SOIC	C=0°C to +70°C @ V _{DD} =5V	Standard Configuration -1

Example: Order ICD2093SC-1 for the ICD2093, 24-pin plastic SOIC, commercial temperature range device which uses the standard configuration code -1 (SYSCLK=24 MHz, Power-Down not enabled, one ÷1 CPU clock and seven ÷2 CPU clocks).

Custom configurations are also available. To order a custom configuration, please contact your Cypress representative.

Document #: 38-00401

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Input Voltage -0.5V to $V_{DD} + 0.5V$
 Storage Temperature -55°C to +125°C
 Max soldering temperature (10 sec) 260°C
 Junction Temperature +125°C

Operating Range

Ambient Temperature	V_{DD}
$0^{\circ}C \leq T_{AMBIENT} \leq 70^{\circ}C$	$5V \pm 10\%$
C_L 25 pF max.	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DD}	Supply Current	$V_{DD} = \text{Max.}$, Output <90 MHz CE = V_{DD}		55.0	mA
V_{OH}	Output HIGH Voltage	$I_{OH} = -4.0\text{mA}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 4.0\text{mA}$		0.4	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_{IH}	Input HIGH Current	$V_{IH} = V_{DD} - 0.5V$		100.0	μA
I_{IL}	Input LOW Current	$V_{IL} = +0.5V$		-250.0	μA

Switching Characteristics Over the Operating Range^[1]

Parameter	Description	Test Conditions	Min.	Max.	Unit
t_1	Output Period	5V Operation	11.1 90 MHz	1066.7 937.5 kHz	ns
	Output Duty Cycle	Duty cycle for output pads, define as $t_1 \div t_2$	40	60	%
t_3	Rise Time	Clock output rise time		4	ns
t_4	Fall Time	Clock output fall time		4	ns
t_5	Power-Up	Time for output to become valid		15	msec
t_6	Three-State	Time for output oscillator to enter three-state mode after OE goes LOW		12	ns
t_7	CLK Valid	Time for output oscillator to enter three-state mode after OE goes HIGH		12	ns

Note:

1. Input capacitance is typically 10pF.

Programmable Skew Clock Buffer (PSCB)

Features

- Output pair skew <100 ps typical (250 max.)
- All outputs skew <250 ps typical (500 max.)
- 3.75- to 80-MHz output operation
- User-selectable output functions
 - Selectable skew to 18 ns
 - Inverted and non-inverted
 - Operation at 1/2 and 1/4 input frequency
 - Operation at 2x and 4x input frequency (input as low as 3.75 MHz)
- Zero input to output delay
- 50% duty-cycle outputs
- Outputs drive 50Ω terminated lines
- Low operating current
- 32-pin PLCC/LCC package
- Jitter < 200 ps peak-to-peak (< 25 ps RMS)

- Compatible with a Pentium™ -based processor

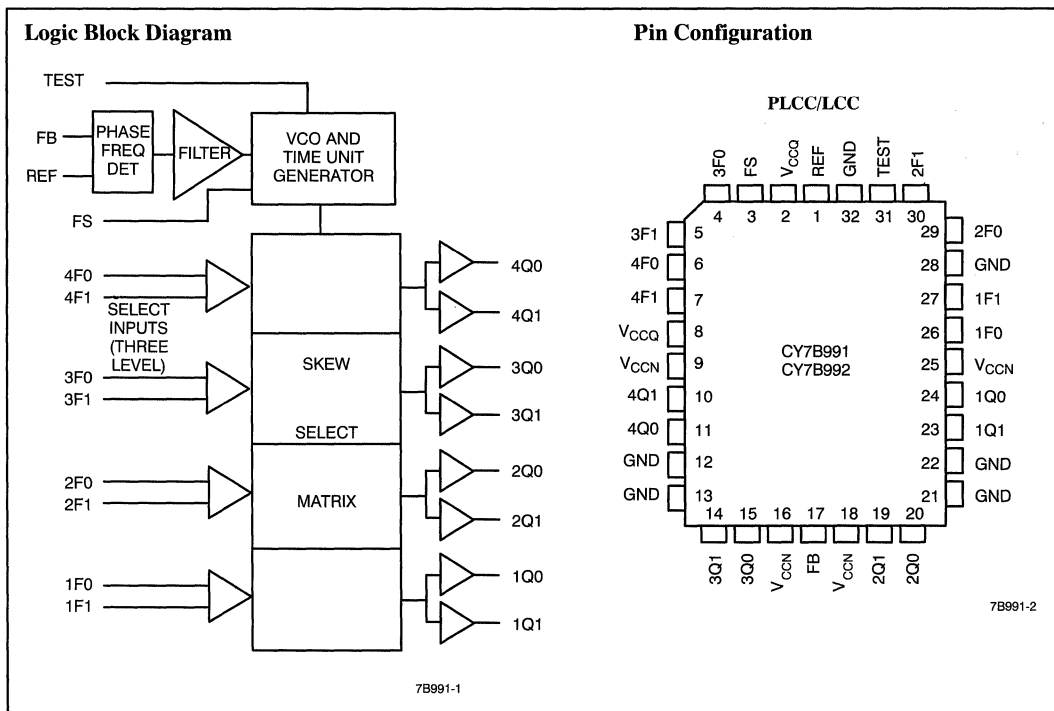
Functional Description

The CY7B991 and CY7B992 Programmable Skew Clock Buffers (PSCB) offer user-selectable control over system clock functions. These multiple-output clock drivers provide the system integrator with functions necessary to optimize the timing of high-performance computer systems. Eight individual drivers, arranged as four pairs of user-controllable outputs, can each drive terminated transmission lines with impedances as low as 50Ω while delivering minimal and specified output skews and full-swing logic levels (CY7B991 TTL or CY7B992 CMOS).

Each output can be hardwired to one of nine delay or function configurations. Delay increments of 0.7 to 1.5 ns are de-

termined by the operating frequency with outputs able to skew up to ±6 time units from their nominal “zero” skew position. The completely integrated PLL allows external load and transmission line delay effects to be canceled. When this “zero delay” capability of the PSCB is combined with the selectable output skew functions, the user can create output-to-output delays of up to ±12 time units.

Divide-by-two and divide-by-four output functions are provided for additional flexibility in designing complex clock systems. When combined with the internal PLL, these divide functions allow distribution of a low-frequency clock that can be multiplied by two or four at the clock destination. This facility minimizes clock distribution difficulty while allowing maximum system clock speed and flexibility.



Pentium is a trademark of Intel Corporation.

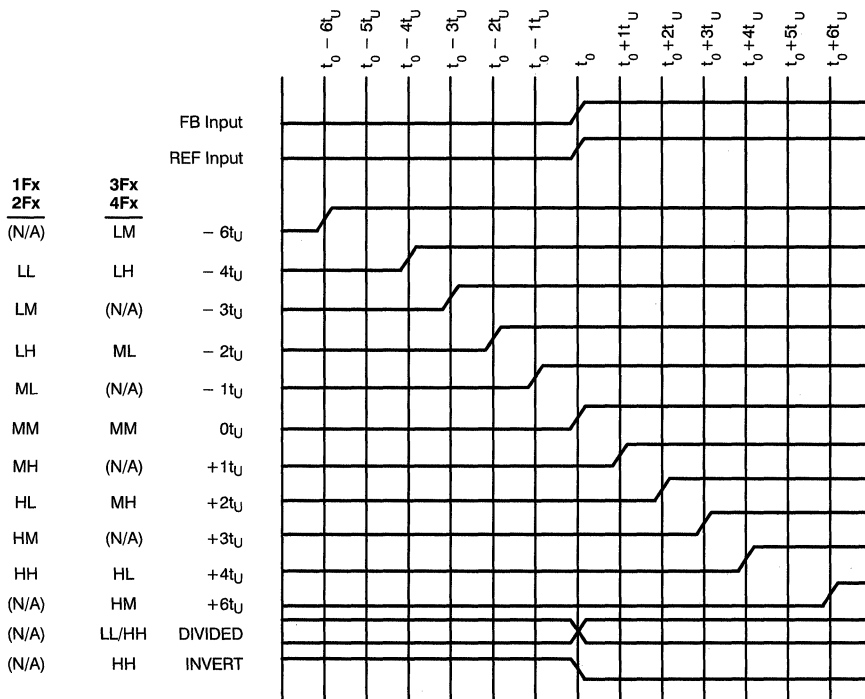


Figure 1. Typical Outputs with FB Connected to a Zero-Skew Output^[4]

7B991-3

Test Mode

The TEST input is a three-level input. In normal system operation, this pin is connected to ground, allowing the CY7B991/CY7B992 to operate as explained briefly above (for testing purposes, any of the three-level inputs can have a removable jumper to ground, or be tied LOW through a 100Ω resistor. This will allow an external tester to change the state of these pins.)

If the TEST input is forced to its MID or HIGH state, the device will operate with its internal phase locked loop disconnected, and input levels supplied to REF will directly control all outputs. Relative output to output functions are the same as in normal mode.

In contrast with normal operation (TEST tied LOW). All outputs will function based only on the connection of their own function select inputs (xF0 and xF1) and the waveform characteristics of the REF input.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

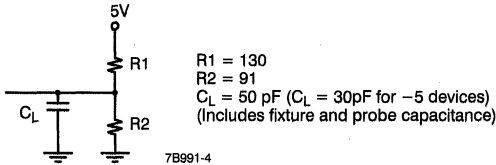
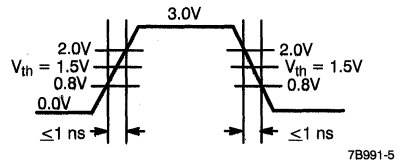
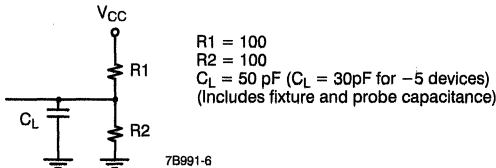
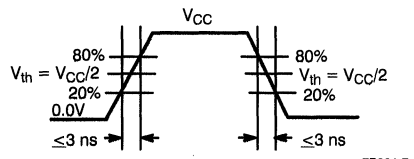
Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
Output Current into Outputs (LOW)	64 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Military ^[5]	-55°C to +125°C	5V ± 10%

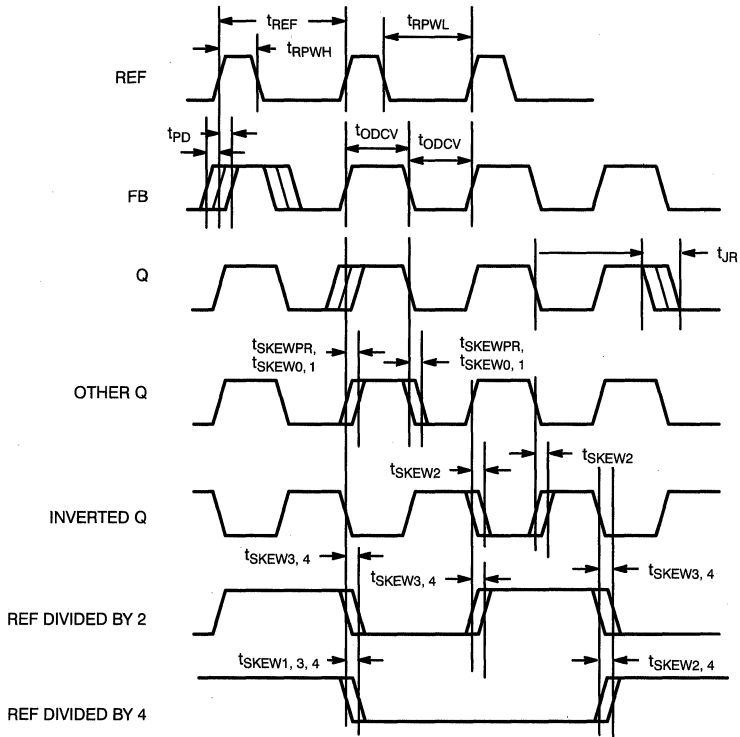
Notes:

- 4 FB connected to an output selected for "zero" skew (i.e., xF1 = xF0 = MID).
5. Indicates case temperature.

AC Test Loads and Waveforms

TTL AC Test Load (CY7B991)

TTL Input Test Waveform (CY7B991)

CMOS AC Test Load (CY7B992)

CMOS Input Test Waveform (CY7B992)
Switching Characteristics Over the Operating Range^[2, 13]

Parameter	Description	CY7B991-5			CY7B992-5			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW ^[1, 2]		15		30	15		MHz
		FS = MID ^[1, 2]		25		50	25		
		FS = HIGH ^[1, 2, 3]		40		80	40	80 ^[14]	
t_{RPWH}	REF Pulse Width HIGH	5.0			5.0			ns	
t_{RPWL}	REF Pulse Width LOW	5.0			5.0			ns	
t_U	Programmable Skew Unit	See Table I							
t_{SKEWPR}	Zero Output Matched-Pair Skew (XQ0, XQ1) ^[15, 16]		0.1	0.25		0.1	0.25	ns	
t_{SKEW0}	Zero Output Skew (All Outputs) ^[15, 17]		0.25	0.5		0.25	0.5	ns	
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs) ^[15, 18]		0.6	0.7		0.6	0.7	ns	
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided) ^[15, 18]		0.5	1.0		0.6	1.2	ns	
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs) ^[15, 18]		0.5	0.7		0.5	0.7	ns	
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted) ^[15, 18]		0.5	1.0		0.6	1.3	ns	
t_{SKEW5}	Device-to-Device Skew ^[19, 25]			0.2			0.2	ns	
t_{PD}	Propagation Delay, REF Rise to FB Rise	-0.5	0.0	+0.5	-0.5	0.0	+0.5	ns	
t_{ODCV}	Output Duty Cycle Variation ^[20]	-1.0	0.0	+1.0	-1.0	0.0	+1.0	ns	
t_{PWH}	Output HIGH Time Deviation from 50% ^[21, 22]			2.5			3.5	ns	
t_{PWL}	Output LOW Time Deviation from 50% ^[21, 22]			3			3.5	ns	
t_{ORISE}	Output Rise Time ^[21, 23]	0.15	1.0	1.5	0.5	2.0	3.0	ns	
t_{OFALL}	Output Fall Time ^[21, 23]	0.15	1.0	1.5	0.5	2.0	3.0	ns	
t_{LOCK}	PLL Lock Time ^[24]			0.5			0.5	ms	
t_{JR}	Cycle-to-Cycle Output Jitter	RMS ^[25]		25			25	ps	
		Peak-to-Peak ^[25]		200			200	ps	

AC Timing Diagrams



7B991-8

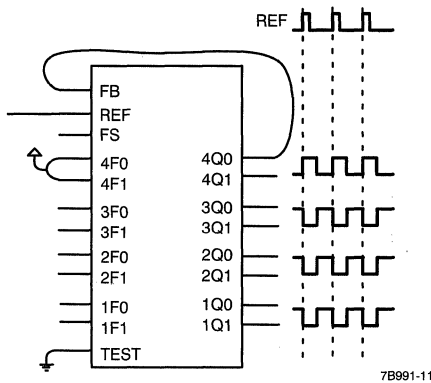
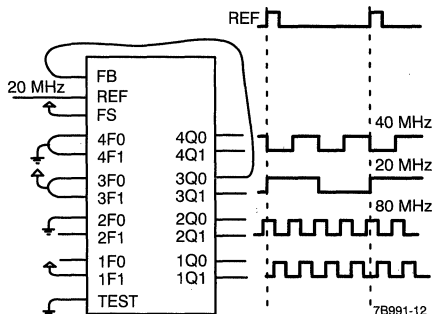

Figure 4. Inverted Output Connections

Figure 4 shows an example of the invert function of the PSCB. In this example the 4Q0 output used as the FB input is programmed for invert (4F0 = 4F1 = HIGH) while the other three pairs of outputs are programmed for zero skew. When 4F0 and 4F1 are tied high, 4Q0 and 4Q1 become inverted zero phase outputs. The PLL aligns the rising edge of the FB input with the rising edge of the REF. This causes the 1Q, 2Q, and 3Q outputs to become the “inverted” outputs with respect to the REF input. By selecting which output is connect to FB, it is possible to have 2 inverted and 6 non-inverted outputs or 6 inverted and 2 non-inverted outputs. The correct configuration would be determined by the need for more (or fewer) inverted outputs. 1Q, 2Q, and 3Q outputs can also be skewed to compensate for varying trace delays independent of inversion on 4Q.

Figure 5 illustrates the PSCB configured as a clock multiplier. The 3Q0 output is programmed to divide by four and is fed back to FB. This causes the PLL to increase its frequency until the 3Q0 and 3Q1 outputs are locked at 20 MHz while the 1Qx and 2Qx outputs run at 80 MHz. The 4Q0 and 4Q1 outputs are programmed to divide by two, which results in a 40-MHz waveform at these outputs. Note that the 20- and 40-MHz clocks fall simultaneously and are out of phase on their rising edge. This will al-


Figure 5. Frequency Multiplier with Skew Connections

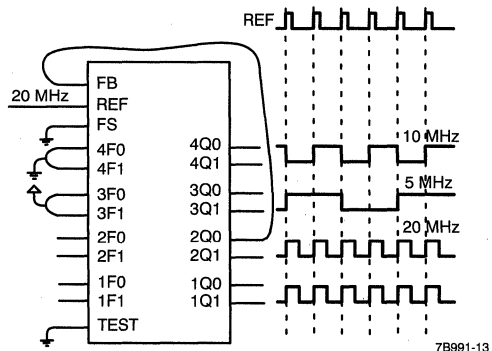
low the designer to use the rising edges of the $\frac{1}{2}$ frequency and $\frac{1}{4}$ frequency outputs without concern for rising-edge skew. The 2Q0, 2Q1, 1Q0, and 1Q1 outputs run at 80 MHz and are skewed by programming their select inputs accordingly. Note that the FS pin is wired for 80-MHz operation because that is the frequency of the fastest output.

Figure 6 demonstrates the PSCB in a clock divider application. 2Q0 is fed back to the FB input and programmed for zero skew. 3Qx is programmed to divide by four. 4Qx is programmed to divide by two. Note that the falling edges of the 4Qx and 3Qx outputs are aligned. This allows use of the rising edges of the $\frac{1}{2}$ frequency and $\frac{1}{4}$ frequency outputs without concern for skew mismatch. The 1Qx outputs are programmed to zero skew and are aligned with the 2Qx outputs. In this example, the FS input is grounded to configure the device in the 15- to 30-MHz range since the highest frequency output is running at 20 MHz.

Figure 7 shows some of the functions that are selectable on the 3Qx and 4Qx outputs. These include inverted outputs and outputs that offer divide-by-2 and divide-by-4 timing. An inverted output allows the system designer to clock different subsystems on opposite edges, without suffering from the pulse asymmetry typical of non-ideal loading. This function allows the two subsystems to each be clocked 180 degrees out of phase, but still to be aligned within the skew spec.

The divided outputs offer a zero-delay divider for portions of the system that need the clock to be divided by either two or four, and still remain within a narrow skew of the “1X” clock. Without this feature, an external divider would need to be added, and the propagation delay of the divider would add to the skew between the different clock signals.

These divided outputs, coupled with the Phase Locked Loop, allow the PSCB to multiply the clock rate at the REF input by either two or four. This mode will enable the designer to distribute a low-frequency clock between various portions of the system, and then locally multiply the clock rate to a more suitable frequency, while still maintaining the low-skew characteristics of the clock driver. The PSCB can perform all of the functions described above at the same time. It can multiply by two and four or divide by two (and four) at the same time that it is shifting its outputs over a wide range or maintaining zero skew between selected outputs.


Figure 6. Frequency Divider Connections

Ordering Information

Accuracy (ps)	Ordering Code	Package Name	Package Type	Operating Range
500	CY7B991-5JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
750	CY7B991-7JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B991-7JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B991-7LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military
500	CY7B992-5JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
750	CY7B992-7JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B992-7JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B992-7LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military

**MILITARY SPECIFICATIONS
Group A Subgroup Testing**
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
V _{IHH}	1, 2, 3
V _{IMM}	1, 2, 3
V _{ILL}	1, 2, 3
I _{IH}	1, 2, 3
I _{IL}	1, 2, 3
I _{IHH}	1, 2, 3
I _{IMM}	1, 2, 3
I _{ILL}	1, 2, 3
I _{CCQ}	1, 2, 3
I _{CCN}	1, 2, 3

Document #: 38-00188-F

Switching Characteristics

Parameter	Subgroups
t _{NOM}	9, 10, 11
t _{RPWH}	9, 10, 11
t _{RPWL}	9, 10, 11
t _U	9, 10, 11
t _{SKEWPR}	9, 10, 11
t _{SKEW0}	9, 10, 11
t _{SKEW1}	9, 10, 11
t _{SKEW2}	9, 10, 11
t _{SKEW3}	9, 10, 11
t _{SKEW4}	9, 10, 11
t _{PD}	9, 10, 11
t _{ODCV}	9, 10, 11
t _{PWH}	9, 10, 11
t _{PWL}	9, 10, 11
t _{QRISE}	9, 10, 11
t _{QFALL}	9, 10, 11
t _{LOCK}	9, 10, 11



Pin Definitions

Signal Name	I/O	Description
REF	I	Reference frequency input. This input supplies the frequency and timing against which all functional variation is measured.
FB	I	PLL feedback input (typically connected to one of the eight outputs).
FS ^[1, 2, 3]	I	Three-level frequency range select. See <i>Table 1</i> .
TEST	I	Three-level select. See Test Mode section.
Q[0..7]	O	Clock outputs.
V _{CCN}	PWR	Power supply for output drivers.
V _{CCQ}	PWR	Power supply for internal circuitry.
GND	PWR	Ground.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied -55°C to +125°C
 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Input Voltage -0.5V to +7.0V
 Output Current into Outputs (LOW) 64 mA
 Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY7B9910		CY7B9920		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -16 mA	2.4				V
		V _{CC} = Min., I _{OH} = -40 mA			V _{CC} -0.75		
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 46 mA		0.45			V
		V _{CC} = Min., I _{OL} = 46 mA				0.45	
V _{IH}	Input HIGH Voltage (REF and FB inputs only)		2.0	V _{CC}	V _{CC} - 1.35	V _{CC}	V
V _{IL}	Input LOW Voltage (REF and FB inputs only)		-0.5	0.8	-0.5	1.35	V
V _{IHH}	Three-Level Input HIGH Voltage (Test, FS) ^[1]	Min. ≤ V _{CC} ≤ Max.	V _{CC} - 1V	V _{CC}	V _{CC} - 1V	V _{CC}	V
V _{IMM}	Three-Level Input MID Voltage (Test, FS) ^[1]	Min. ≤ V _{CC} ≤ Max.	V _{CC} /2 - 500 mV	V _{CC} /2 + 500 mV	V _{CC} /2 - 500 mV	V _{CC} /2 + 500 mV	V
V _{ILL}	Three-Level Input LOW Voltage (Test, FS) ^[1]	Min. ≤ V _{CC} ≤ Max.	0.0	1.0	0.0	1.0	V
I _{IH}	Input HIGH Leakage Current (REF and FB inputs only)	V _{CC} = Max., V _{IN} = Max.		10		10	µA
I _{IL}	Input LOW Leakage Current (REF and FB inputs only)	V _{CC} = Max., V _{IN} = 0.4V	-500		-500		µA
I _{IHH}	Input HIGH Current (Test, FS)	V _{IN} = V _{CC}		200		200	µA
I _{IMM}	Input MID Current (Test, FS)	V _{IN} = V _{CC} /2	-50	50	-50	50	µA
I _{ILL}	Input LOW Current (Test, FS)	V _{IN} = GND		-200		-200	µA

Switching Characteristics Over the Operating Range^[7]

Parameter	Description	CY7B9910-5			CY7B9920-5			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.		
f _{NOM}	Operating Clock Frequency in MHz	FS = LOW ^[8, 9]	15		30	15		30	MHz
		FS = MID ^[8, 9]	25		50	25		50	
		FS = HIGH ^[8, 9, 10]	40		80	40		80 ^[11]	
t _{RPWH}	REF Pulse Width HIGH	5.0			5.0			ns	
t _{RPWL}	REF Pulse Width LOW	5.0			5.0			ns	
t _{SKEW}	Zero Output Skew (All Outputs) ^[12, 13]		0.25	0.5		0.25	0.5	ns	
t _{DEV}	Device-to-Device Skew ^[14, 15]			1.0			1.0	ns	
t _{PD}	Propagation Delay, REF Rise to FB Rise	- 0.5	0.0	+0.5	- 0.5	0.0	+0.5	ns	
t _{ODCV}	Output Duty Cycle Variation ^[16]	- 1.0	0.0	+1.0	- 1.0	0.0	+1.0	ns	
t _{ORISE}	Output Rise Time ^[17, 18]	0.15	1.0	1.5	0.5	2.0	3.0	ns	
t _{OFALL}	Output Fall Time ^[17, 18]	0.15	1.0	1.5	0.5	2.0	3.0	ns	
t _{LOCK}	PLL Lock Time ^[19]			0.5			0.5	ms	
t _{JR}	Cycle-to-Cycle Output Jitter	Peak to Peak ^[15]			200			200	ps
		RMS ^[15]			25			25	ps

Parameter	Description	CY7B9910-7			CY7B9920-7			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.		
f _{NOM}	Operating Clock Frequency in MHz	FS = LOW ^[8, 9]	15		30	15		30	MHz
		FS = MID ^[8, 9]	25		50	25		50	
		FS = HIGH ^[8, 9, 10]	40		80	40		50	
t _{RPWH}	REF Pulse Width HIGH	5.0			5.0			ns	
t _{RPWL}	REF Pulse Width LOW	5.0			5.0			ns	
t _{SKEW}	Zero Output Skew (All Outputs) ^[12, 13]		0.3	0.75		0.3	0.75	ns	
t _{DEV}	Device-to-Device Skew ^[14, 15]			1.5			1.5	ns	
t _{PD}	Propagation Delay, REF Rise to FB Rise	- 0.7	0.0	+0.7	- 0.7	0.0	+0.7	ns	
t _{ODCV}	Output Duty Cycle Variation ^[16]	- 1.2	0.0	+1.2	- 1.2	0.0	+1.2	ns	
t _{ORISE}	Output Rise Time ^[17, 18]	0.15	1.5	2.5	0.5	3.0	5.0	ns	
t _{OFALL}	Output Fall Time ^[17, 18]	0.15	1.5	2.5	0.5	3.0	5.0	ns	
t _{LOCK}	PLL Lock Time ^[19]			0.5			0.5	ms	
t _{JR}	Cycle-to-Cycle Output Jitter	Peak to Peak ^[15]			200			200	ps
		RMS ^[15]			25			25	ps

Notes:

- Test measurement levels for the CY7B9910 are TTL levels (1.5V to 1.5V). Test measurement levels for the CY7B9920 are CMOS levels ($V_{CC}/2$ to $V_{CC}/2$). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
- For all three-state inputs, HIGH indicates a connection to V_{CC} , LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.
- The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the VCO (see Logic Block Diagram). The frequency appearing at the REF and FB inputs will be f_{NOM} when the output connected to FB is unswitched. The frequency of the REF and FB inputs will be f_{NOM}/X when the device is configured for a frequency multiplication by using external division in the feedback path of value X.
- When the FS pin is selected HIGH, the REF input must not transition upon power-up until V_{CC} has reached 4.3V.
- Except as noted, all CY7B9920-5 timing parameters are specified to 80-MHz with a 30-pF load.
- SKEW is defined as the time between the earliest and the latest output transition among all outputs when all are loaded with 50 pF and terminated with 50Ω to 2.06V (CY7B9910) or $V_{CC}/2$ (CY7B9920).
- t_{SKEW} is defined as the skew between outputs.
- t_{DEV} is the output-to-output skew between any two outputs on separate devices operating under the same conditions (V_{CC} , ambient temperature, air flow, etc.).
- Tested initially and after any design or process changes that may affect these parameters.
- t_{ODCV} is the deviation of the output from a 50% duty cycle.
- Specified with outputs loaded with 30 pF for the CY7B99X0-5 devices and 50 pF for the CY7B99X0-7 devices. Devices are terminated through 50Ω to 2.06V (CY7B9910) or $V_{CC}/2$ (CY7B9920).
- t_{ORISE} and t_{OFALL} measured between 0.8V and 2.0V for the CY7B9910 or 0.8V_{CC} and 0.2V_{CC} for the CY7B9920.
- t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

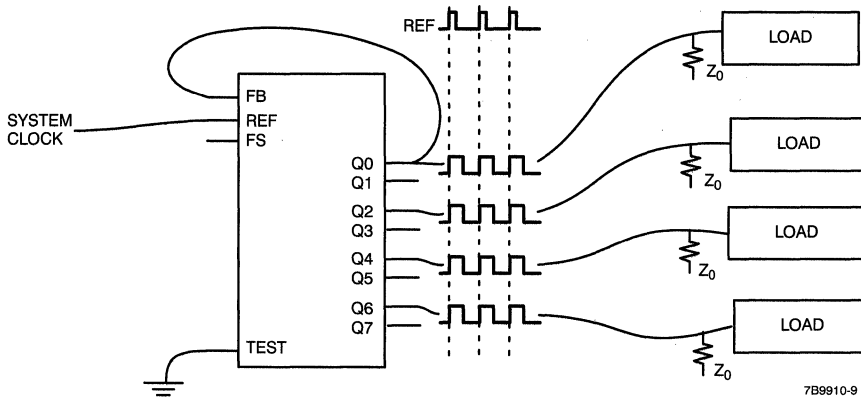
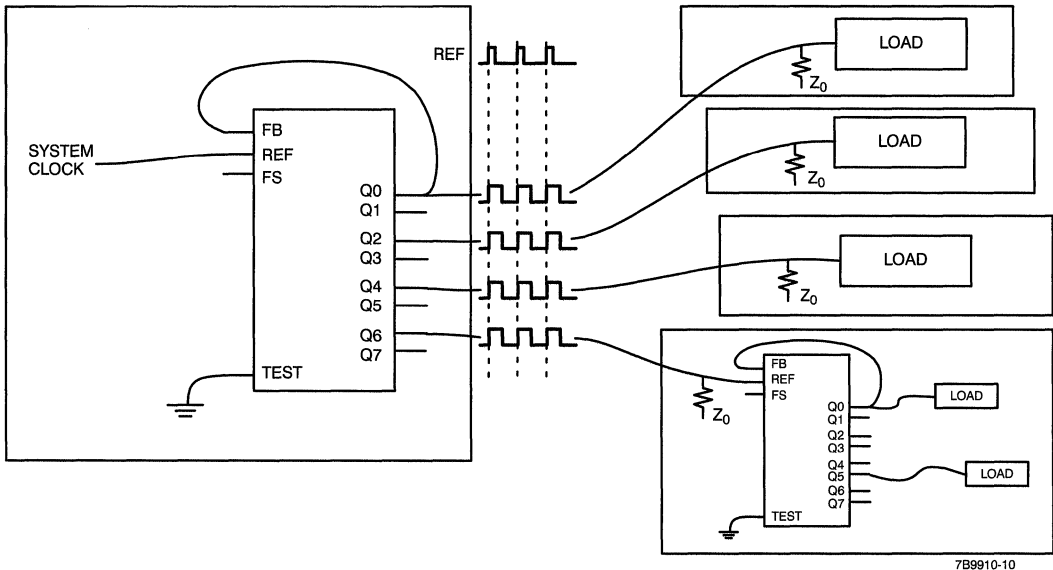

Figure 1. Zero-Skew and/or Zero-Delay Clock Driver
Operational Mode Descriptions

Figure 1 shows the device configured as a zero-skew clock buffer. In this mode the 7B9910/9920 can be used as the basis for a low-skew clock distribution tree. The outputs are aligned and may each drive a terminated transmission line to an independent load. The FB input can be tied to any output and the operating frequency range is selected with the FS pin. The low-skew specification, coupled with the ability to drive terminated transmission

lines (with impedances as low as 50 ohms), allows efficient printed circuit board design.

Figure 2 shows the CY7B9910/9920 connected in series to construct a zero-skew clock distribution tree between boards. Cascaded clock buffers will accumulate low-frequency jitter because of the non-ideal filtering characteristics of the PLL filter. It is not recommended that more than two clock buffers be connected in series.


Figure 2. Board-to-Board Clock Distribution





Section Contents

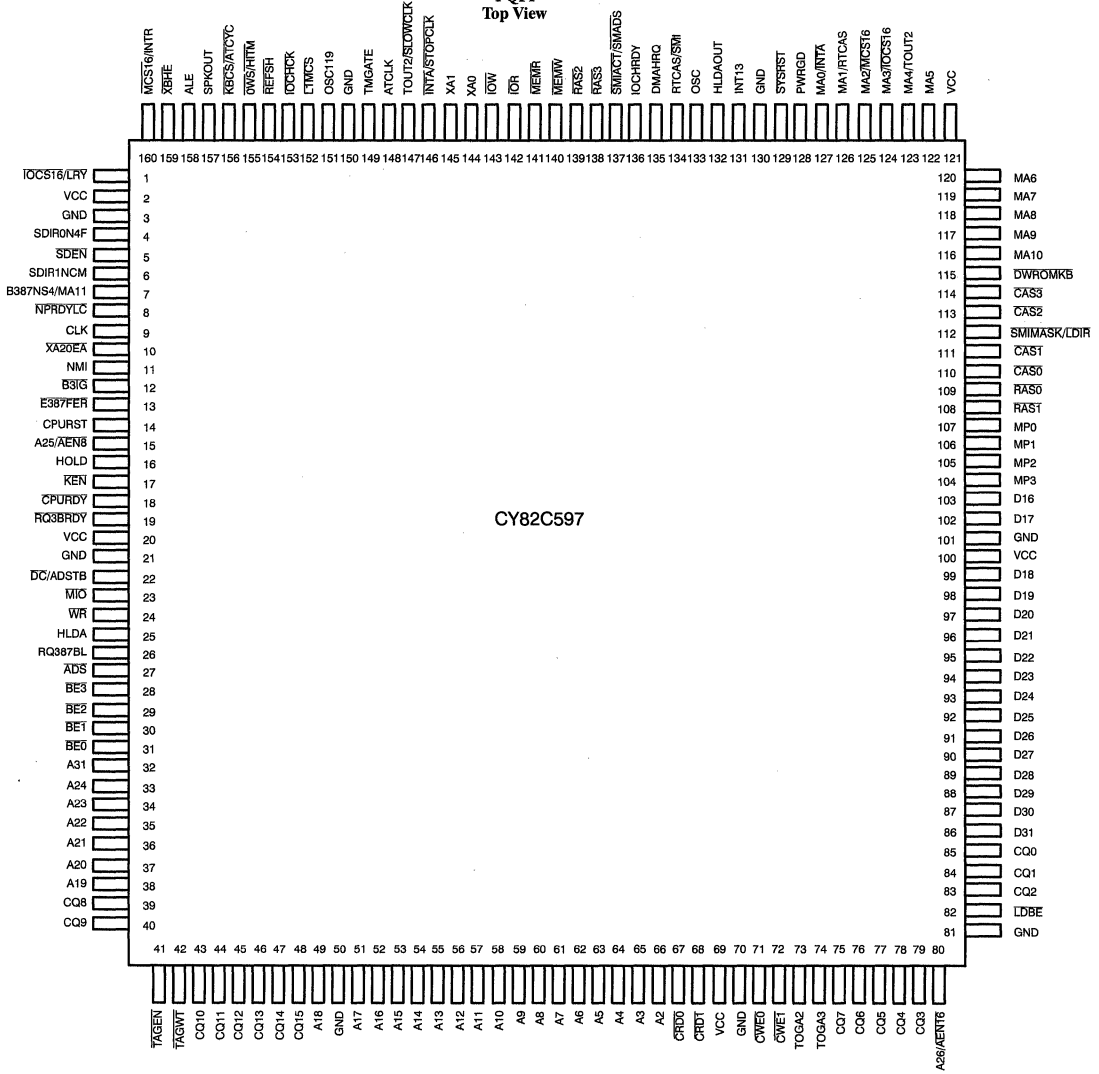
PC Chipsets

Page Number

Device	Description	
CY82C597	386/486 Green Chipset	11-1
CY82C599	Intelligent PCI Bus Controller	11-61

Pin Configuration

PQFP
Top View



the arbitration between Refresh, DMA and non-TURBO hold request.

5. Level 1 Write-back CPU Support

In order to improve system performance and reduce bus bandwidth requirements, some CPUs (from Intel, AMD, Cyrix, etc.) implement an internal, level 1, write-back cache. Write-back CPUs must snoop (by way of inquiry transactions) all memory transactions. The CY82C597 will generate an inquiry cycle by asserting $\overline{\text{EADS}}$, which will be monitored by the CPU, whenever there is an ISA DMA/MASTER memory cycle. During VESA master memory cycles, the VESA master must assert $\overline{\text{EADS}}$ along with $\overline{\text{ADS}}$. For PCI master memory cycles, the CY82C597 will assert $\overline{\text{EADS}}$.

Upon seeing $\overline{\text{EADS}}$ asserted, a write-back CPU will check the status of its internal cache. If the CPU's cache contains the line and it is marked modified (the data in the level 1 cache is more up-to-date than the data in main memory), the CPU will assert the HITM signal. If the CY82C597 sees HITM asserted, it will relinquish the bus to the CPU and will not respond to the original access until the CPU first copies the cache data back to system memory (this is referred to as a write-back cycle). Write-backs consist of burst write cycles (the CY82C597 will handle burst writes to memory). The CY82C597 will wait until the CPU has completed the write-back transaction before allowing any bus master to access the modified memory location.

The CY82C597 has an inquiry filter to reduce the overhead of unnecessary snoop cycles. Every time a bus master attempts to access system memory, the CY82C597 will check to see if the address was previously used for an inquiry cycle. If the address was "snooped" in the previous transaction, the CY82C597 will not generate an inquiry cycle (for ISA/DMA MASTER cycles) or will ignore the results of the inquiry cycle (for VESA/PCI Bus Master cycles) and will allow the transaction to pass directly to system memory.

6. Write-back/Write-through Cache Controller

Write-back Operation

The CY82C597 implements a Burst mode, write-back cache controller. It monitors TAGA[6:0] and compares it with the CPU TAG address. If the cache is enabled and the Tag address matches the CPU address, a "cache hit" is detected. During a read hit, the CY82C597 will burst four double words to the CPU by alternating $\overline{\text{CRD0}}$ and $\overline{\text{CRD1}}$ (2 Banks of cache) or strobing $\overline{\text{CRD0}}$ four times (1 Bank of cache).

In the case of a write hit, the CPU data will be written to the cache RAMs by asserting $\overline{\text{CWE0}}$ or $\overline{\text{CWE1}}$. DRAM data is not updated.

During a read miss, the DIRTY bit will be checked before reading in new data from the DRAMs. If DIRTY=1, the

Note:

1. 128MB is the maximum DRAM size supported.

displaced data from the SRAMs is copied to the DRAMs before the line fill. In the case of a write miss, data will only be written to DRAM.

The CY82C597 also supports an 8-bit tag size (TAGA[7:0]) without a DIRTY bit. All lines are considered dirty. On a cache read miss, the line in the cache is automatically written back to memory before the new line in memory is read. In the case of a write miss, data will only be written to DRAM memory.

Write-through Operation

The CY82C597 also supports write-through cache operation. During a write hit, the CY82C597 writes data to both the SRAMs and the DRAMs. Additional wait states are required especially when a DRAM page miss occurs. For a write miss, data is written to DRAM memory only. Only the 8-bit tag configuration is supported in write-through mode.

The selection between write-through or write-back cache policies is controlled by bit 6 of register 11.

DMA/ISA Master Transactions

When a DMA/MASTER memory read hit occurs, data will be supplied from the cache SRAMs instead of the DRAMs. On a memory read miss, data is supplied by the DRAMs. In the case of a DMA/MASTER memory write hit cycle, data will be written into the DRAMs and SRAMs. A DMA/MASTER write miss cycle will only write data into the DRAMs.

Tag RAM/Data RAM Configurations

The CY82C597 supports 32KB, 64KB, 128KB, and 256KB cache sizes for the 386, and 64KB, 128KB, 256KB, 512KB, and 1MB cache sizes for the 486. In write-back mode, the CY82C597 combines the DIRTY RAM with the Tag RAM, thereby saving one SRAM for cache systems. The dirty bit can be replaced by a tag address in order to increase the cachable range. See Tables 3, 4, and 5. Dirty bit support vs. more cachable memory is controlled through bit 4 of control register 16.

Table 3. Tag RAM/Data RAM Requirements without a Dirty Bit

Cache Size	Tag RAM	Tag Address	Tag Field	Cachable Size ^[1]
32KB	2K x 8	A14 – A4	A22 – A15	8 MB
64KB	4K x 8	A15 – A4	A23 – A16	16 MB
128KB	8K x 8	A16 – A4	A24 – A17	32 MB
256KB	16K x 8	A17 – A4	A25 – A18	64 MB
512KB	32K x 8	A18 – A4	A26 – A19	128 MB
1MB	64K x 8	A19 – A4	A26 – A20	128 MB

7. Page Mode DRAM Controller
Introduction

A pure Page mode DRAM controller is used in this design. No Interleaving is required. The CY82C597 can support mixed DRAM sizes. The starting address of each DRAM bank is calculated by internal hardware. The user can configure DRAM memory from 1MB to 128MB, as long as the memory stays

continuous. The DRAM controller supports up to four banks of DRAM memory. Four RAS and four CAS signals (for three and four bank systems) or two RAS and four CAS signals (for one and two bank systems) are the allowed options. The DRAM controller also provides the multiplexed row and column addresses for the DRAMs. The address split is configurable, and the supported DRAM splits are given in the following tables.

DRAM Row/Column Address

The DRAM row address is listed as follows:

Address Split		DRAM Type	Row Address											
Row	Col.		MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9	MA10	MA11
9	9	256KB	A12	A13	A14	A15	A16	A17	A18	A19	A11	X	X	X
9	10	512KB	A12	A13	A14	A15	A16	A17	A18	A19	A20	X	X	X
10	10	1MB	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	X	X
11	9	1MB	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A11	X
12	8	1MB	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A11	A10
11	10	2MB	A22	A13	A14	A15	A16	A17	A18	A19	A20	A21	A12	X
12	9	2MB	A22	A13	A14	A15	A16	A17	A18	A19	A20	A21	A12	A11
11	11	4MB	A23	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	X
12	10	4MB	A23	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A12
16	6	4MB	A23	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	X
12	12	16MB	A23	A24	A14	A15	A16	A17	A18	A19	A20	A21	A22	A25

The DRAM column address is listed as follows: ^[6]

Address Split		DRAM TYPE	Column Address											
Row	Col.		MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9	MA10	MA11
9	9	256KB	$\bar{A}2$	$\bar{A}3$	$\bar{A}4$	$\bar{A}5$	$\bar{A}6$	$\bar{A}7$	$\bar{A}8$	$\bar{A}9$	$\bar{A}10$	X	X	X
9	10	512KB	$\bar{A}2$	$\bar{A}3$	$\bar{A}4$	$\bar{A}5$	$\bar{A}6$	$\bar{A}7$	$\bar{A}8$	$\bar{A}9$	$\bar{A}10$	$\bar{A}11$	X	X
10	10	1MB	$\bar{A}2$	$\bar{A}3$	$\bar{A}4$	$\bar{A}5$	$\bar{A}6$	$\bar{A}7$	$\bar{A}8$	$\bar{A}9$	$\bar{A}10$	$\bar{A}11$	X	X
11	9	1MB	$\bar{A}2$	$\bar{A}3$	$\bar{A}4$	$\bar{A}5$	$\bar{A}6$	$\bar{A}7$	$\bar{A}8$	$\bar{A}9$	$\bar{A}10$	X	X	X
12	8	1MB	$\bar{A}2$	$\bar{A}3$	$\bar{A}4$	$\bar{A}5$	$\bar{A}6$	$\bar{A}7$	$\bar{A}8$	$\bar{A}9$	X	X	X	X
11	10	2MB	$\bar{A}2$	$\bar{A}3$	$\bar{A}4$	$\bar{A}5$	$\bar{A}6$	$\bar{A}7$	$\bar{A}8$	$\bar{A}9$	$\bar{A}10$	$\bar{A}11$	X	X
12	9	2MB	$\bar{A}2$	$\bar{A}3$	$\bar{A}4$	$\bar{A}5$	$\bar{A}6$	$\bar{A}7$	$\bar{A}8$	$\bar{A}9$	$\bar{A}10$	X	X	X
11	11	4MB	$\bar{A}2$	$\bar{A}3$	$\bar{A}4$	$\bar{A}5$	$\bar{A}6$	$\bar{A}7$	$\bar{A}8$	$\bar{A}9$	$\bar{A}10$	$\bar{A}11$	$\bar{A}12$	X
12	10	4MB	$\bar{A}2$	$\bar{A}3$	$\bar{A}4$	$\bar{A}5$	$\bar{A}6$	$\bar{A}7$	$\bar{A}8$	$\bar{A}9$	$\bar{A}10$	$\bar{A}11$	X	X
16	6	4MB	$\bar{A}2$	$\bar{A}3$	$\bar{A}4$	$\bar{A}5$	$\bar{A}6$	$\bar{A}7$	$\bar{A}8$	$\bar{A}9$	$\bar{A}10$	$\bar{A}11$	$\bar{A}12$	X
12	12	16MB	$\bar{A}2$	$\bar{A}3$	$\bar{A}4$	$\bar{A}5$	$\bar{A}6$	$\bar{A}7$	$\bar{A}8$	$\bar{A}9$	$\bar{A}10$	$\bar{A}11$	$\bar{A}12$	$\bar{A}13$

Notes:

6. The column address lines are inverted from the CPU address.

16. Numerical Coprocessor Interface Logic

The CY82C597 supports the Weitek 4167 Numerical Coprocessor (486SX systems), the Weitek 3167, and the Intel 387 Numerical Coprocessor (386 systems) without any external logic.

For 486SX systems, INT13 will be asserted when either $\overline{\text{FERR}}$ or $\overline{\text{WTINTR}}$ is activated. As soon as the $\overline{\text{FERR}}$ is asserted, the interrupt service routine will handle the error and clear the interrupt by executing a dummy write to I/O port F0H. The $\overline{\text{IGNNE}}$ signal is also activated by writing to the I/O port F0H.

For 386 systems, $\overline{\text{BUSY386}}$ is asserted when $\overline{\text{BUSY387}}$ is active to signal the 386 that the coprocessor is currently executing an instruction. If $\overline{\text{BUSY387}}$ is active when $\overline{\text{ERR387}}$ is active, the $\overline{\text{BUSY387}}$ will be latched and IRQ will be generated. The latched $\overline{\text{BUSY387}}$ can be cleared by performing a write to I/O port F0H. If the Weitek 3167 is being used and the interrupt signal ($\overline{\text{WTINTR}}$) is active, IRQ will be asserted. The $\overline{\text{ERR386}}$ signal is asserted after system reset if a 387 is present. It will stay active until the first CPU cycle begins.

17. Keyboard Emulation Logic

I/O Port 60H and 64H are used to implement keyboard controller emulation. The keyboard emulation is enabled by programming register 10, bit 3 to a 0. When fast GA20 is enabled, writing DIH to Port 64H followed by DDH to Port 60H, A20 will be forced LOW in a 386 system. For a 486 system, the A20M pin should be connected to the 8042 and E386NGT functions as the A25 input. If the system is designed to support 32 MB of main memory or less, the E386NGT signal can be connected to the A20M signal on the 486 for fast GATEA20 operation.

The CY82C597 also performs fast RESET by intercepting the keyboard reset command sequence and performing the reset directly. The CY82C597 can be programmed to wait for a HALT instruction before asserting reset to the CPU.

18. Port B (61H), NMI, and Port 70H

When a parity error is detected by the CY82C597, an NMI will be generated to the CPU if NMI reporting is enabled. NMI reporting can be enabled by setting bit 7 of Port 70H to 0. The CY82C597 provides access to the Port B register defined for a PC/AT. The chart below illustrates the bit definition for Port B (61H):

Address	Bit	Access	Description
61H	7	Read Only	System memory parity check
	6	Read Only	I/O channel check
	5	Read Only	Timer 2 output
	4	Read Only	Refresh detection
	3	Read/Write	0: Enable I/O channel check 1: Disable I/O channel check
	2	Read/Write	0: Enable system memory parity check. 1: Disable system memory parity check
	1	Read/Write	Speaker data
	0	Read/Write	Timer 2 gate

19. Power Management Logic

The CY82C597 implements flexible power management logic. When used with the CY82C599 (for a full VESA/ISA/PCI system), most of the power management functions are performed by the CY82C599. The CY82C597 will only perform the SMM

memory mapping. All other power management functions in the CY82C597 are disabled. For VESA/ISA-only systems, the CY82C597 provides all of the chipset power management.

There are eleven event detectors and five user-programmable timers in the CY82C597 allowing it to support full hardware power management (for CPUs that do not support SMM, System Management Mode) and software power management (through SMM).

Monitored Events

The CY82C597 allows the following events to be monitored:

1. VESA master request
2. Keyboard command
3. Serial Port command
4. Parallel Port command
5. Hard Disk command
6. DMA/MASTER request from the ISA bus
7. Non-motherboard memory access
8. Video memory access
9. A specific I/O address
10. A specific memory range
11. A specific I/O range

When events are detected, the CY82C597 will transition to different power-down states.

Hardware Power Management

For hardware power management, the CY82C597 supports Full-speed/Stand-by/Suspend/Off states. In Stand-by state, the CY82C597 will assert the $\overline{\text{SLOWCLK}}$ signal that can be used by the system to slow down the CPU's clock frequency. In the Suspend state, the CY82C597 will assert the $\overline{\text{STOPCLK}}$ signal. $\overline{\text{STOPCLK}}$ can be used to stop the CPU's clock or turn off the monitor and other supported peripherals.

In the Full-speed state, the CY82C597 will monitor all stand-by events. Any monitored event will reset the stand-by timer. If no events occur within the period specified by the stand-by timer, the CY82C597 will enter the Stand-by state and assert the $\overline{\text{SLOWCLK}}$ signal. Once Stand-by state has been entered, the CY82C597 will monitor Suspend state events. If no event occurs within the period specified by the suspend timer, the CY82C597 will assert $\overline{\text{STOPCLK}}$ and enter the Suspend state. In the Suspend state, the assertion of $\overline{\text{STOPCLK}}$ can be used to stop the CPU's clock or power-down any supported peripherals. If any monitored event is detected, the CY82C597 will return to the Full-speed state and $\overline{\text{STOPCLK}}/\overline{\text{SLOWCLK}}$ will be deasserted.

Any interrupt will temporarily cause the $\overline{\text{STOPCLK}}$ signal (and optionally the $\overline{\text{SLOWCLK}}$ signal) to be deasserted (allowing the CPU to service the interrupt). If the interrupt timer expires before a monitored event occurs, the CY82C597 will automatically return to the power-down state it was in prior to the interrupt (with the appropriate signal asserted).



CY82C597 Control Registers

The control registers for the CY82C597 are defined in this section. The registers can be accessed through I/O Ports 22H and 23H. To access each register, the user must first write the index

number of the register into Port 22, which forces the internal decoding logic to point to the selected register. Data can be accessed by then reading/writing to/from Port 23.

Register 10: AT Bus Control, Index: 10

Bit	Function	Default
7	486 speed indicator: 0: 20/25 MHz 1: 33/40/50 MHz	0
6	Parity check disable: [7] 0: Enable parity checking 1: Disable parity checking	0
5	386 speed indicator: 0: 40 MHz 1: 33 MHz (or any speed below 33 MHz)	0
4	Reserved, BIOS should set to 1.	0
3	Fast Gate A20 Emulation Control (386 only): 0: Enable 1: Disable	0
2	Turbo speed control: 0: Enable turbo speed (high speed) 1: Enable low speed	0
1:0	ATCLK control: Bits 01: 486 system: (pin 4 tied to V _{CC} through a 51KΩ resistor) 00: CLK/4 01: CLK/6 10: CLK/8 11: CLK/5 Bits 01: 486 system: (pin 4 tied to V _{SS} through a 1KΩ resistor) 00: CLK/2 01: CLK/3 10: CLK/4 11: CLK/2.5 Bits 01: 386 system: 00: CLK/4 01: CLK/6 10: CLK/8 11: CLK/10	00

Notes:

7. If parity checking is disabled, the parity bits are used as VESA local bus request and grant signals (see pin description). If parity is required in the system, an external PAL must be used to control VESA

local arbitration signals (if bus mastership from the VESA slots is allowed).

Register 13: DRAM Wait State and Cachable Range Control, Index: 13^[13]

Bit	Function	Default
7:4	Bits: 7654 Range 0000: 0–128MB 0001: 0–8MB 0010: 0–16MB 0011: 0–24MB 0100: 0–32MB 0101: 0–40MB 0110: 0–48MB 0111: 0–56MB 1000: 0–64MB 1001: 0–72MB 1010: 0–80MB 1011: 0–88MB 1100: 0–96MB 1101: 0–104MB 1110: 0–112MB 1111: 0–128MB	0000
3	Reserved, BIOS should set to 1.	0
2	DRAM write wait states: 0: 1 wait state 1: 0 wait states	0
1:0	DRAM read wait states: Bits 10 # of wait states 00: 3 01: 2 10: 1 11: 0	00

Notes:

13. The CY82C597 will take care of the cachable range. Bits [7:4] are for custom memory configurations.

Shadowing Instructions

To shadow system BIOS (Block F), you must:

1. Set register 15, bit 6 to "0" to enable ROM access.
2. Read ROM data into the CPU register.
3. Set register 15, bit 6 to "1" to enable RAM access.
4. Set register 15, bit 7 to "0" to enable RAM write.
5. Write the data stored in the CPU register to RAM.
6. Go to step 1 if not done. Else, go to step 7.
7. Set register 15, bit 7 to "1" to enable shadow RAM read access and write protect it.

Shadowing on-board ROM is similar to shadowing system ROM. The following example is used to shadow Block C from on-board ROM:

1. Set register 15, bit 0 to "1" to enable ROM access.
2. Read ROM data into the CPU register.
3. Set register 15, bit 0 to "0" to enable RAM access.
4. Set register 15, bit 1 to "0" to enable RAM write.
5. Write the data stored in the CPU register to RAM.
6. Go to step 1 if not done. Else, go to step 7.
7. Set register 15, bit 1 to "1" to enable shadow RAM read access and write protect it.

Shadowing AT bus ROM is slightly different than shadowing on-board ROM. The following example is used to shadow Block C from AT bus ROM:

1. Set register 15, bit 0 to 0 to disable on-board ROM access.
2. Set register 15, bits 2, 3, 4, and 5 to 0 to disable RAM access. All access to Block C will go to the AT bus.
3. Read AT ROM data into CPU register.
4. Set register 15, bits 2, 3, 4, and 5 to 1 to enable RAM access.
5. Set register 15, bit 1 to 0 to enable RAM write.
6. Write the data stored in CPU register to RAM.
7. Go to step 1 if not done. Else, go to step 8.
8. Set register 15, bit 1 to 1 to enable shadow RAM read access and write protect it.

Register 19: Non-cachable Block 0 Starting Address and Size, Index: 19^[18]

Bit	Function	Default
7	Slow DRAM select: 0: Fast page mode DRAM supported. 1: Fast page mode DRAM not supported	0
6	486 Single bank SRAM select: 0: Support interleaved SRAMs (2 banks of SRAMs). 1: Support 1 bank of SRAMs. This is for 128KB cache using 32Kx8 SRAMs and 512KB cache using 128Kx8 SRAMs.	0
5	Reserved, BIOS should set to 0.	0
4	Non-cachable Block 0 control: 0: Disable. 1: Enable.	0
3:1	Non-cachable size Bits: 321 Size 000: 64KB 010: 128KB 100: 256KB 110: 512KB 001: 1MB 011: 2MB	000
0	Non-cachable/non-local Block 0 starting address A24.	0

Note:

18. For 64KB non-cachable size, the starting address is bound by A24–A16 from the configuration registers.
 For 128KB non-cachable size, the starting address is bound by A24–A17 from the configuration registers.
 For 256KB non-cachable size, the starting address is bound by A24–A18 from the configuration registers.
 For 512KB non-cachable size, the starting address is bound by A24–A19 from the configuration registers.
 For 1MB non-cachable size, the starting address is bound by A24–A20 from the configuration registers.
 For 2MB non-cachable size, the starting address is bound by A24–A21 from the configuration registers.

Please note that the non-cachable size is independent of cache size. The non-cachable starting address and non-cachable size are used to define an address range that will not be cached.

When Register 16, bit 2 is set to 1, the non-cachable block will be changed to a non-local block. All addresses within this block will not be on the motherboard, i.e., they will go to the AT bus or VESA bus.

For 386 systems, 32KB/128KB cache is fixed to 1 bank of SRAMs. 64KB/256KB is fixed to 2 banks of SRAMs. For 486 systems, 64KB/128KB/256KB/512KB/1MB can be either 1 or 2 banks of SRAMs.

Register 1C: Miscellaneous Control Register, Index: 1C

Bit	Function	Default
7	Bits 0: Symmetrical 4MB DRAM 1: Special 4MB DRAM with 16 row addresses and 6 column addresses	0
6	Bits 0: Symmetrical 4MB DRAM 1: Special 4MB DRAM with 12 row addresses and 10 column addresses	0
5	Bits 0: Normal mode (For 40/50 MHz systems, this bit should be set to 0) 1: Fast write at 25/33 MHz	0
4	Reserved, BIOS must set to 1.	0
3	Bits 0: Keyboard soft reset will not generate NPRST 1: Keyboard soft reset will generate NPRST	0
2	Reserved, BIOS should be set to 0.	0
1	Bits 0: ATCLK controlled by register 10, bit [1:0] 1: ATCLK fixed at 7.159 MHz	0
0	Bits 0: Normal mode (no additional IDLE AT CYCLES between AT command cycles) 1: Add one extra IDLE AT CYCLE between AT command cycles	0

Register 1D: Miscellaneous Control Register, Index: 1D

Bit	Function	Default
7	Bits 0: Normal mode (enable upper DRAM) 1: Upper 64KB or 1KB DRAM memory will be disabled	0
6	Bits 0: Upper 64K of DRAM will be disabled if bit 7=1 1: Upper 1K of DRAM will be disabled if bit 7=1	0
5	Reserved, BIOS should set to 0.	0
4	Bits 0: Add one SYSCLK cycle of delay before AT cycle detection 1: Add two SYSCLK cycles of delay before AT cycle detection	0
3	Fast DRAM write, BIOS should set to 1.	0
2	Reserved, BIOS should be set to 0.	0
1	Bits 0: AT cycle detection at end of T2 if register 11, bit 7=1 (2111 mode) AT cycle detection at end of second T2 if register 11, bit 7=0 (3111/3222 mode) 1: Add extra delay on AT cycle detection, extra delay based on register 1D, bit 4 setting	0
0	Reserved, BIOS should set to 0.	0

Register 60: I/O Address (for Address Detection), Index: 60

Bit	Function	Default
7:0	Bits 7:0 I/O Address to be Monitored	00000000

Register 61: I/O Address Detection and Miscellaneous Control, Index: 61

Bit	Function	Default
7	Bits 0: VESA/AT only mode (82C597 stand-alone) 1: 82C599 PCI bridge is present in the system	0
6	Bits 0: NMI output is non three-state 1: NMI output is three-state	0
5	Reserved	0
4	Reserved	0
3	Bits 0: Disable I/O address detection 1: Enable I/O address detection	0
2	Reserved, must be 0.	0
1:0	I/O address (9:8).	00

Register 62: Suspend Timer and Interrupt Timer Control, Index: 62

Bit	Function	Default
7:4	Bits (Suspend Timer Period) 0000: 3.8 min. 0001: 7.5 min. 0010: 15 min. 0011: 30 mins. 0100: 60 mins. 0101: 120 mins. 0110: 240 mins. 0111: 480 mins. 0000: 1 sec. 1001: 1.8 sec. 1010: 3.5 sec. 1011: 7 sec. 1100: 14 sec. 1101: 28 sec. 1110: 56 sec. 1111: 2 min.	0000
3:0	Bits (Interrupt Timer Period) 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 54 μ sec. 0110: 107 μ sec. 0111: 215 μ sec. 0000: 430 μ sec. 1001: 860 μ sec. 1010: 1.7 msec. 1011: 3.4 msec. 1100: 7 msec. 1101: 14 msec. 1110: 28 msec. 1111: 55 msec.	0000

Hardware Power-down mode allows $\overline{\text{STOPCLK}}$ and $\overline{\text{SLOWCLK}}$ mode will use System Management Mode (SMM) subroutines to be controlled by the 82C597 hardware. Software Power-down implement power-down control.

Register 64: Power-Down Mode Control, Index: 64

Bit	Function	Default
7	Bits Software initial $\overline{\text{SMI}}$ 0: Normal 1: Writing a 1 to this bit will generate an $\overline{\text{SMI}}$ to CPU. After a 1 is written, software should write a 0 to this bit.	0
6	Bits $\overline{\text{SMI}}$ inactive control 0: Normal 1: Writing a 1 to this bit will deassert the $\overline{\text{SMI}}$ signal. This is the only way to cause the 82C597 to deassert $\overline{\text{SMI}}$. After a 1 is written, 0 should be written to this bit.	0
5	Bits $\overline{\text{STOPCLK}}$ Active Control 0: Normal 1: Writing a 1 to this bit will assert $\overline{\text{STOPCLK}}$. Software should subsequently write a 0 to this bit to allow $\overline{\text{STOPCLK}}$ to be deasserted.	0
4	Bits Software $\overline{\text{STOPCLK}}$ Inactive Control 0: Normal 1: Writing a 1 will deassert $\overline{\text{STOPCLK}}$. Software should subsequently write a 0 to this bit to allow $\overline{\text{STOPCLK}}$ to be asserted.	0
3	Bits Software $\overline{\text{SLOWCLK}}$ Active Control 0: Normal 1: Writing a 1 will assert $\overline{\text{SLOWCLK}}$. Software should subsequently write a 0 to this bit to allow $\overline{\text{SLOWCLK}}$ to be deasserted.	0
2	Bits Software $\overline{\text{SLOWCLK}}$ Inactive Control 0: Normal 1: Writing a 1 will deassert $\overline{\text{SLOWCLK}}$. Software should subsequently write a 0 to this bit to allow $\overline{\text{SLOWCLK}}$ to be asserted.	0
1	Bits Suspend Timer Control 0: Enable suspend timer (default) 1: Disable suspend timer The 82C597 allows a second Suspend mode to be started after current suspend timer has reached its terminal count (i.e. When the current suspend timer expires, it will assert $\overline{\text{SMI}}$.) Within the $\overline{\text{SMI}}$ subroutine, the suspend timer can be disabled and the suspend timer reenable. After the new terminal count has been reached, the 82C597 will initiate another $\overline{\text{SMI}}$.	0
0	Bits Disable Software Reset Mask 0: Normal 1: Force 82C597 to activate pin 153. This bit should be set to 1, then set to 0 before leaving the SMI subroutine.	0

Register 65: Power Management Control, Index: 65

Bit	Function	Default
7	Bits 0: Disable $\overline{\text{SMIACT}}/\overline{\text{SMADS}}$ input signal 1: Enable $\overline{\text{SMIACT}}/\overline{\text{SMADS}}$ input signal	0
6	Bits 0: INTEL SMM mode 1: Cyrix/AMD SMM mode	0
5	Bits 0: Disable quick power-down mode 1: Enable quick power-down mode when power-down key is pushed.	0
4	Reserved, must be 0	0
3:0	Reserved	0000

Register 6A: 82C597 Status Register, Index: 6A

Read Cycle:	Set A	Set B
Bit 7=1	SMI caused by start of stand-by mode	SMI caused by timer 5 reaching its terminal count
Bit 6=1	SMI caused by end of stand-by mode	SMI caused by timer 5 reset by an event
Bit 5=1	SMI caused by suspend timer reaching its terminal count	82C597 is in power-down mode (stand-by or suspend mode)
Bit 4=1	SMI caused by register 64, bit 7	82C597 is in suspend mode. Once in suspend mode, this bit will stay 1 unless any suspend event becomes active, or power-down mode is disabled
Bit 3=1	SMI caused by timer 3 reaching its terminal count	STOPCLK pin is active
Bit 2=1	SMI caused by timer 3 reset by an event	SLOWCLK pin is active
Bit 1=1	SMI caused by timer 4 reaching its terminal count	Suspend timer has reached its terminal count. It will be 0 if register 64, bit 1 is set to 1 later
Bit 0=1	SMI caused by timer 4 reset by an event	SMI pin is active

The CY82C597 has two status registers (16 bits total) that can be read through register 6A. Writing a 0 into bit 7 will cause A status set to be read on a read cycle. Writing a 1 into bit 7 will cause B status set to be read on a read cycle.

Register 6A contains the source of an $\overline{\text{SMI}}$ and some internal status. The status can be used to power-down/power-up individual system devices (monitor, CPU, hard disk, etc.).

Register 6B: DRAM Bank 2/3 Control, Index: 6B

Bit	Function	Default
7	Reserved	0
6:4	Bits 000: Disable Bank 3 001: Bank 3 is 256KB 010: Bank 3 is 1MB 011: Bank 3 is 4MB 100: Reserved 101: Bank 3 is 512KB 110: Bank 3 is 16MB 111: Bank 3 is 2MB	000
3	Bits 0: Disable Bank 2 and 3 1: Enable Bank 2 and 3	0
2:0	Bits 000: Disable Bank 2 001: Bank 2 is 256KB 010: Bank 2 is 1MB 011: Bank 2 is 4MB 100: Reserved 101: Bank 2 is 512KB 110: Bank 2 is 16MB 111: Bank 2 is 2MB	000

Register 6E: Shadow RAM Block D, C Control, Index: 6E

Bit	Function	Default
7	Register 15, Bit 1 control (Block C RAM R/W control): Bits 0: Enable Register 15, Bit 1 1: Disable Register 15, Bit 1 (Replaced by Register 6E, Bit 6)	0
6	Block C RAM enable control (see Bit 7): Bits 0: Read or Write 1: Read only	0
5	Shadow RAM at DC000H–DFFFFH control: Bits 0: Disable. Will access AT Bus memory 1: Enable.	0
4	Shadow RAM at D8000H–DBFFFH control: Bits 0: Disable. Will access AT Bus memory 1: Enable.	0
3	Shadow RAM at D4000H–D7FFFH control: Bits 0: Disable. Will access AT Bus memory 1: Enable.	0
2	Shadow RAM at D0000H–D3FFFH control: Bits 0: Disable. Will access AT Bus memory 1: Enable.	0
1	Block D RAM access control (D0000H–DFFFFH): Bits 0: Read or Write 1: Read only	0
0	Block D RAM/ROM control: Bits 0: Access RAM. For those disabled RAM, access will go to AT Bus memory. 1: Access on board ROM.	0

Register 71: Timer 3 Event Detection Control, Index: 71

Bit	Function	Default
7	Bits 0: Disable key-board event detection 1: Enable key-board event detection	0
6	Bits 0: Disable serial port event detection 1: Enable serial port event detection	0
5	Bits 0: Disable parallel port event detection 1: Enable parallel port event detection	0
4	Bits 0: Disable hard disk event detection 1: Enable hard disk event detection	0
3	Bits 0: Disable DMA/ISA master event detection 1: Enable DMA/ISA master event detection	0
2	Bits 0: Disable non-motherboard memory event detection 1: Enable non-motherboard memory event detection	0
1	Reserved	0
0	Bits 0: Disable video memory (Block A,B) event detection 1: Enable video memory (Block A,B) event detection	0

Register 72: Timer 3 Control, Index: 72

Bit	Function	Default
7:4	Bits Terminal Time 0000: 1 sec. 0001: 1.8 sec 0010: 3.5 sec 0011: 7 sec. 0100: 14 sec. 0101: 28 sec. 0110: 56 sec. 0111: 2 min. 1000: 3.8 min. 1001: 7.5 min. 1010: 15 min. 1011: 30 min. 1100: 60 min. 1101: 120 min. 1110: 240 min. 1111: 480 min.	0
3	Bits 0: Disable timer 3 1: Enable timer 3	0
2	Bits 0: Disable special memory I/O event detection (please see register 66, 67, and 68) 1: Enable special memory I/O event detection	0
1	Bits 0: Disable I/O event detection (please see registers 60 and 61) 1: Enable I/O event detection	0
0	Bits 0: Disable VESA master event detection 1: Enable VESA master event detection	0

Register 75: Timer 5 Event Detection Control, Index: 75

Bit	Function	Default
7	Bits 0: Disable key-board event detection 1: Enable key-board event detection	0
6	Bits 0: Disable serial port event detection 1: Enable serial port event detection	0
5	Bits 0: Disable parallel port event detection 1: Enable parallel port event detection	0
4	Bits 0: Disable hard disk event detection 1: Enable hard disk event detection	0
3	Bits 0: Disable DMA/ISA master event detection 1: Enable DMA/ISA master event detection	0
2	Bits 0: Disable non-motherboard memory event detection 1: Enable non-motherboard memory event detection	0
1	Reserved	0
0	Bits 0: Disable video memory (Block A,B) event detection 1: Enable video memory (Block A,B) event detection	0

Register 76: Timer 5 Control, Index: 76

Bit	Function	Default
7:4	Bits Terminal Time 0000: 1 sec. 0001: 1.8 sec 0010: 3.5 sec 0011: 7 sec. 0100: 14 sec. 0101: 28 sec. 0110: 56 sec. 0111: 2 min. 1000: 3.8 min. 1001: 7.5 min. 1010: 15 min. 1011: 30 min. 1100: 60 min. 1101: 120 min. 1110: 240 min. 1111: 480 min.	0000
3	Bits 0: Disable timer 5 1: Enable timer 5	0
2	Bits 0: Disable special memory I/O event detection (please see register 66, 67, and 68) 1: Enable special memory I/O event detection	0
1	Bits 0: Disable I/O event detection (Please see register 60, 61) 1: Enable I/O event detection	0
0	Bits 0: Disable VESA master event detection 1: Enable VESA master event detection	0

Register 79: Non-Cachable Block 1 Starting Address and Size, Index: 79^[24]

Bit	Function	Default
7	Non-cachable/non-local Block 1 starting address A26.	0
6	Non-cachable/non-local Block 1 starting address A25.	0
5	Non-cachable Block 1 dual Functions control: 0: For non-cachable Block 1: For non-local memory Block	0
4	Non-cachable non-local Block 1 control: 0: Disable. 1: Enable.	0
3:1	Non-cachable size Bits 321 Size 000: 64KB 010: 128KB 100: 256KB 110: 512KB 001: 1MB 011: 2MB	000
0	Non-cachable/non-local Block 1 starting address A24.	0

Register 7B: Miscellaneous Control Register, Index: 7B

Bit	Function	Default
7	Reserved	0
6	Reserved	0
5	1: Enable Non-turbo speed set-up 0: Disable Non-turbo speed set-up	0
4	1: Non-turbo speed 0: Normal speed	0
3	1: Disable OSC119 output 0: Enable OSC119 output	0
2	1: Enable 0 ws input 0: Disable 0 ws input	0
1:0	Reserved	00

Register 7C: Reserved, Index: 7C

Bit	Function	Default
7:4	Not implemented	0
3	Reserved	0
2	Reserved, BIOS shall set to 1	0
1	Reserved, BIOS shall set to 1	0
0	Reserved	0

Note:

24. For 64KB non-cachable size, the starting address is bound by A24–A16 from the configuration registers.
 For 128KB non-cachable size, the starting address is bound by A24–A17 from the configuration registers.
 For 256KB non-cachable size, the starting address is bound by A24–A18 from the configuration registers.
 For 512KB non-cachable size, the starting address is bound by A24–A19 from the configuration registers.
 For 1MB non-cachable size, the starting address is bound by A24–A20 from the configuration registers.
 For 2MB non-cachable size, the starting address is bound by A24–A21 from the configuration registers.

Please note that the non-cachable size is independent of cache size. The non-cachable starting address and non-cachable size are used to define an address range that will not be cached.

When Register 79, bit 4 is set to 1, the non-cachable block will be changed to a non-local block. All addresses within this block will not be on the motherboard, i.e., they will go to the AT bus, VESA bus, or PCI bus.

CPU Control

Name	I/O	Pin Number	Description
A31	I	32	CPU address line 31.
A[24:21]	I	33–36	CPU address lines [24:21].
A20	I/O	37	CPU address line 20. Output during DMA/MASTER cycles for 386 systems.
A19	I	38	CPU address line 19.
A18	I	49	CPU address line 18.
A17	I	51	CPU address line 17.
A[16:2]	I/O	52–66	CPU address lines [16:2]. Outputs during DMA/MASTER cycles.
BE[3:0]	I/O	28–31	Byte enable [3:0]. Inputs during CPU cycles. Outputs during DMA/MASTER.
ADS	I/O	27	CPU address strobe. Output during DMA/MASTER accesses on the VESA local bus.
MIO	I/O	23	CPU memory I/O cycle status. Output during DMA/MASTER accesses on the VESA local bus cycles.
DC/ADSTB	I	22	This pin is the CPU data/code status input during CPU cycles and the ADSTB signal during DMA cycles.
WR	I/O	24	CPU write/read status. Output during DMA/MASTER accesses on VESA local bus.
CPURDY	I/O	18	Ready output to terminate CPU cycle. During local bus/numerical processor cycles, the CY82C597 monitors this signal to see when the cycle has ended.
D[31:18]	I/O	86–99	CPU data bus for read/write data.
D[17:16]	I/O	102–103	CPU data bus for read/write data.
CQ[15:10]	I/O	48–43	Contaq bus or CQ bus [15:10]. The CQ bus sits between the CPU data bus and the AT SD bus. Used also as TAGA[7:2].
CQ[9:8]	I/O	40–39	CQ bus [9:8]. Used also as TAGA[1:0].
CQ[7:3]	I/O	75–79	CQ bus [7:3].
CQ[2:0]	I/O	83–85	CQ bus [2:0].
NMI	O	11	Non-maskable interrupt output to the CPU. When active, it indicates the CY82C597 has detected either a local memory or AT memory parity error.

Bus Arbitration

Name	I/O	Pin Number	Description
DMAHRQ	I	135	DMA hold request from the 83C206.
HOLD	O	16	Hold request to the CPU. Hold goes active due to a refresh request or a de-turbo request.
HLDA	I	25	Hold acknowledge from the CPU.
HLDAOUT	O	132	DMA/MASTER cycle hold acknowledge output to the 83C206. After receiving this signal, the DMA/MASTER can begin its cycle.
REFSH	I/O	154	REFRESH, an active LOW signal. An output to the AT bus during non-master cycles. An input during MASTER cycles.

DRAM Control (continued)

Name	I/O	Pin Number	Description
LIMCS	O	152	Indicates the current address is below 1 MB.

Cache Control

Name	I/O	Pin Number	Description
CRD0	O	67	Cache read for the even bank of SRAMs. Connected to \overline{OE} of Bank 0 cache data SRAMs.
CRD1	O	68	Cache read for the odd bank of SRAMs. Connected to \overline{OE} of Bank 1 cache data SRAMs.
CWE0	O	71	Cache write enable for the even bank of SRAMs.
CWE1	O	72	Cache write enable for the odd bank of SRAMs.
TOGA2	O	73	A dual function pin. For 386 systems, it is used to toggle CPU address A2 during cache accesses. For 486 systems with 1 bank of SRAMs, it is address 2 to bank 0. For 486 systems with 2 banks of SRAMs, it is address 3 input to bank 0.
TOGA3	O	74	A dual function pin. For 386 systems, it is used to toggle CPU address A3 during cache accesses. For 486 systems with 1 bank of SRAM, it is address 3 to bank 0. For 486 systems with 2 banks of SRAMs, it is address 3 input to bank 1.
TAGWT	O	42	Tag RAM write enable, active LOW. It is active during a cache write hit or cache move in cycle.
TAGEN	O	41	An active LOW signal. When active, it will enable the CY82C597 to read/write the Tag RAM.
XA20EA	I/O	10	This is a dual function pin. For 486 systems, it is \overline{EADS} to invalidate a 486 internal cache line. It is active during DMA/MASTER memory write hit cycles. For 386 systems, the CPU is from CYRIX, this pin is the \overline{EADS} output to invalidate the CPU's cache line during DMA/MASTER memory write cycles. If Intel or AMD, this pin the SA20 output or input for DMA/MASTER cycles.
A25/AEN8	I/O	15	This is the CPU A25 input signal during CPU cycles and the $\overline{AEN8}$ input signal during DMA cycles.
KEN	O	17	\overline{KEN} to the 486 to indicate that the cycle is cachable. It can also be connected to C&T 38605 and CYRIX CPU \overline{KEN} pins making an external PAL unnecessary.
RQ3BRDY	I/O	19	A dual function pin. For 486 systems, it is an I/O pin, \overline{BRDY} . During VESA local cycles, it is an input that monitors \overline{BRDY} from the local device and determines when the cycle has terminated. During local memory cycles, it is an output that terminates the burst transfer. For 386 systems, it is an output connected to PEREQ of the 386.
RQ387BL	I	26	A dual function pin. For 486 systems, it is an input signal (\overline{BLAST}) from the 486. When active, it tells the CY82C597 that the next cycle will be the last burst cycle. For 386 systems, it is an input from the 387 (PRQ387) that requests a data operand to be transferred to/from memory by the 386.

AT Control

Name	I/O	Pin Number	Description
XA0	I/O	144	System address line 0. It is an input during MASTER and 8 bit DMA cycles, otherwise it is an output.
XA1	I/O	145	System address line 1. It is an input during DMA/MASTER cycles, otherwise it is an output.
MEMR	I/O	141	AT memory read command. It is an input during DMA/MASTER cycles, otherwise it is an output.
MEMW	I/O	140	AT memory write command. It is an input during DMA/MASTER cycles, otherwise it is an output.

AT Control (continued)

Name	I/O	Pin Number	Description
LDBE	O	82	An active LOW system data bus enable signal to turn on/off the bidirectional buffer between D[15:0] bus and CQ[15:0] bus.
SMIMASK/LDIR	I/O	112	In 597 mode, this pin is an output that controls the Data bus to CQ bus buffer direction. In 597 PCI mode, this pin is an input that masks out SMI generation during the reset period.

Ground and V_{CC}

Name	I/O	Pin Number	Description
GND	I	3, 21, 50, 70, 81, 101, 130, and 150	Ground
V _{CC}	I	2, 20, 69, 100, and 121	+5V

CY82C597 DC Characteristics
Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage +6.5 V
 Ambient Operating Temperature -25°C to +70°C

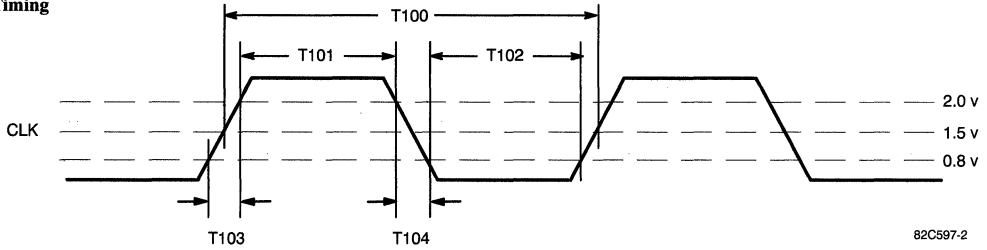
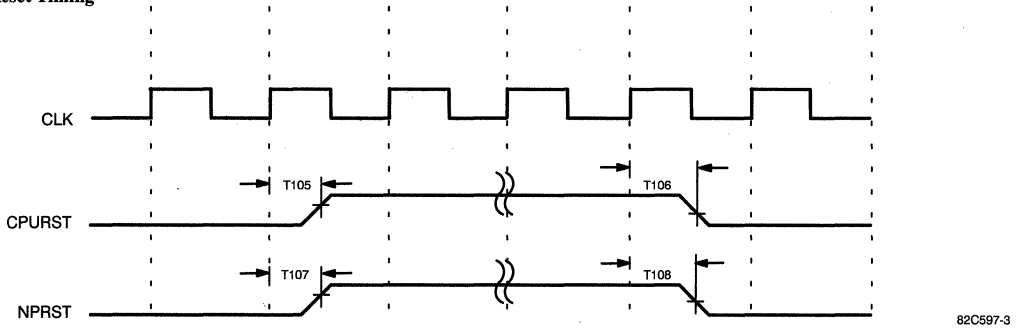
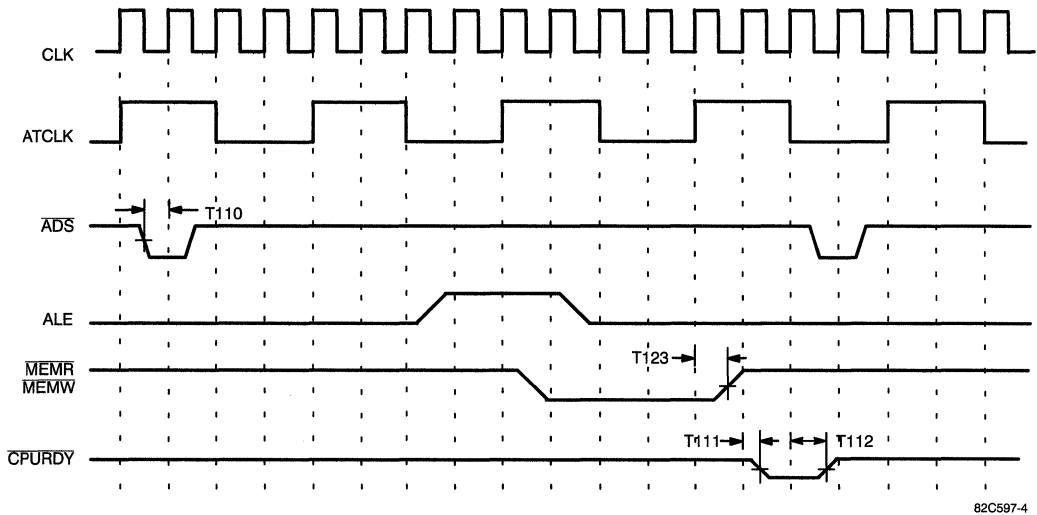
Ambient Storage Temperature -40°C to 125°C
 DC Voltage Applied to Outputs -0.5V to +5.5V
 DC Input Voltage -0.5V to +5.5V

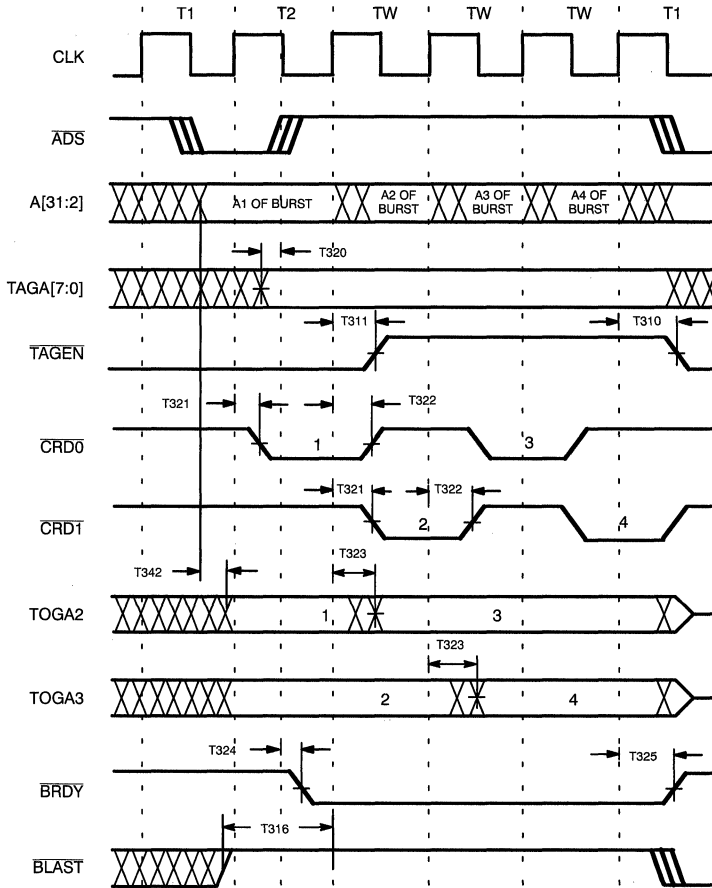
Electrical Characteristics Over the Operating Range (0°C to 70°C, V_{CC} = +5V ± 5%)

Parameter	Description	CY82C597		Unit
		Min.	Max.	
V _{IL}	Input LOW Voltage		0.8	V
V _{IH}	Input HIGH Voltage	2.0		V
V _{OL}	Output LOW Voltage		0.4	V
V _{OH}	Output HIGH Voltage	2.4		V
I _{IL}	Input Leakage Current		10	μA
I _{OZ}	Three-state Leakage Current		10	μA
C _{IN}	Input Capacitance		20	pF
C _{OUT}	Output Capacitance		20	pF
I _{CC}	Power Supply Current	33 MHz	150	mA
		50 MHz	200	mA

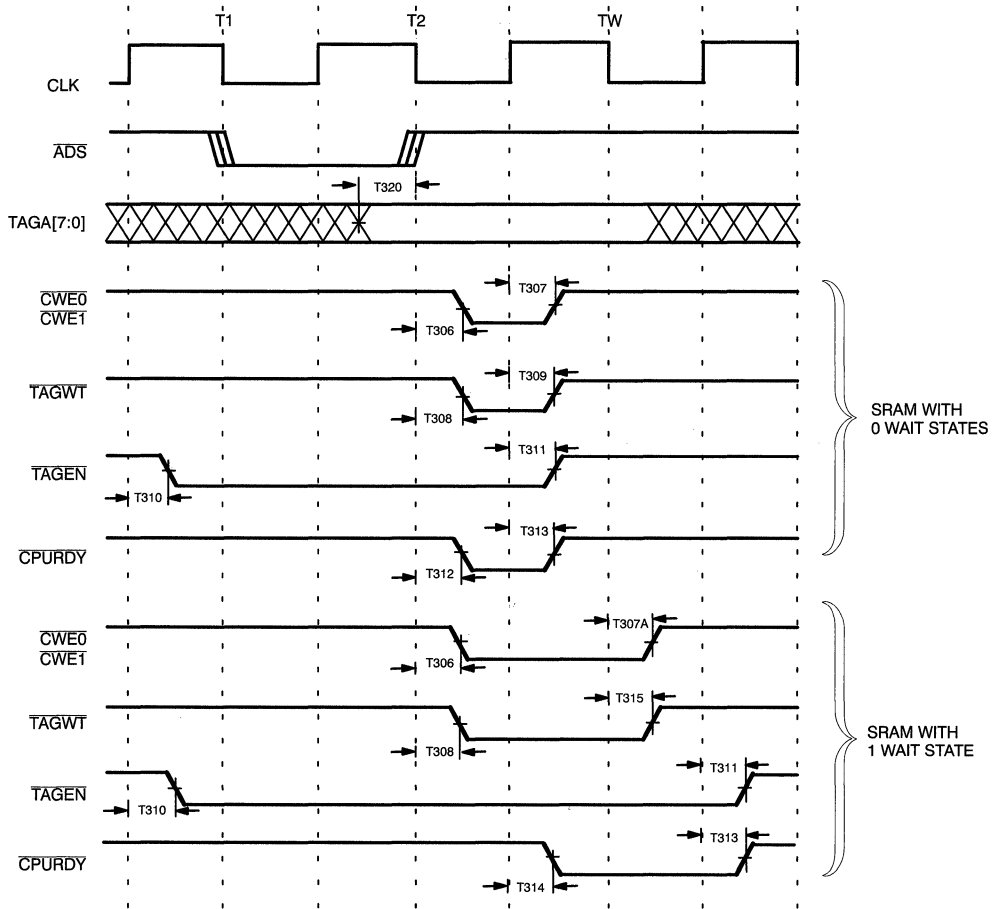
Switching Characteristics (continued)

Parameter	Description	CY82C597		Unit
		Min.	Max.	
T320	TAGA[7:0] set-up time to CLK LOW	15		ns
T321	CRD active delay from CLK HIGH	5	15	ns
T322	CRD inactive delay from CLK HIGH	6	13	ns
T323	TOGA2/TOGA3 delay from CLK HIGH	3	15	ns
T324	BRDY active delay from CLK LOW	4	15	ns
T325	BRDY inactive delay from CLK HIGH	4	13	ns
T330	CLK HIGH to DWROMKB active delay	5	18	ns
T331	CLK HIGH to DWROMKB inactive delay	4	14	ns
T332	CLK LOW to CAS active delay	6	18	ns
T333	CLK LOW to CAS inactive delay	4	15	ns
T334	CLK HIGH to CAS active delay	6	18	ns
T335	CLK HIGH to CAS inactive delay	4	17	ns
T336	A[31:2] to MA[10:0] delay	5	18	ns
T337	CLK HIGH to RAS inactive delay	5	20	ns
T338	CLK HIGH to RAS active delay	5	18	ns
T339	CLK HIGH to MA[10:0] delay	5	18	ns
T340	CLK HIGH to CRD active delay	4	15	ns
T341	CLK LOW to CRD inactive delay	4	13	ns
T342	A[31:3] to TOGA2/TOGA3 delay	5	16	ns
T343	CLK HIGH to TOGA2/TOGA3 valid delay	5	16	ns
T344	CLK HIGH to CPURDY active delay	4	16	ns
T345	CLK HIGH to CPURDY inactive delay	4	14	ns
T346	CLK LOW to TAGWT active delay	4	14	ns
T347	CLK LOW to TAGWT inactive delay	4	14	ns
T348	CLK LOW to CWE active delay	5	15	ns
T349	CLK LOW to CWE inactive	4	13	ns
T350	CLK LOW to TAGEN active		18	ns
T351	CLK LOW to CQ[15:8]		18	ns
DMA/MASTER TIMING				
T360	COMMAND active to RAS active delay	9	25	ns
T361	COMMAND inactive to RAS inactive	9	25	ns
T362	CLK HIGH to MA[10:0] delay	5	18	ns
T363	CLK HIGH to CAS active delay	5	20	ns
T364	COMMAND inactive to CAS inactive delay	5	22	ns
T365	COMMAND active CRD active delay	5	16	ns
T366	COMMAND inactive to CRD inactive delay	6	18	ns
T367	COMMAND active to DWROMKB active delay	5	20	ns
T368	COMMAND inactive to DWROMKB inactive	5	18	ns

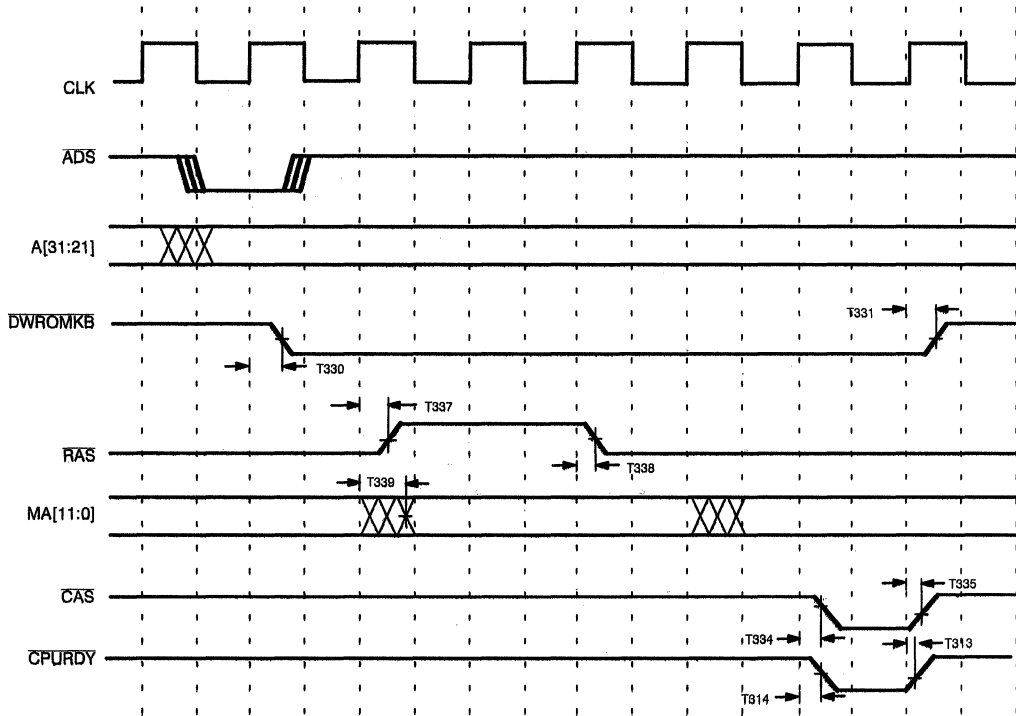
Switching Waveforms
Clock Timing

Reset Timing

AT Cycle Timing


Switching Waveforms (continued)
486 Cache Read Hit (2-1-1-1 Burst Mode), 2 Banks of Cache, Interleaved


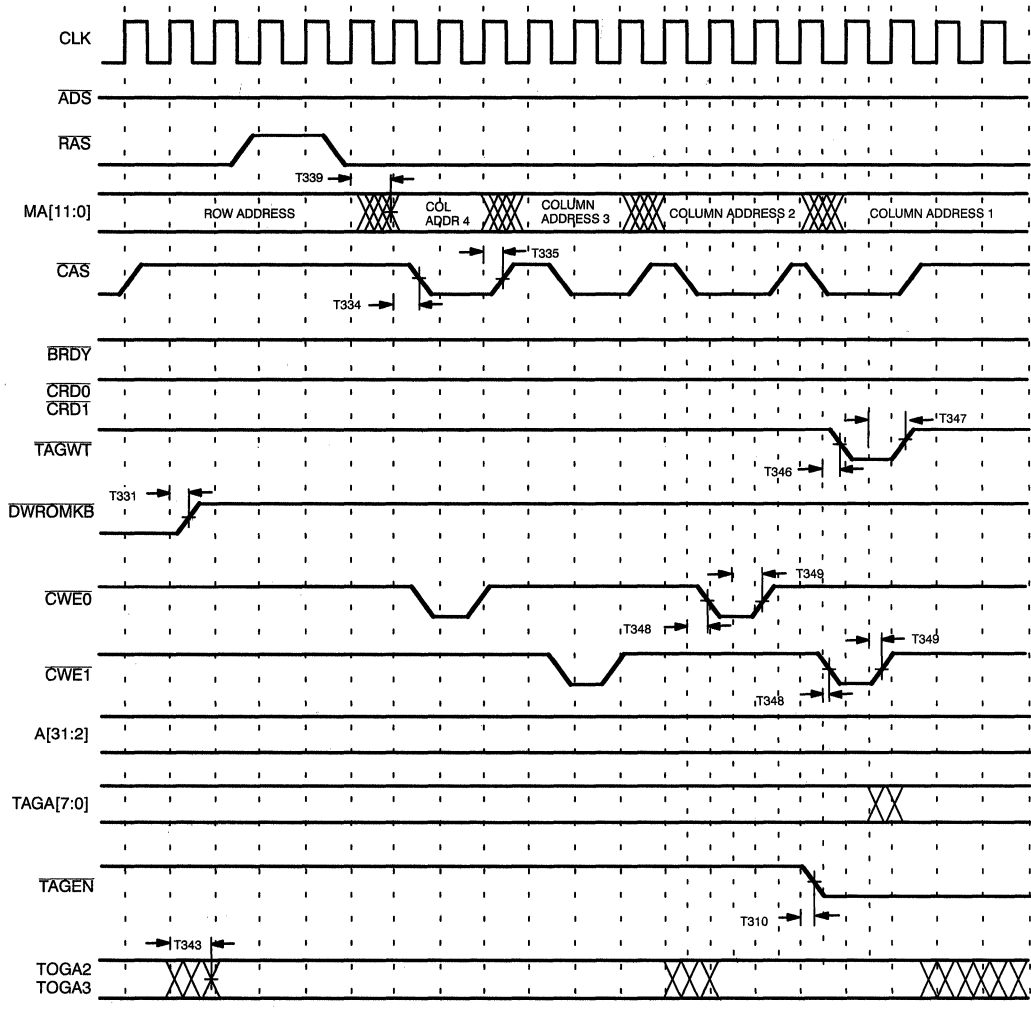
82C597-7

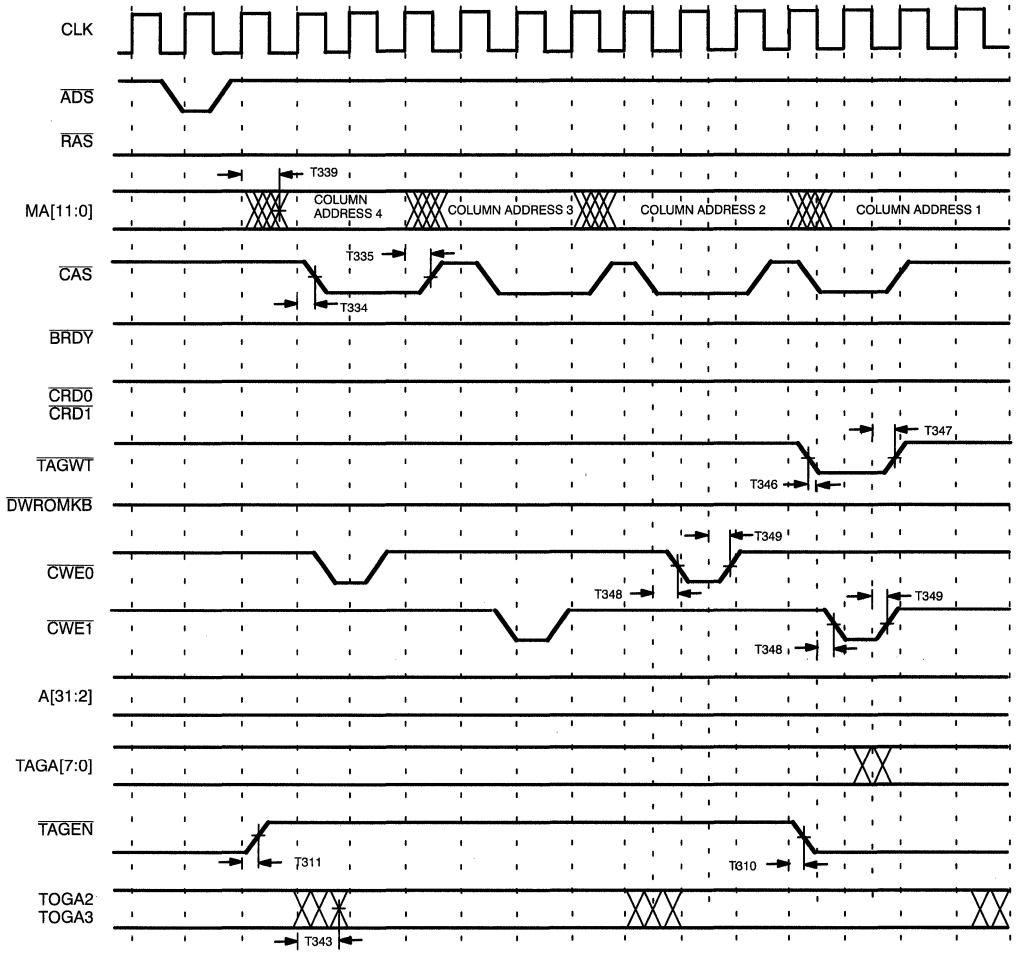
Switching Waveforms (continued)
Cache Write Hit Cycle (Write-Back)


82C597-9

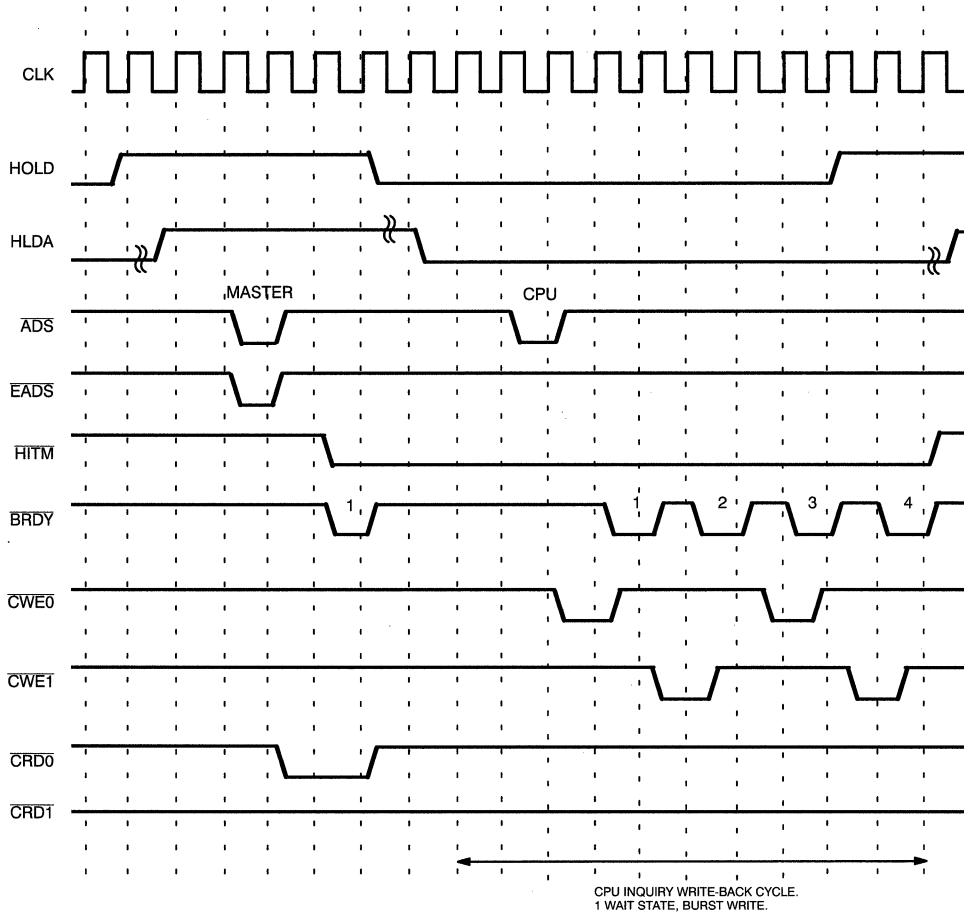
Switching Waveforms (continued)
Cache Write Miss, Page Miss Cycle


82C597-11

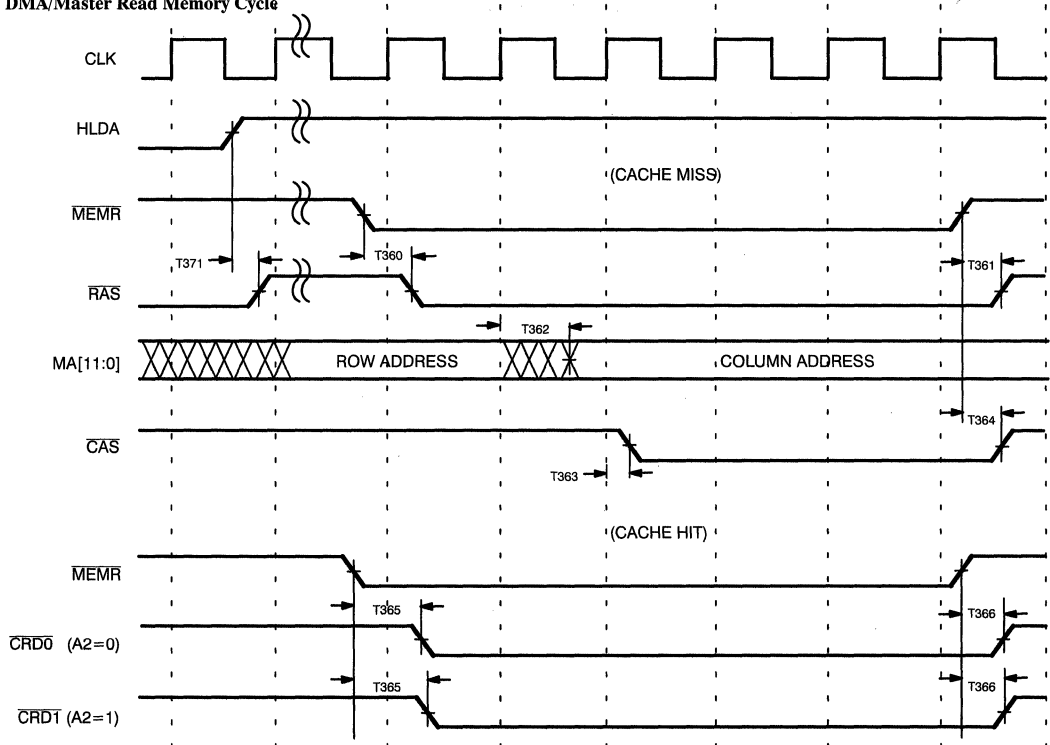
Switching Waveforms (continued)
Cache Burst Read Miss (2-1-1-1 Mode), Page Miss, Dirty = 1, DRAM R1WT Cycle (Page 2 of 3)


Switching Waveforms (continued)
Cache Burst Read Miss (2-1-1-1 Mode), Page Hit, Dirty = 0, DRAM R1WT Cycle (Page 1 of 2)


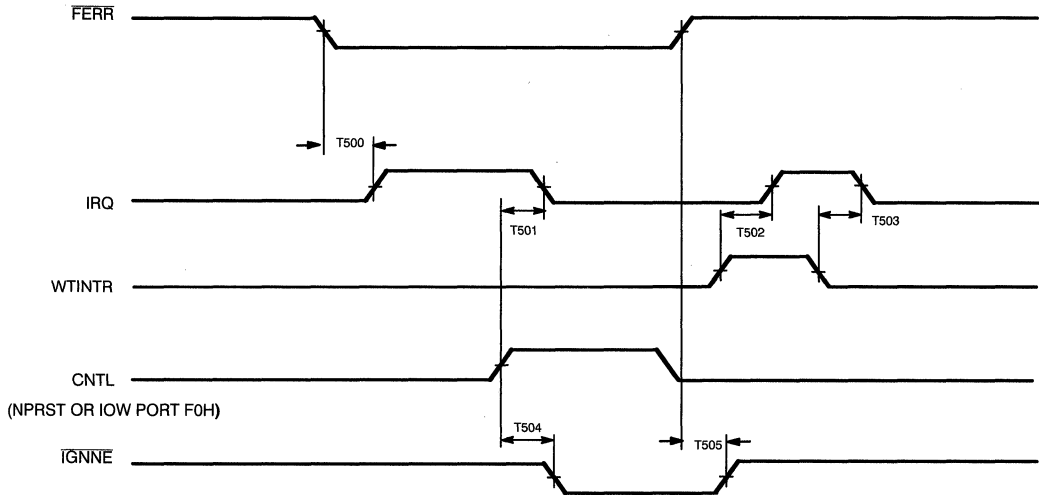
82C597-15

Switching Waveforms (continued)
VESA/PCI Master Read Memory Cycle with Inquiry Hit and Dirty ($\overline{\text{HITM}}=0$) (Part 1 of 2)


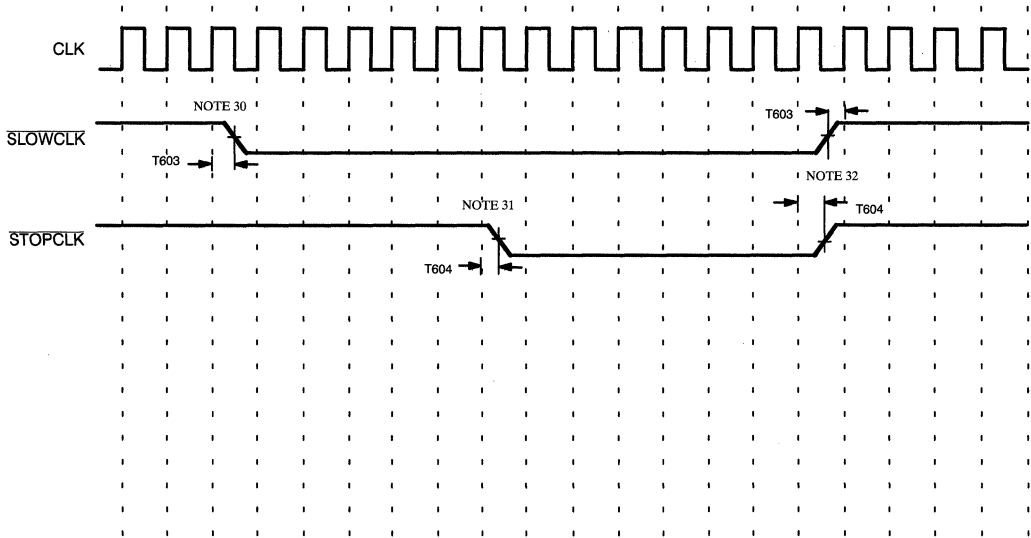
82C597-17

Switching Waveforms (continued)
DMA/Master Read Memory Cycle


82C597-19

Switching Waveforms (continued)
Numerical Coprocessor Interface Timing


82C597-21

Switching Waveforms (continued)
Hardware Power-Down


82C597-22

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY82C597-NC	N160	160-Lead Plastic Quad Flatpack	Commercial

Notes:

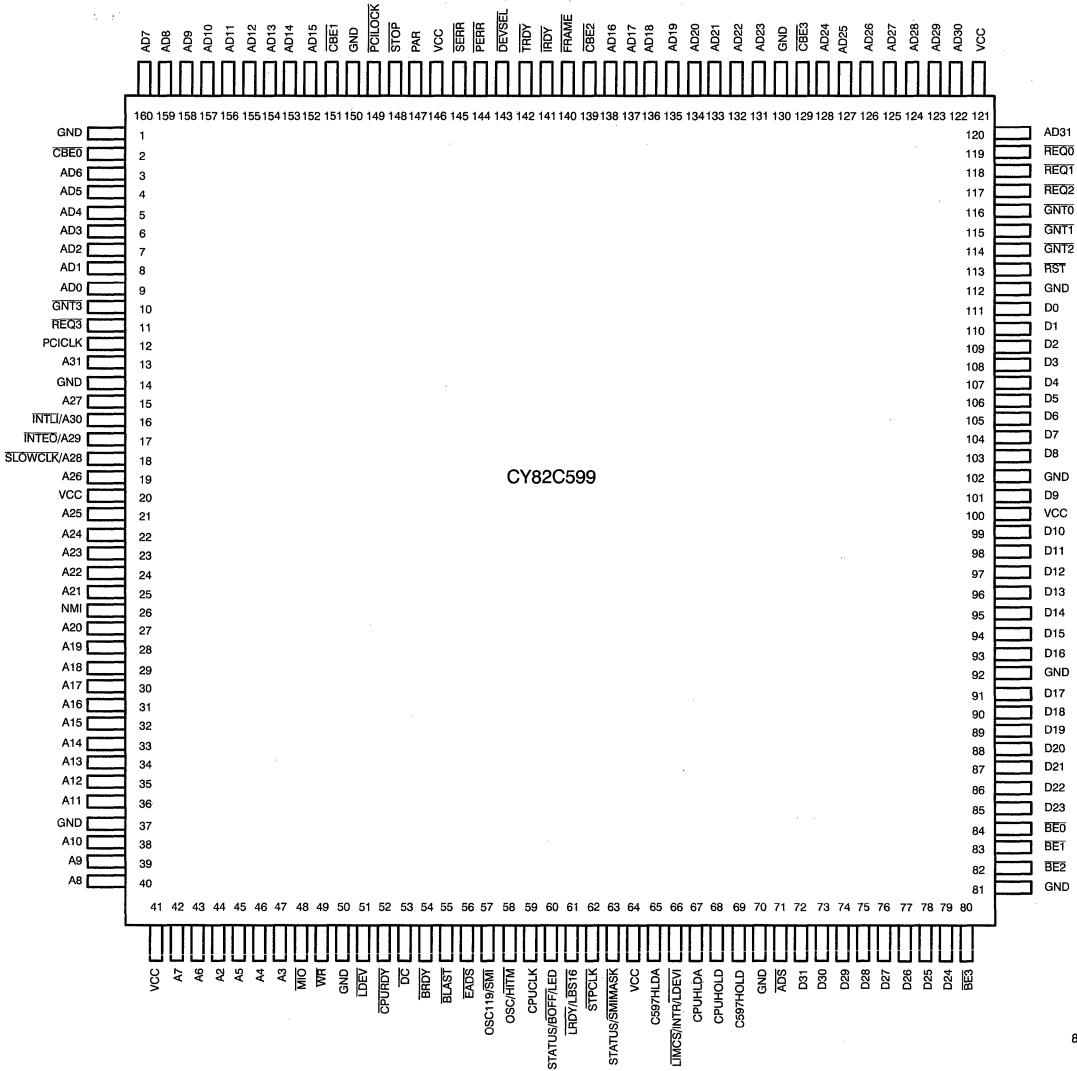
30. The assertion of **SLOWCLK** caused by the stand-by timer reaching its terminal count with no detected events.
31. The assertion of **STOPCLK** caused by the suspend timer reaching its terminal count with no detected events.

32. **SLOWCLK** and **STOPCLK** deassertion caused by the detection of one of the monitored events.

Document #: 38-00411

Pin Configurations

POFP
Top View



phase. By doing so, all of the agents on the bus, including the Target and the Arbiter, recognize that the current transaction is coming to an end. This advanced notice allows the Arbiter to grant ownership of the bus to the next requesting agent. This is referred to as Hidden Arbitration since no additional clock cycles are consumed. The new Master will not start to drive the bus until the current transaction is actually completed. The Target has the ability to abort the transaction prematurely should the need arise, although this is not the typical method of termination.

Arbitration in PCI is access based instead of time slot based. This is accomplished through a simple request-grant handshaking scheme through a central arbiter. Each agent has dedicated request and grant lines to the arbiter. A bus Master must request and be granted bus ownership each time a transaction is desired.

PCI defines three different physical address spaces; memory, I/O, and configuration space. Each of these address spaces has its own characteristics. Therefore, transactions to each space are handled differently, particularly in regards to AD[0:1]. The memory and I/O address spaces are customary, but the configuration address space has been defined by PCI in order to support hardware configuration.

4.0 Address Space

The purpose of this section is to explain the memory and I/O address space mapping used by the CY82C599.

The CY82C599 recognizes two different physical address spaces, memory and I/O. Transactions to these two address spaces are handled differently, and therefore need to be distinguished from one another. The CY82C599 differentiates these two different types of transactions by monitoring the M/I/O signal coming from the CPU bus, or the C/BE signals coming from the PCI bus. In order to recognize the destination of each transaction, each address space needs to be divided (or mapped) into the different target areas (ISA, PCI, VESA, or Local Memory). Each address map, memory and I/O, is discussed below.

4.1 I/O Address Space

Although the I/O address space can extend the full 32 bits (a possible 4 GB of I/O address space), x86 CPUs limit I/O transactions to the lower 64KB (0000h–FFFFh). The remaining address locations are not valid I/O address space. In addition, the lower 1KB (0000h–03FFh) of I/O space has been assigned as AT I/O space. Within the lower 1KB (AT space) resides numerous predefined I/O blocks that can be assigned to PCI or ISA/VESA through configuration registers. The remaining I/O address locations (0400h–FFFFh) can be mapped using three 100% user defined I/O blocks. The base address, block size, and bus location (e.g. PCI, VESA, or ISA) of these I/O blocks are determined by the configuration registers during boot-up (see configuration registers). If an I/O address area is excluded from the user defined blocks mentioned above, it is considered to be in an 'unknown' I/O location. 'Unknown' I/O address locations are handled on a priority basis (see the I/O access priority sections for further details). Although the PCI base address can be placed anywhere within the lower 64KB using one of the three 100% user defined I/O blocks, it is recommended that the PCI base address be placed at 8000h or above to avoid contention with VESA devices. VESA and PCI devices should never occupy the same I/O address location. Doing so will cause a bus contention condition. How the CY82C599 responds to each I/O transaction is discussed in the following sections.

4.2 Memory Address Space

The CY82C599 supports up to 256MB of local memory space (128MB when used with the CY82C596/7). The full 4GB memory space can be mapped over the PCI, VESA, or ISA regions (see configuration registers). This mapping allows the CY82C599 to determine the destination of the transaction and respond appropriately. A minimum of 64KB (0000h–FFFFh) of memory address space is reserved for system usage. Up to 256MB can be defined as local memory. The Local memory ending address is user defined through configuration registers 20h and 21h. The CY82C599 also supports 4 user defined memory block. Blocks 0 & 1 can be mapped over the entire address space by defining the base address, block size, and bus location. Blocks 2 & 3 are simply enabled/disabled (through register 46h) and can only be mapped to PCI. With these memory blocks the user can define the memory map of the system. As with I/O address space, some memory areas can be excluded from the memory map, and are therefore defined as 'unknown'. These 'unknown' locations are handled on a priority basis that is discussed in memory priority sections. How the CY82C599 responds to each transaction is discussed in each of the following sections.

4.3 PCI Configuration Space

The CY82C599 supports the preferred PCI Configuration Mechanism #1 that allows PCI configuration cycles to be generated by software. Both Type 0 and Type 1 configurations accesses are also supported. All required fields within the Configuration Header Space are also supported.

5.0 Device Operation

The purpose of this section is to describe the basic operation of the CY82C599 Intelligent PCI Bus Interface. The CY82C599 functional block diagram is shown in the functional block diagram. The core functionality of the CY82C599 is controlled by the Central Arbiter and the surrounding four state machines. These four state machines communicate with one another in order to properly conduct and synchronize all transactions. Supporting functions are conducted through control logic, interface and synchronization logic (PCI and CPU buses), configuration registers, and an internal bidirectional FIFO. The following sections describes the functionality of each of these major blocks within the CY82C599.

5.1 Central Arbiter

The Central Arbiter is responsible for delegating control of the CY82C599 Intelligent PCI Bus Interface. In addition, the Central Arbiter also performs the general arbitration on the PCI bus. The Central Arbiter monitors incoming requests from both the CPU and PCI buses and grants control of the Interface to either the PP (PCI Master Controlling PCI bus) or CC (CPU Master Controlling CPU bus) state machines. Once a request has been granted, control of the Interface is transferred to that particular state machine. Once the transaction is complete, the arbiter delegates control of the bridge to the next requesting agent. Should there be no pending requests, the default owner of the bridge is the CC (CPU Master Controlling CPU bus) state machine. When servicing a CPU master bus cycle, the Central Arbiter will not grant a PCI agent control of the PCI bus (although CY82C599 to PCI transfers are permitted during CPU to memory bus transactions due to Post-Write Operations). Also, when servicing a PCI agent, a CPU hold is established (HOLD asserted and HLDA acknowledged) prior to the PCI GNT signal

memory or I/O address space, as well as accesses to 'unknown' address locations. The purpose of the following sections is to explain the priorities of each type of transaction from each side of the CY82C599 Interface.

6.1 CPU Bus Master Priority-Memory Accesses

The highest priority in a CPU bus master memory access is when the target resides in Local memory. During these cycles, the CY82C599 monitors, but does not participate in the transaction.

The second highest priority in a CPU bus master memory access is when the target is in PCI or VESA memory address space. For transactions to PCI memory space, the CY82C599 will claim the transaction by asserting LDEV. The transaction is allowed to proceed normally, and is terminated on the CPU bus with CPURDY from the CY82C599. If the transaction is claimed by a VESA device, the VESA target will drive LDEV and terminates the transaction with CPURDY.

The lowest priorities are CPU bus master memory accesses to VESA or ISA address space. The CY82C599 will monitor, but will not participate in the transaction.

The CY82C599 will claim all memory transactions to 'unknown' address space on the CPU bus by asserting LDEV and will immediately initiate a PCI cycle. If the target is a PCI device (in 'unknown' space), the transaction is claimed by the PCI device and proceeds normally, with the CY82C599 terminating the transaction by asserting CPURDY to the CPU. If the PCI transaction goes unclaimed, the CY82C599 de-asserts LDEV. The CY82C599 will automatically de-assert LDEV if CPURDY goes active (the transaction was claimed and completed by a VESA device). If the target is a VESA device (in 'unknown' space), it asserts LDEV and claims the transaction. Since LDEV from the CY82C599 and the VESA devices are ANDed together, the CY82C596/7 will only pass the cycle to the ISA bus if neither VESA or PCI claims the transaction. Since VESA and PCI agents share the same priority, two memory devices (one on VESA and the other PCI) should never share the same address space. Doing so will cause a clash condition by having both devices claim the same transaction.

6.2 CPU Bus Master Priority-I/O Accesses

The highest priority CPU bus master I/O transaction is PCI/VESA space. These two types of devices I/O address spaces are considered to have the same priority. The CY82C599 will claim I/O transactions to PCI address space by asserting LDEV. The transaction is allowed to proceed normally, and is terminated on the CPU bus with CPURDY from the CY82C599. If the transaction is to VESA I/O address space, the VESA target will claim the transaction by asserting LDEV.

The second priority CPU bus master access to I/O space is when the target resides in ISA space. The CY82C599 will monitor, but not participated in CPU bus master transactions to ISA space.

If the address is not mapped to PCI/VESA or ISA space, then it is considered as 'unknown'. The CY82C599 will claim all I/O transactions to 'unknown' address space on the CPU bus by asserting LDEV and will immediately initiate a PCI cycle. If the target is a PCI device (in 'unknown' space), the transaction is claimed by the PCI device and proceeds normally, with the CY82C599 terminating the transaction by asserting CPURDY to the CPU. If the PCI transaction goes unclaimed, the CY82C599 de-asserts LDEV. The CY82C599 will automatically de-assert LDEV if CPURDY goes active (the transaction was claimed and completed by a VESA device). If the target is a VESA device (in 'unknown' space), it asserts LDEV and claims the transaction. Since LDEV from the CY82C599 and the VESA devices are

ANDed together, the CY82C596/7 will only pass the cycle to the ISA bus if neither VESA or PCI claims the transaction. Since VESA and PCI agents share the same priority, two I/O devices (one on VESA and the other PCI) should never share the same address space. Doing so will cause a clash condition by having both devices claim the same transaction.

6.3 PCI Master Priority-Memory Accesses

The highest priority PCI master memory transaction is an access to Local memory. During such transactions the CY82C599 will claim the CPU bus as quickly as possible by asserting a hold request to the CPU. PCI bus ownership is not granted until a hold acknowledge is received back from the CPU. Once bus ownership has been established, the transaction proceeds normally with the CY82C599 as the CPU bus master.

The second priority PCI master memory transaction is to PCI memory located on another PCI card. During these transactions the CY82C599 monitors, but does not participate in the transaction. In addition, the CY82C599 will hold the CPU bus during the entire transaction.

The third priority PCI master memory transaction is to ISA/VESA address space. During these types of transfers, the CY82C599 will claim the ISA/VESA bus as soon as possible and initiate an ISA/VESA cycle.

If the address is not mapped to PCI/VESA or ISA space, then it is considered as 'unknown'. PCI agents are given the first opportunity to claim PCI master accesses to 'unknown' memory space. The CY82C599 will wait for a PCI agent to claim the transaction by monitoring DEVSEL. If the transaction goes unclaimed on the PCI bus, the CY82C599 will automatically start a CPU bus cycle. If the transaction goes unclaimed on the CPU bus, the 82C596/7 will automatically pass the transaction to the ISA bus.

6.4 PCI Master Priority-I/O Accesses

The highest priority PCI master I/O access is to PCI address space. During these transactions the CY82C599 monitors, but does not participate in the transaction. In addition, the CPU bus is held during the entire transaction.

The second priority PCI master I/O transaction is to the ISA bus. During such transactions, the CY82C599 will claim the transaction by asserting DEVSEL and behave as the PCI target. The CY82C599 will also start a CPU bus as soon as possible and initiate an ISA/VESA cycle.

If the address is not mapped to PCI/VESA or ISA space, then it is considered as 'unknown'. PCI agents are given the first opportunity to claim PCI master accesses to 'unknown' I/O space. The CY82C599 will wait for a PCI agent to claim the transaction by monitoring the DEVSEL. If the transaction goes unclaimed on the PCI bus, the CY82C599 will automatically start a CPU bus cycle. If the transaction goes unclaimed on the CPU bus, the 82C596/7 will automatically pass the transaction to the ISA bus.

7.0 Level 1 Write-Back Cache Support

The CY82C599 also provides for chipsets that support Level 1 write-back cache. The CY82C599 adheres to the HITM protocol required to maintain cache coherency. When HITM is asserted, the CPU has detected a hit to a modified line in the Level 1 cache. In order to allow the CPU to write-back the modified line, the CY82C599 de-asserts the HOLD request to the CPU. The CPU then proceeds to write the modified line to DRAM and L2 cache (if a L2 cache hit is detected). The CY82C599 immediately requests another HOLD to the CPU so the initial transaction can continue.

10.0 Control Registers

This section summarizes the registers in the CY82C599.

The on-chip registers are accessed via I/O sequence 22H and 23H. Each register is selected by writing a byte containing the register address index to I/O address 22H. A subsequent byte read/write to I/O address 23H will modify/read-out the contents of the selected register.

The CY82C599 provides five groups of registers :

- Memory address space configuration registers (except PC/AT high memory)
- I/O address space configuration registers
- Power down configuration registers
- State machine configuration registers
- PC/AT high memory address space configuration registers

The Local DRAM Address Configuration Registers are used to establish the boundary of the Local DRAM in the system. Index 20H and 21H are used to specify the ending address of on-board DRAMs. Index 22H to 27H are the configuration registers for

Memory Blocks 0 and 1. They contain the base address of each memory block, the block sizes, and the mapping selection for each block : Local DRAM region, PCI region or ISA region. It is best to specify all Non-Local DRAM memory areas below 16Mbytes as ISA region and remap all other Non-Local DRAM memory areas above 2 Gbytes as the PCI region.

I/O Block Configuration Registers are used to specify the base address, block size, and function select for the user selectable I/O blocks. The pre-defined I/O blocks are simply enabled or disabled.

Power Down Configuration Registers allow various hardware events to be monitored in order to invoke or come out of power down mode.

State Machine configuration registers control features of the PCI and CPU bus State Machines. These features include the number of wait states, and arbitration priority of both State Machines.

PC/AT High Memory Address Space Configuration Registers are used to specify the memory regions from 000A0000H to 000FFFFFFH (blocks A, B, C, D, E, and F). These bits are used with CY82C59/67 to provide shadowing in a PC/AT system.

Index 20H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Reserved	0000	0000
3:0	Local DRAM Ending Address: $\overline{A27} : \overline{A24}$	0000	User selectable

Index 21H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Local DRAM Ending Address: $\overline{A23} : \overline{A16}$	00000000	User selectable

Index 22H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Memory Block 0 Base Address: $\overline{A31} : \overline{A24}$	00000000	User selectable

Index 23H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Memory Block 0 Base Address: $\overline{A23} : \overline{A16}$	00000000	User selectable

Index 27H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:6	Memory Block 1 Base Address: A15 : A14	00	User selectable
5:4	Memory Block 1 Function Select: 00: Disable (Default) 01: Local DRAM Region 10: PCI Region 11: ISA/VESA Region	00	User selectable
3:0	Memory Block 1 Size Select: 0000: 16KByte (Default) 0001: 32KByte 0010: 64KByte 0011: 128KByte 0100: 256KByte 0101: 512KByte 0110: 1MByte 0111: 2MByte 1000: 4MByte 1001: 8MByte 1010: 16MByte 1011: 32MByte 1100: 64MByte 1110: 256MByte 1111: 512MByte	0000	User selectable

Index 28H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	I/O Block 0 Base Address: A15 : A8	00000000	User selectable

Index 29H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	I/O Block 0 Base Address: A7 : A4	0000	User selectable
3:2	I/O Block 0 Function Select: 0X: Disable (Default) 10: PCI Region 11: ISA/VESA Region	00	User selectable
1:0	I/O Block 0 Size Select: 00: 16 Byte (Default) 01: 64 Byte 10: 256 Byte 11: 1024Byte	00	User selectable

Index 2AH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	I/O Block 1 Base Address: A15 : A8	00000000	User selectable

Index 2DH

Bit	Function	Hardware Default	Recommended BIOS power-on setting																		
7	Reserved	0	0																		
6	Green Feature Timer Select (see Register 2DH, Bits 3:0).	0	User selectable																		
5	PCI Master Detection Enable: 0: Disable 1: Enable	0	User selectable																		
4	Floppy Disk Detection Enable: 0: Disable 1: Enable	0	User selectable																		
3:1	Green Feature Timer Delay Select: <table border="0" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%; text-align: center;">Bit 6=0</td> <td style="width: 50%; text-align: center;">Bit 6=1</td> </tr> <tr> <td>000: 30 Second</td> <td>000: 0.2 Seconds</td> </tr> <tr> <td>001: 4 Minute</td> <td>001: 0.4 Seconds</td> </tr> <tr> <td>010: 8 Minute</td> <td>010: 1.0 Seconds</td> </tr> <tr> <td>011: 16 Minute</td> <td>011: 1.8 Seconds</td> </tr> <tr> <td>100: 32 Minute</td> <td>100: 3.5 Seconds</td> </tr> <tr> <td>101: 65 Minute</td> <td>101: 7.0 Seconds</td> </tr> <tr> <td>110: 130 Minute</td> <td>110: 14.0 Seconds</td> </tr> <tr> <td>111: 260 Minute</td> <td>111: 30.0 Seconds</td> </tr> </table>	Bit 6=0	Bit 6=1	000: 30 Second	000: 0.2 Seconds	001: 4 Minute	001: 0.4 Seconds	010: 8 Minute	010: 1.0 Seconds	011: 16 Minute	011: 1.8 Seconds	100: 32 Minute	100: 3.5 Seconds	101: 65 Minute	101: 7.0 Seconds	110: 130 Minute	110: 14.0 Seconds	111: 260 Minute	111: 30.0 Seconds	000	User selectable
Bit 6=0	Bit 6=1																				
000: 30 Second	000: 0.2 Seconds																				
001: 4 Minute	001: 0.4 Seconds																				
010: 8 Minute	010: 1.0 Seconds																				
011: 16 Minute	011: 1.8 Seconds																				
100: 32 Minute	100: 3.5 Seconds																				
101: 65 Minute	101: 7.0 Seconds																				
110: 130 Minute	110: 14.0 Seconds																				
111: 260 Minute	111: 30.0 Seconds																				
0	Green Feature Enable 0: Disable 1: Enable	0	User selectable																		

Index 2EH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	I/O Trap Address: IOA7 : IOA0	00000000	User selectable

Index 2FH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Reserved	0000	0000
3	I/O Trap Detection Enable: 0: Disable 1: Enable	0	User selectable
2	Reserved	0	0
1:0	I/O Trap Address: IOA9 : IOA8	00	User selectable

Index 33H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	CPU Master CPU State Machine I/O Post Write Cycle Enable: 0: Disable 1: Enable	0	0
6	Reserved	0	1
5:4	CPU Master PCI Retry: 00: Disable (Default) 01: 1 10: 3 11: Infinite	00	11
3	CPU Master Write Burst Mode Enable: 0: Disable 1: Enable	0	0
2	CPU Master PCI State Machine Fast Back-to-Back Enable: 0: Disable 1: Enable	0	0
1	CPU Master PCI State Machine Address OWS Enable: 0: Disable 1: Enable	0	0
0	CPU Master PCI State Machine Data Write OWS Enable: 0: Disable 1: Enable	0	0

Index 35H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	PCI Master PCI State Machine Data Write OWS Enable: 0: Disable 1: Enable	0	0
6	PCI Master PCI State Machine Burst Mode Enable: 0: Disable 1: Enable	0	0
5	PCI Master State Machine Fast Interface Enable: 0: Disable 1: Enable	0	0
4	PCI Master State Machine Generate Fast \overline{ADS} Cycle Enable: 0: Disable 1: Enable Note: See register 34, Bit6.	0	0
3:2	CPU Master PCI DEVSEL Time Out Period: 00: 6 PCICLK (Default) 01: 5 PCICLK 10: 4 PCICLK 11: 3 PCICLK	00	00
1:0	PCI Master PCI Subtractive Decode DEVSEL Time Out Period: 00: 6 PCICLK (Default) 01: 5 PCICLK 10: 4 PCICLK 11: 3 PCICLK	00	10

Note: PCI Master PCI Subtractive Decode DEVSEL Time Out Period must be equal or less than CPU Master PCI DEVSEL Time Out Period

Index 36H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Configuration Address Cycle Enable: 0: Disable 1: Enable	0	1
6	Configuration Data Cycle Enable: 0: Disable 1: Enable	0	1
5	Configuration Data Special Cycle Enable: 0: Disable 1: Enable	0	1
4	PCI Master Configuration Address Cycle Enable: 0: Disable 1: Enable	0	0
3	Reserved	0	0
2	Reserved	0	0
1	First Level Arbitration Rotate Enable: 0: Disable 1: Enable	0	0
0	Reserved	0	1

Index 3AH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Shadow Block C0000h : C3FFFh Bits 7:6 <u>Function</u> 00: Disable 01: Local DRAM Read 10: PCI Read 11: ISA/VESA Read Bits 5:4 <u>Function</u> 00: Disable 01: Local DRAM Write 10: PCI Write 11: ISA/VESA Write	0000	User selectable
3:0	Shadow Block C4000h : C7FFFh Bits 3:2 <u>Function</u> 00: Disable 01: Local DRAM Read 10: PCI Read 11: ISA/VESA Read Bits 1:0 <u>Function</u> 00: Disable 01: Local DRAM Write 10: PCI Write 11: ISA/VESA Write	0000	User selectable

Index 3BH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Shadow Block C8000h : CBFFFh Bits 7:6 <u>Function</u> 00: Disable 01: Local DRAM Read 10: PCI Read 11: ISA/VESA Read Bits 5:4 <u>Function</u> 00: Disable 01: Local DRAM Write 10: PCI Write 11: ISA/VESA Write	0000	User selectable
3:0	Shadow Block CC000h : CFFFFh Bits 3:2 <u>Function</u> 00: Disable 01: Local DRAM Read 10: PCI Read 11: ISA/VESA Read Bits 1:0 <u>Function</u> 00: Disable 01: Local DRAM Write 10: PCI Write 11: ISA/VESA Write	0000	User selectable

Index 3CH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Shadow Block D0000h : D3FFFh Bits 7:6 <u>Function</u> 00: Disable 01: Local DRAM Read 10: PCI Read 11: ISA/VESA Read Bits 5:4 <u>Function</u> 00: Disable 01: Local DRAM Write 10: PCI Write 11: ISA/VESA Write	0000	User selectable
3:0	Shadow Block D4000h : D7FFFh Bits 3:2 <u>Function</u> 00: Disable 01: Local DRAM Read 10: PCI Read 11: ISA/VESA Read Bits 1:0 <u>Function</u> 00: Disable 01: Local DRAM Write 10: PCI Write 11: ISA/VESA Write	0000	User selectable

Index 40H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Reserved. Must be set to 1 after power-on.	0	1
6	Reserved.	0	1
5	Reserved, Must be set to 1 after power-on.	0	1
4	I/O write 22H, 23H, & 61H LDEV mask enable.	0	0
3	Reserved, must be set to 1 after power-on.	0	1
2	Configuration register Read Enable: 0: Write only. 1: Read/Write.	0	1
1	Monitor VESA VL Bus LDEV enable.	0	0
0	VESA to PCI Stand Alone enable.	0	0

Index 41H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	VESA VL Bus $\overline{BSI6}$ support enable.	0	0
6:0	Reserved	0000000	0010111

Index 42H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Reserved.	0000	0001
3	Write back mode with no PCI Master HOLD support enable.	0	0
2:1	Reserved, set to 0 after power-on.	00	00
0	Level 1 Write back mode enable.	0	0

Index 43H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	\overline{LRDY} delay 1 CPUCLK enable.	0	0
6:0	Reserved	0000000	0000000

Index 44H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Not used, available for BIOS storage.	00000000	00000000

Index 45H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Not used, available for BIOS storage.	00000000	00000000

Index 49H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	ISA/VESA I/O space 0180H to 018FH select enable.	0	User selectable
6	ISA/VESA I/O space 0190H to 019FH select enable.	0	User selectable
5	ISA/VESA I/O space 01A0H to 01AFH select enable.	0	User selectable
4	ISA/VESA I/O space 01B0H to 01BFH select enable.	0	User selectable
3	ISA/VESA I/O space 01C0H to 01CFH select enable.	0	User selectable
2	ISA/VESA I/O space 01D0H to 01DFH select enable.	0	User selectable
1	ISA/VESA I/O space 01E0H to 01EFH select enable.	0	User selectable
0	ISA/VESA I/O space 01F0H to 01FFH select enable.	0	User selectable

Index 4AH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	ISA/VESA I/O space 0200H to 020FH select enable.	0	User selectable
6	ISA/VESA I/O space 0210H to 021FH select enable.	0	User selectable
5	ISA/VESA I/O space 0220H to 022FH select enable.	0	User selectable
4	ISA/VESA I/O space 0230H to 023FH select enable.	0	User selectable
3	ISA/VESA I/O space 0240H to 024FH select enable.	0	User selectable
2	ISA/VESA I/O space 0250H to 025FH select enable.	0	User selectable
1	ISA/VESA I/O space 0260H to 026FH select enable.	0	User selectable
0	ISA/VESA I/O space 0270H to 027FH select enable.	0	User selectable

Index 4BH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	ISA/VESA I/O space 0280H to 028FH select enable.	0	User selectable
6	ISA/VESA I/O space 0290H to 029FH select enable.	0	User selectable
5	ISA/VESA I/O space 02A0H to 02AFH select enable.	0	User selectable
4	ISA/VESA I/O space 02B0H to 02BFH select enable.	0	User selectable
3	ISA/VESA I/O space 02C0H to 02CFH select enable.	0	User selectable
2	ISA/VESA I/O space 02D0H to 02DFH select enable.	0	User selectable
1	ISA/VESA I/O space 02E0H to 02EFH select enable.	0	User selectable
0	ISA/VESA I/O space 02F0H to 02FFH select enable.	0	User selectable

Index 4FH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	PCI I/O space 01F0H to 01FFH select enable.	0	User selectable
6	PCI I/O space 03F6H to 03F7H select enable.	0	User selectable
5	PCI I/O space 0170H to 017FH select enable.	0	User selectable
4	PCI I/O space 0370H to 0377H select enable.	0	User selectable
3	PCI I/O space 03B0H to 03BBH select enable.	0	User selectable
2	PCI I/O space 03C0H to 03CFH select enable.	0	User selectable
1	PCI I/O space 03D0H to 03DFH select enable.	0	User selectable
0	PCI I/O space 03F0H to 03F5H select enable.	0	User selectable

Register 50: Suspend Timer and Interrupt Timer Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Bits (Suspend Timer Period) 0000: 3.8 min. 0001: 7.5 min. 0010: 15 min. 0011: 30 mins. 0100: 60 mins. 0101: 120 mins. 0110: 240 mins. 0111: 480 mins. 0000: 1 sec. 1001: 1.8 sec. 1010: 3.5 sec. 1011: 7 sec. 1100: 14 sec. 1101: 28 sec. 1110: 56 sec. 1111: 2 min.	0000	User selectable
3:0	Bits (Interrupt Timer Period) 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 54 μ sec. 0110: 107 μ sec. 0111: 215 μ sec. 0000: 430 μ sec. 1001: 860 μ sec. 1010: 1.7 msec. 1011: 3.4 msec. 1100: 7 msec. 1101: 14 msec. 1110: 28 msec. 1111: 55 msec.	0000	User selectable

Register 52: Power-Down Mode Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Bits Software initial <u>SMI</u> 0: Normal 1: Writing an 1 to this bit will generate an <u>SMI</u> to the CPU. After a 1 is written, software should write a 0 to this bit.	0	User selectable
6	Bits <u>SMI</u> inactive control 0: Normal 1: Writing a 1 to this bit will deassert the <u>SMI</u> signal. This is the only way to cause the 82C599 to deassert <u>SMI</u> . After a 1 is written, 0 should be written to this bit to allow <u>SMI</u> to be deasserted.	0	User selectable
5	Bits <u>STOPCLK</u> Active Control 0: Normal 1: Writing a 1 to this bit will assert the <u>STOPCLK</u> signal. Software should subsequently write a 0 to this bit to allow <u>STOPCLK</u> to be deasserted.	0	User selectable
4	Bits Software <u>STOPCLK</u> Inactive Control 0: Normal 1: Writing a 1 will deassert <u>STOPCLK</u> . Software should subsequently write a 0 to this bit to allow <u>STOPCLK</u> to be asserted.	0	User selectable
3	Bits Software <u>SLOWCLK</u> Active Control 0: Normal 1: Writing a 1 will assert <u>SLOWCLK</u> . Software should subsequently write a 0 to this bit to allow <u>SLOWCLK</u> to be deasserted.	0	User selectable
2	Bits Software <u>SLOWCLK</u> Inactive Control 0: Normal 1: Writing a 1 will deassert <u>SLOWCLK</u> . Software should subsequently write a 0 to this bit to allow <u>SLOWCLK</u> to be asserted.	0	User selectable
1	Bits Suspender Time Control 0: Enable suspend timer (default) 1: Disable suspend timer The 82C599 allows a second Suspend mode to be started after the current suspend timer has reached its terminal count (i.e. When the current suspend timer expires, it will assert <u>SMI</u>). Within the <u>SMI</u> subroutine, the suspend timer can be disabled and the suspend timer reenabled. After the new terminal count has been reached, the 82C599 will initiate another <u>SMI</u> .	0	User selectable
0	Bits Disable Software Reset Mask 0: Normal 1: Force CY82C599 to inactivate pin 112. This bit should be set to "1", then set to "0" before leaving <u>SMI</u> subroutine.	0	0

Register 56: Special Memory and I/O Event Detection

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Bits 0: Disable special memory I/O detection 1: Enable special memory I/O detection	0	User selectable
6	Bits 0: Detect I/O cycle 1: Detect memory cycle	0	User selectable
5	Bits 0: No write cycle detection 1: Detect write cycle	0	User selectable
4	Bits 0: No read cycle detection 1: Detect ready cycle	0	User selectable
3	I/O address A19.	0	User selectable
2	I/O address A18.	0	User selectable
1	I/O address A17.	0	User selectable
0	I/O address A16.	0	User selectable

Registers 54, 55, and 56 allow for special memory or I/O event detection. For memory detection, address A31, A26, A25, A24, A23, A22, A21, and A20 are monitored. Memory detection can also be limited to read cycles or write cycles. Certain memory addresses can also be masked. (Register 55) If the corresponding

mask bit (e.g. mask A20) is set, then address (A20) will not be decoded. For I/O detection, addresses A19–A0 can be monitored. I/O detection can also be limited to read-only or write-only. I/O detection does not allow for address masking.

Register 57: Power Down Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Reserved.	0	0
6:5	Bits (LED frequency control) 00: 0.4 sec. 01: 1.0 sec. 10: 1.8 sec. 11: 3.5 sec.	0	User selectable
4	Bits Quick Power Down control 0: Disable Quick Power Down mode. 1: Enable Quick Power Down mode.	0	User selectable
3:0	Reserved.	0	0

The 82C599 supports Quick Power Down through pin 18. When pin 18 is selected, the CY82C599 will bring itself into Power Down Mode in 3 seconds if no event is detected, and Register 57, Bit 4=1.

Register 5A: Timer 3 Event Detection Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Bits 0: Disable key-board event detection 1: Enable key-board event detection	0	User selectable
6	Bits 0: Disable serial port event detection 1: Enable serial port event detection	0	User selectable
5	Bits 0: Disable parallel port event detection 1: Enable parallel port event detection	0	User selectable
4	Bits 0: Disable hard disk event detection 1: Enable hard disk event detection	0	User selectable
3	DMA/ISA master / AT refresh detection: 0: Disable DMA/ISA master / AT refresh detection 1: Enable DMA/ISA master / AT refresh detection	0	User selectable
2	Bits 0: Disable non-motherboard memory detection 1: Enable non-motherboard memory detection	0	User selectable
1	Bits 0: Disable access floppy detection 1: Enable access floppy detection	0	0
0	Bits 0: Disable video memory (Block A,B) event detection 1: Enable video memory (Block A,B) event detection	0	User selectable

Index 5C: Timer 4 Event Detection Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Bits 0: Disable key-board event detection 1: Enable key-board event detection	0	User selectable
6	Bits 0: Disable serial port event detection 1: Enable serial port event detection	0	User selectable
5	Bits 0: Disable parallel port event detection 1: Enable parallel port event detection	0	User selectable
4	Bits 0: Disable hard disk event detection 1: Enable hard disk event detection	0	User selectable
3	Bits 0: Disable DMA/ISA master / AT refresh event detection 1: Enable DMA/ISA master / AT refresh event detection	0	User selectable
2	Bits 0: Disable non-motherboard memory event detection 1: Enable non-motherboard memory event detection	0	User selectable
1	Floppy Access Detection: 0: Disable Floppy Disk Detection 1: Enable Floppy Disk Detection	0	0
0	Bits 0: Disable video memory (Block A,B) event detection 1: Enable video memory (Block A,B) event detection	0	User selectable

CY82C599 Pin Descriptions
PCI Interface

Name	I/O	Pin Number	Description
AD[31:0]	I/O	120, 122-128, 131-138, 152-160, 3-9	PCI Address and Data bus. During the address phase, AD[31:0] contain a physical address. During data phase, it contains 32-bit data.
CBE[3:0]	I/O	129, 139, 151, 2	Bus Command and Byte Enables are multiplexed.
PAR	I/O	147	Parity is even parity across AD[31:0].
FRAME	I/O	140	Cycle Frame is driven by the current master to indicate the beginning and duration of an access.
IRDY	I/O	141	Initiator Ready indicates the master's ability to complete the current data phase of the transaction.
TRDY	I/O	142	Target Ready indicates the target agent's ability to complete the current data phase of the transaction.
STOP	I/O	148	Stop indicates the current target is requesting the master to stop the current transaction.
REQ[3:0]	I	11, 117, 118, 119	Request indicate to the arbiter that this agent desires of the bus.
GNT[3:0]	O	10, 114, 115, 116	Grant indicate to the agent that access to the bus has been granted.
RST	I	113	Reset.
PCICLK	I	12	Clock to every PCI device.
PCILOCK	I/O	149	Lock indicates an atomic operation that may require multiple transactions to complete.
DEVSEL	I/O	143	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current address. As an input, it indicates whether any device on the bus has been selected.
SERR	I	145	System Error.
PERR	I	144	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle.



Arbitration

Name	I/O	Pin Number	Description
CPUHLDA	I	67	Input from CPU HLDA signal.
CPUHOLD	O	68	Output to CPU HOLD signal.
C597HOLD	I	69	Input from 82C597 HOLD signal.
C597HLDA	O	65	Output to 82C597 HLDA signal.

Ground and V_{CC}

Name	I/O	Pin Number	Description
V _{CC}	I	20, 41, 64, 100, 121, and 146	+5V power supply
GND	I	1, 14, 37, 50, 70, 81, 92, 102, 112, 130, and 150	Ground

CY82C599 DC Characteristics

Maximum Ratings

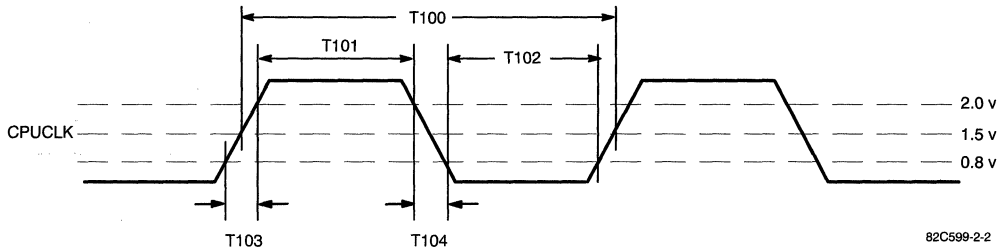
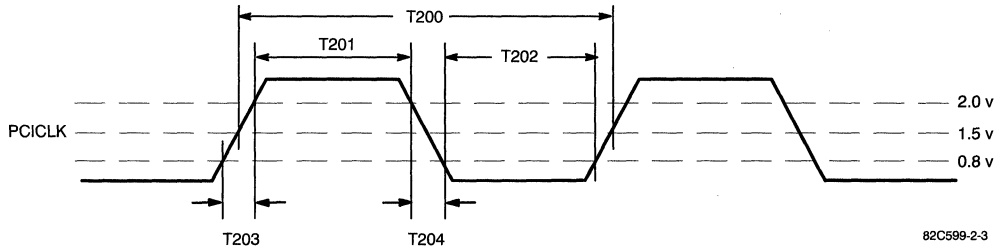
(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage +7 V
 Ambient Operating Temperature -25°C to +70°C

Ambient Storage Temperature -40°C to 125°C
 DC Voltage Applied to Outputs -0.5V to +5.5V
 DC Input Voltage -0.5V to +5.5V

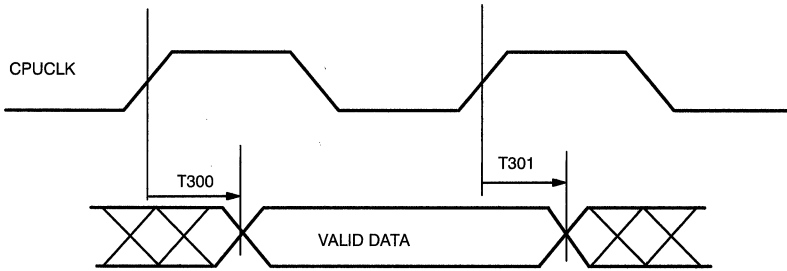
Electrical Characteristics Over the Operating Range (0°C to 70°C, V_{CC} = +5V ± 5%)

Parameter	Description	CY82C599		Unit
		Min.	Max.	
V _{IL}	Input LOW Voltage	-.05	0.8	V
V _{IH}	Input HIGH Voltage	2.0	V _{CC} +0.5	V
V _{OL}	Output LOW Voltage		0.4	V
V _{OH}	Output HIGH Voltage	2.4		V
I _{IL}	Input Leakage Current		10	μA
I _{OL}	Output Leakage		10	μA
C _{IN}	Input Capacitance		10	pF
C _{OUT}	Output Capacitance		10	pF
I _{CC}	Power Supply Current	33 MHz	100	mA

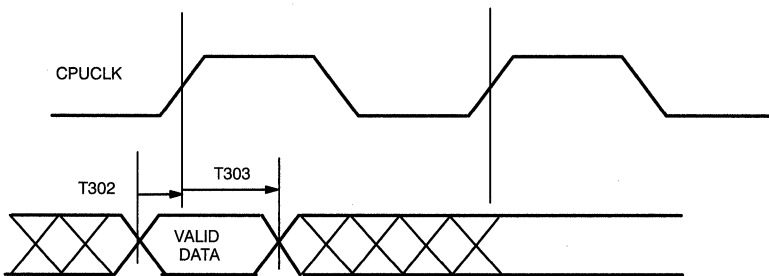
Switching Waveforms
CPUCLK Timing

PCICLK Timing


Switching Waveforms (continued)

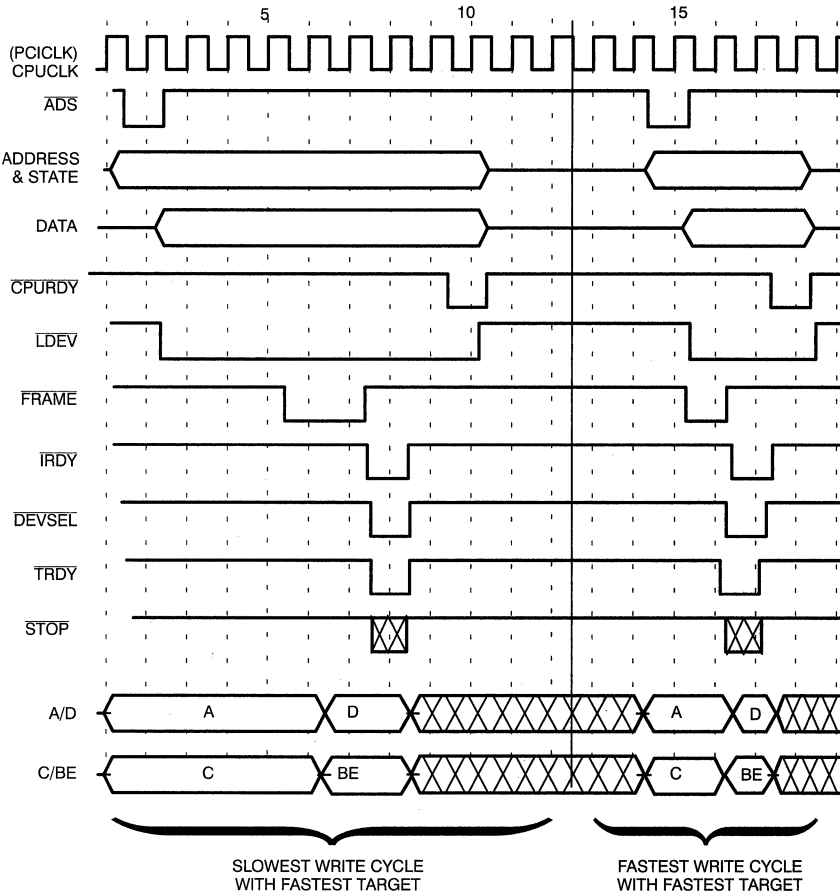
CPU BUS INTERFACE TIMING



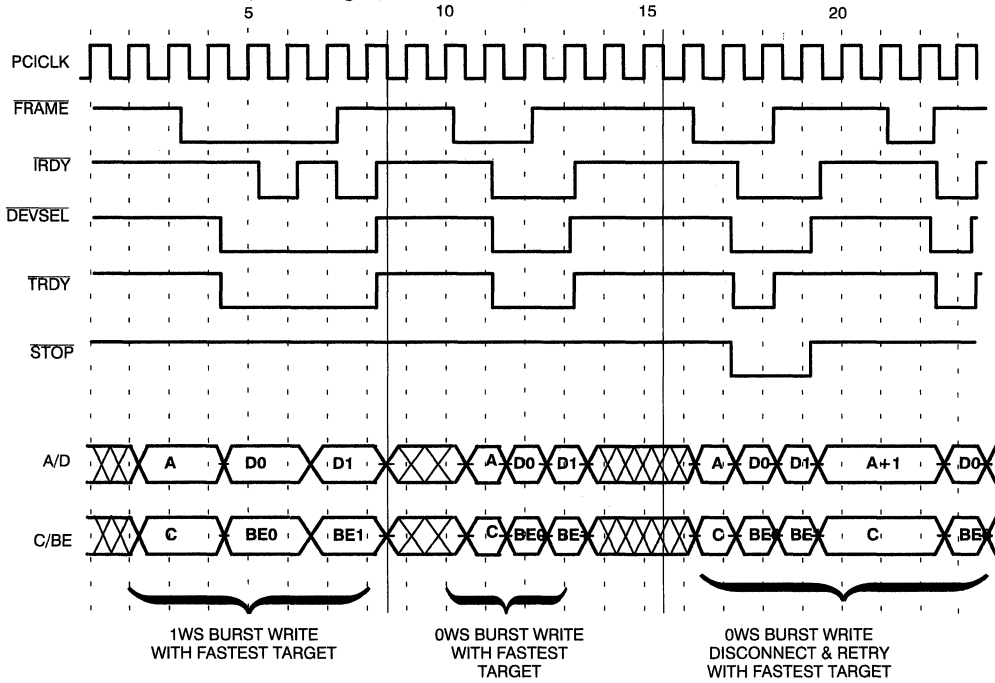
82C599-2-7



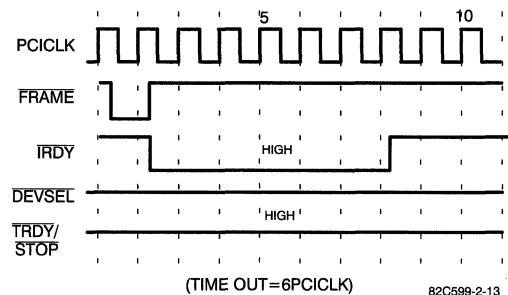
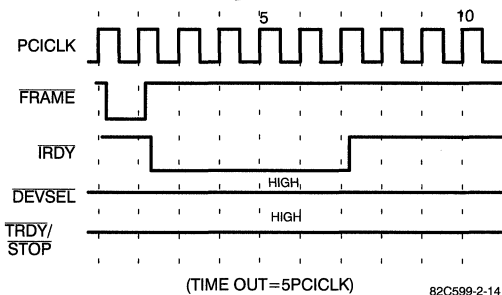
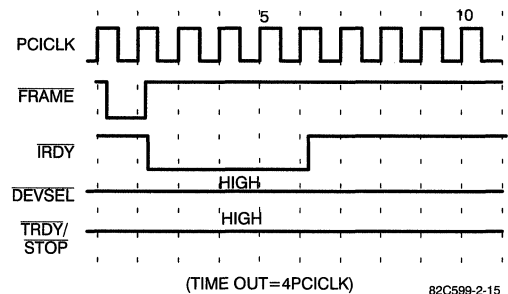
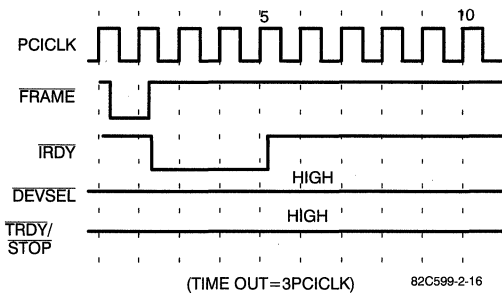
82C599-2-6

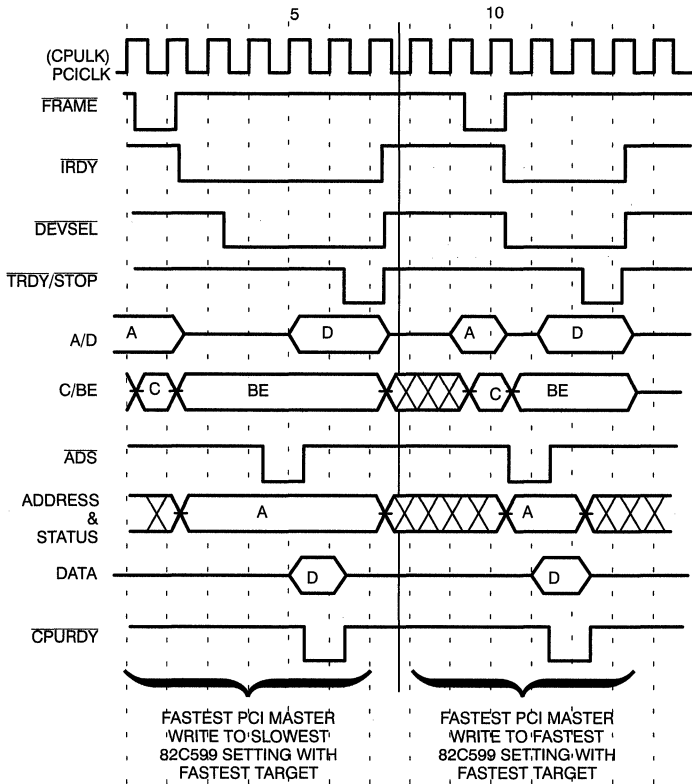
Switching Waveforms (continued)
CPU Master Write PCI Target


82C599-2-9

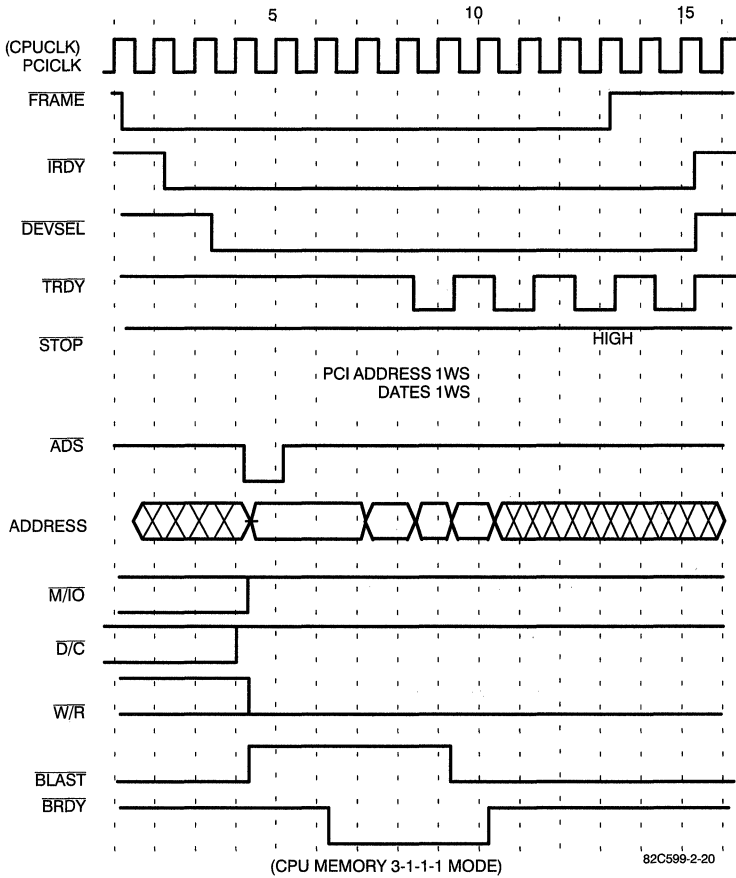
Switching Waveforms (continued)
CPU Master Burst Post Write, to PCI Target (PCI side) Data Available in Buffer.


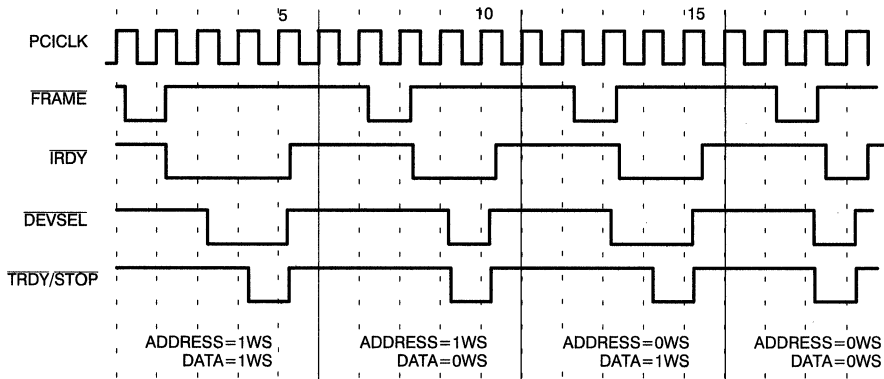
82C599-2-11

Switching Waveforms (continued)
**CPU Master to PCI Bus "Master Abort"
(DEVSEL) Time-Out Timing**

Switching Waveforms (continued)
**CPU Master to PCI Bus "Master Abort"
(DEVSEL) Time-Out Timing**

Switching Waveforms (continued)
**CPU Master to PCI Bus "Master Abort"
(DEVSEL) Time-Out Timing**

Switching Waveforms (continued)
**CPU Master to PCI Bus "Master Abort"
(DEVSEL) Time-Out Timing**


Switching Waveforms (continued)
PCI Master Read From 82C599 Target


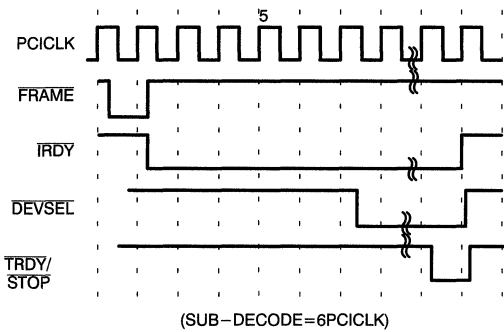
82C599-2-18

Switching Waveforms (continued)
PCI Master Burst Pre-Read to CPU


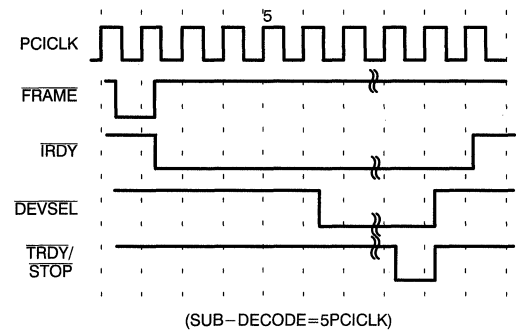
Switching Waveforms (continued)
PCI Master Post Write to CPU, PCI Side Buffer Available


82C599-2-22

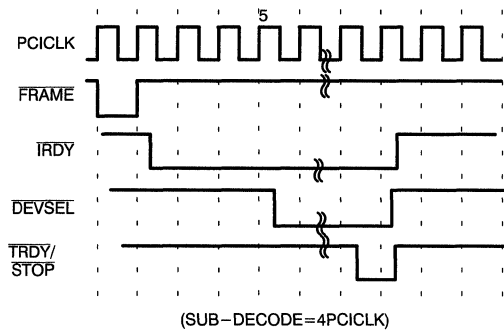
Note: CPU side same as 486 type CPU write cycle

Switching Waveforms (continued)
PCI Master Subtractive Decode "DEVSEL" Timing


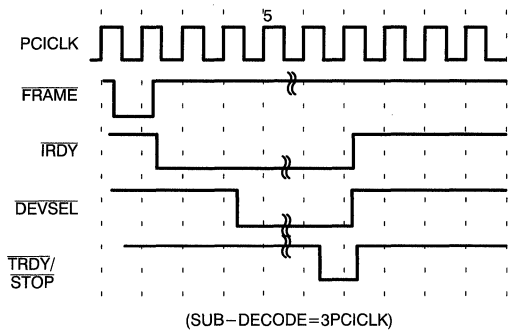
82C599-2-24

Switching Waveforms (continued)
PCI Master Subtractive Decode "DEVSEL" Timing


82C599-2-25

Switching Waveforms (continued)
PCI Master Subtractive Decode "DEVSEL" Timing


82C599-2-26

Switching Waveforms (continued)
PCI Master Subtractive Decode "DEVSEL" Timing


82C599-2-27



Section Contents

Military Information

Page Number

Military Overview	12-1
Military Product Selector Guide	12-2
Military Ordering Information	12-7



Military Product Selector Guide

Static RAMs

Size	Organization	Pins (DIP)	Part Number	JAN/SMD Number	Speed (ns)	I _{CC} /I _{SP} /I _{CCDR} (mA @ ns)	883 Availability
64	16x4—Inverting	16	CY7C189		t _{AA} = 25	70 @ 25	Now
64	16x4—Non-Inverting	16	CY7C190	5962-89694	t _{AA} = 25	70 @ 25	Now
64	16x4—Inverting	16	CY27S03/A		t _{AA} = 25, 35	100 @ 35	Now
64	16x4—Non-Inverting	16	CY27S07/A		t _{AA} = 25, 35	100 @ 25	Now
1K	256x4—10K/10KH ECL	24	CY10E422L		t _{AA} = 5, 7	150 @ 5/7	Now
1K	256x4	22	CY7C122	5962-88594	t _{AA} = 25, 35	90 @ 25	Now
1K	256x4	24S	CY7C123	5962-90696	t _{AA} = 10, 12, 15	150 @ 15	Now
1K	256x4	22	CY9122/91L22	5962-88594	t _{AA} = 35, 45	90 @ 45	Now
1K	256x4	22	CY93422A/93L422A	5962-88594	t _{AA} = 45, 55, 60, 75	90 @ 55	Now
4K	4Kx1—CS Power-Down	18	CY7C147	M38510/289	t _{AA} = 35, 45	110/10 @ 35	Now
4K	4Kx1—CS Power-Down	18	CY2147	M38510/289	t _{AA} = 45, 55	140/25 @ 45	Now
4K	4Kx1—CS Power-Down	18	CY7C147	5962-88587	t _{AA} = 35, 45	110/10 @ 35	Now
4K	4Kx1—CS Power-Down	18	CY2147	5962-88587	t _{AA} = 45, 55	140/25 @ 45	Now
4K	1Kx4—10K/10KH ECL	24	CY10E474L	5962-91518	t _{AA} = 5, 7	190 @ 5/7	Now
4K	1Kx4—CS Power-Down	18	CY7C148	M38510/289	t _{AA} = 35, 45	110/10 @ 35	Now
4K	1Kx4—CS Power-Down	18	CY2148	M38510/289	t _{AA} = 45, 55	140/25 @ 45	Now
4K	1Kx4	18	CY7C149		t _{AA} = 35, 45	110 @ 35	Now
4K	1Kx4	18	CY2149		t _{AA} = 45, 55	140 @ 45	Now
4K	1Kx4—Separate I/O	24S	CY7C150	5962-88588	t _{AA} = 12, 15, 25, 35	100 @ 15	Now
8K	1Kx8—Dual Port	48	CY7C130/31	5962-86875	t _{AA} = 35, 45, 55	120/40 @ 45	Now
8K	1Kx8—Dual-Port Slave	48	CY7C140/41	5962-86875	t _{AA} = 35, 45, 55	120/40 @ 45	Now
16K	4Kx4—CSECL	28	CY10E484L		t _{AA} = 7, 10	200 @ 10	Now
16K	2Kx8—CS Power-Down	24S	CY7C128A	5962-89690	t _{AA} = 20, 25	125 @ 20	Now
16K	2Kx8—CS Power-Down	24	CY6116A/7A	5962-89690	t _{AA} = 20, 25	125 @ 20	Now
16K	2Kx8—CS Power-Down	24S	CY7C128A	84036	t _{AA} = 35, 45, 55	125/40 @ 25	Now
16K	16Kx1—CS Power-Down	20	CY7C167A	84132	t _{AA} = 20, 25, 35, 45	70/20 @ 25	Now
16K	4Kx4—CS Power-Down	20	CY7C168A	5962-86705	t _{AA} = 20, 25, 35, 45	100/20 @ 25	Now
16K	4Kx4	20	CY7C169A		t _{AA} = 20, 25, 35, 40	100/20 @ 35	Now
16K	4Kx4—Output Enable	22S	CY7C170A		t _{AA} = 20, 25, 35, 45	120 @ 25	Now
16K	4Kx4—Separate I/O	24S	CY7C171A		t _{AA} = 20, 25, 35, 45	100/20 @ 25	Now
16K	4Kx4—Separate I/O, Power-Down	24S	CY7C172A	5962-89790	t _{AA} = 20, 25, 35, 45	90 @ 20	Now
16K	2Kx8—Dual-Port	48	CY7C132/36	5962-90620	t _{AA} = 35, 45, 55	170/65 @ 35	Now
16K	2Kx8—Dual-Port Slave	48	CY7C142/46	5962-90620	t _{AA} = 35, 45, 55	120/40 @ 45	Now
32K	4Kx8—Dual-Port	48	CY7B134	5962-93001	t _{AA} = 25, 35	280 @ 25	Now
32K	4Kx8—Dual-Port	52	CY7B135	5962-93001	t _{AA} = 25, 35	280 @ 25	Now
32K	4Kx8—Dual-Port Semaphores	52	CY7B1342		t _{AA} = 25, 35	280 @ 25	Now
32K	4Kx8—Dual-Port Semaphores Int, Busy	68	CY7B138		t _{AA} = 25, 35	280 @ 25	Now
32K	4Kx9—Dual-Port Semaphores Int, Busy	68	CY7B139		t _{AA} = 25, 35	280 @ 25	Now
64K	8Kx8—CS Power-Down	28S	CY7C185A	5962-38294	t _{AA} = 20, 25, 35, 45	125 @ 20	Now
64K	8Kx8—CS Power-Down	28S	CY7C185A	5962-89691	t _{AA} = 20, 25	125 @ 20	Now
64K	8Kx8—CS Power-Down	28S	CY7C185A	5962-85525	t _{AA} = 35, 45	100/20/1 @ 45	Now
64K	8Kx8—CS Power-Down	28S	CY7B185	5962-91594	t _{AA} = 10, 12, 15	145/50 @ 15	Now
64K	8Kx8—CS Power-Down	28	CY7C186A	5962-38294	t _{AA} = 20, 25, 35, 45	125 @ 20	Now
64K	8Kx8—CS Power-Down	28	CY7C186A	5962-89691	t _{AA} = 20, 25	125 @ 20	Now
64K	8Kx8—CS Power-Down	28	CY7C186A	5962-85525	t _{AA} = 35, 45, 55	100/20/1 @ 45	Now
64K	16Kx4—CS Power-Down	22S	CY7C164A	5962-89692	t _{AA} = 20, 25	90 @ 20	Now
64K	16Kx4—CS Power-Down	22S	CY7C164A	5962-86859	t _{AA} = 35	70/20/1 @ 35	Now
64K	16Kx4—CS Power-Down	22S	CY7B164	5962-91593	t _{AA} = 10, 12, 15	135/50 @ 15	Now
64K	16Kx4—CS Power-Down	24S	CY7C166A	5962-89892	t _{AA} = 20, 25	90 @ 20	Now
64K	16Kx4—Output Enable	24S	CY7C166A	5962-86859	t _{AA} = 35	70/20/1 @ 35	Now
64K	16Kx4—Output Enable	24S	CY7B166	5962-91593	t _{AA} = 10, 12, 15	135/50 @ 15	Now
64K	16Kx4—Separate I/O, T-write	28S	CY7C161A	5962-90594	t _{AA} = 20, 25, 35	70/20/1 @ 35	Now
64K	16Kx4—Separate I/O	28S	CY7C162A	5962-89712	t _{AA} = 20, 25, 35	70/20/1 @ 35	Now
64K	16Kx4—Separate I/O, T-write	28S	CY7B161		t _{AA} = 12, 15	135/50 @ 15	Now
64K	16Kx4—Separate I/O	28S	CY7B162	5962-92172	t _{AA} = 12, 15	135/50 @ 15	Now
64K	8Kx1—CS Power-Down	22S	CY7C187A	5962-86015	t _{AA} = 20, 25, 35	70/20/1 @ 35	Now
64K	8Kx8—Dual-Port Semaphores Int, Busy	68	CY7B144		t _{AA} = 25, 35	280 @ 25	Now
64K	8Kx9—Dual-Port Semaphores Int, Busy	68	CY7B145		t _{AA} = 25, 35	280 @ 25	Now



Military Product Selector Guide

PROMs (continued)

Size	Organization	Pins	Part Number	JAN/SMD Number ^{[1]*}	Speed (ns)	I _{CC} /I _{SB} (mA @ ns)	883 Availability
256K	16Kx16	44	CY7C276		t _{AA} =25, 30, 35	250@30	Now
256K	32Kx8—CS Power-Down	28S	CY7C271	5962-89817(W)	t _{AA} = 35, 45, 55	130/40 @ 35	Now
256K	32Kx8—CS Power-Down	28S	CY7C271	5962-93166(O)	t _{AA} = 35, 45, 55	130/40@55	Now
256K	32Kx8—EPROM Pinout	28	CY7C274	5962-89817(W)	t _{AA} = 35, 45, 55	130/40 @ 35	Now
256K	32Kx8—EPROM Pinout	28	CY7C274	5962-93166(O)	t _{AA} = 35, 45, 55	130/40 @ 35	Now
256K	32Kx8—EPROM Pinout	28	CY27C256		t _{AA} = 45, 55, 70, 90, 120, 150, 200	55/20	Now
256K	32Kx8—Registered	28S	CY7C277	5962-91744(W)	t _{SA/CO} = 40/20, 50/25	130 @ 40	Now
256K	32Kx8—Registered	28S	CY7C277	5962-92155(O)	t _{SA/CO} = 40/20, 50/25	130 @ 40	Now
512K	64Kx8—EPROM Pinout	28	CY7C286	5962-91637(O)	t _{AA} = 60, 70	150 @ 60	Now
512K	64Kx8—EPROM Pin	28	CY7C286	5962-92071(W)	t _{AA} = 60, 70	150 @ 60	Now
512K	64Kx8—Registered	28S	CY7C287	5962-90913(W)	t _{SA/CO} = 55/20, 65/25	150 @ 65	Now
512K	64Kx8—Registered	28S	CY7C287	5962-92065(O)	t _{SA/CO} = 55/20, 65/25	150 @ 65	Now
1M	128Kx8	32	CY27H010		t _{AA} = 35, 45, 55, 70	85@35	Now

PLDs

	Organization	Pins	Part Number	JAN/SMD Number ^{[1]*}	Speed (ns/MHz)	I _{CC} (mA @ ns/MHz)	883 Availability
PAL20	16L8, 16R8, 16R6, 16R4	20	PAL16XX	5962-92338(O)	t _{PD} = 7, 10	180 @ 7	Now
PALC20	16L8, 16R8, 16R6, 16R4	20	PALC16XX	5962-88678(W)	t _{PD} = 20, 30, 40	70 @ 20	Now
PALC20	16L8, 16R8, 16R6, 16R4	20	PALC16XX	5962-88713(O)	t _{PD} = 20, 30, 40	70 @ 20	Now
PALCE20	16V8—Macrocell	20S	PALCE16V8	5962-89839	t _{PD} /S/CO = 10/10/7	130 @ 10	Now
PLD24	22V10C—Macrocell	24S	PAL22V10C	5962-91760(O)	t _{PD} /S/CO = 10/3.6/7.5	190 @ 10	Now
PLD24	22V10C—Macrocell	24S	PAL22VP10C	5962-91760(O)	t _{PD} /S/CO = 10/3.6/7.5	190 @ 10	Now
PLDC24	22V10—Macrocell	24S	PALC22V10	5962-87539(W)	t _{PD} /S/CO = 25/18/15	100 @ 25	Now
PLD24	22V10—Macrocell	24S	PALC22V10B	5962-87539(W)	t _{PD} /S/CO = 20/17/15	100 @ 20	Now
PLDC24	22V10—Macrocell	24S	PALC22V10	5962-88670(O)	t _{PD} /S/CO = 25/18/15	100 @ 25	Now
PLD24	22V10—Macrocell	24S	PALC22V10B	5962-88670(O)	t _{PD} /S/CO = 15/12/10	120 @ 15	Now
PLDC24	22V10—Macrocell	24S	PALC22V10B	M38510/507(W)	t _{PD} /S/CO = 15/12/10	120 @ 15	Now
PLDC24	22V10—Macrocell	24S	PALC22V10B	M38510/508(O)	t _{PD} /S/CO = 15/12/10	120 @ 15	Now
PLDC24	22V10D—Macrocell	24S	PALC22V10D	5962-89841(O)	t _{PD} /S/CO = 10/6/7	130@10	Now
PLDC24	20G10—Generic	24S	PLDC20G10	5962-88637(O)	t _{PD} /S/CO = 20/17/15	80 @ 30	Now
PLDC24	20RA10—Asynchronous	24S	PLD20RA10	5962-90555(O)	t _{PD} /SU/CO = 20/10/20	100 @ 25	Now
PLDC24	20RA10—Asynchronous	24S	PLD20RA10	5962-90989(W)	t _{PD} /SU/CO = 20/10/20	100@25	Now
PLDC28	7C330—State Machine	28S	CY7C330	5962-89546(W)	50, 40, 28 MHz	180 @ 40 MHz	Now
PLDC28	7C330—State Machine	28S	CY7C330	5926-90802(O)	50, 40, 28 MHz	180 @ 40 MHz	Now
PLDC28	7C331—Asynchronous	28S	CY7C331	5962-90754(W)	t _{PD} = 25, 30, 40	200 @ 20 MHz	Now
PLDC28	7C331—Asynchronous	28S	CY7C331	5962-89855(O)	t _{PD} = 25, 30, 40	200 @ 20 MHz	Now
PLDC28	7C332—Combinatorial	28S	CY7C332	5962-91584(W)	t _{PD} = 20, 25, 30	200 @ 24 MHz	Now
PLD28	7C335—Synchronous	28S	CY7C335	5862-94510(W)	f _{MAX5} = 66.6, 50, 83	160 @ 66.6 MHz	Now
MAX28	7C344—32 Macrocell	28S	CY7C344/B	5962-90611(W)	t _{PD} = 12, 20, 25, 35	220@25	Now
MAX40	7C343—64 Macrocell	40/44	CY7C343/B	5962-92158(W)	t _{PD} = 15, 20, 25, 30, 35	225@25	Now
MAX68	7C342—128 Macrocell	68	CY7C342/B	5962-89468(W)	t _{PD} = 15, 20, 25, 30, 35	320@30	Now
MAX84	7C341—192 Macrocell	84	CY7C341/B	5962-92062(W)	t _{PD} = 20, 25, 30, 35, 40	480@30	Now
MAX100	7C346—128 Macrocell	84/100	CY7C346/B	5962-91344(W)	t _{PD} = 20, 25, 30, 35	320@35	Now
PLDC28	7C361—State Machine	28S	CY7C361		100, 83, 66 MHz	150 @ 100 MHz	Now
37X-44	7C371—32 Macrocell	44	CY7C371	5962-94684(O)	f _{MAX} /t _S /t _{CO} =83MHz/10/10	260@83	Now
37X-44	7C372—64 Macrocell	44	CY7C372	5962-94688(O)	f _{MAX} /t _S /t _{CO} =83MHz/8/8	300@83	Now
37X-84	7C373—64 Macrocell	84	CY7C373	5962-94689(O)	f _{MAX} /t _S /t _{CO} =83MHz/8/8	300@83	Now
37X-84	7C374—128 Macrocell	84	CY7C374	5962-94713(O)	f _{MAX} /t _S /t _{CO} =83MHz/8/8	370@83	Now
37X-160	7C375—128 Macrocell	160	CY7C375		f _{MAX} /t _S /t _{CO} =83MHz/8/8	270@83	Now
FLASH370-160	7C376—192 Macrocell	160	CY7C376		f _{MAX} /t _S /t _{CO} =83MHz/12/12	300/TBD	4Q95
FLASH370-240	7C377—192 Macrocell	240	CY7C377		f _{MAX} /t _S /t _{CO} =83MHz/12/12	300/TBD	4Q95
FLASH370-160	7C378—256 Macrocell	160	CY7C378		f _{MAX} /t _S /t _{CO} =83MHz/12/12	300/TBD	2Q95



Military Product Selector Guide

VMEbus Interface Products

Organization	Pins	Part Number	JAN/SMD Number	Speed (MHz)	I _{CC} (mA)	883 Availability
VME Interface Controller	144/160	VIC068A	5962-92010	64	250	Now
VME Address Controller	144/160	VAC068A	5962-92009	50	150	Now
64-Bit VIC	144/160	VIC64		64	300	Now
Slave VME Interface Controller	64	CY7C960				Now
Bus Interface Logic Circuit	64	CY7C964	5962-95511			Now

Communication Products

Organization	Pins	Part Number	Speed (Mbps)	I _{CC} (mA)	Packages	883 Availability
HOTLink Transmitter	28	CY7B923	160 – 330	95	L	Now
HOTLink Receiver	28	CY7B933	160 – 330	165	L	Now

Modules

Size	Organization	Pins	Part Number	Packages	Speed (ns)	I _{CC} (mA @ ns)	883 Availability
1M	32Kx32 SRAM	66	CYM1828	HG01	t _{AA} = 35, 45, 55, 70	200@35	Now
2M	64Kx32 SRAM	60	CYM1830	HD06	t _{AA} = 35, 45, 55	880@35	Now
4M	128Kx32 SRAM	66	CYM1838	HG01	t _{AA} = 25, 30, 35	720@25	Now
4M	512Kx8 SRAM	32	CYM1466	HD12	t _{AA} = 35, 45, 55, 70, 85, 100, 120	350@35	Now

Notes:

The following Cypress facilities have been granted Level Q (QML) certification by DESC:

Operation	Facility	Location
Fab	Fab2	Round Rock, TX
	Fab3	Bloomington, MN
Assy/Test	Bangkok	Bangkok, Thailand
Test	San Jose	San Jose, CA

All of the above products are available with processing to MIL-STD-883D at a minimum. Many of these products are also available either to SMDs (Standardized Military Drawings) or to JAN slash sheets.

The speed and power specifications listed above cover the full military temperature range.

Modules are available with MIL-STD-883D components. These modules are assembled and screened to the proposed JEDEC military processing standard for modules.

W = Windowed Package
 O = Opaque Package
 HD = Hermetic DIP Module

100K ECL devices are available only to extended temperature range.

22S stands for 22-pin 300-mil DIP.
 24S stands for 24-pin 300-mil DIP.
 28S stands for 28-pin 300-mil DIP.
 32S stands for 32-pin 300-mil DIP.

HOTLink is a trademark of Cypress Semiconductor.



Military Ordering Information

DESC SMD (Standardized Military Drawing) Approvals^[1] (continued)

SMD Number	Cypress ^[2] Part Number	Package ^[3]		Product Description
		Description	Type	
5962-86846 01VX	CY7C404-10DMB	18.3 DIP	D4	64 x 5 FIFO
5962-86846 012X	CY7C404-10LMB	20 S LCC	L61	64 x 5 FIFO
5962-86846 02VX	CY7C404-15DMB	18.3 DIP	D4	64 x 5 FIFO
5962-86846 022X	CY7C404-15LMB	20 S LCC	L61	64 x 5 FIFO
5962-86846 03VX	CY7C404-25DMB	18.3 DIP	D4	64 x 5 FIFO
5962-86846 032X	CY7C404-25LMB	20 S LCC	L61	64 x 5 FIFO
5962-86859 17LX	CY7C166AL-35DMB	24.3 DIP	D14	16K x 4 SRAM w/OE
5962-86859 17XX	CY7C166AL-35LMB	28 R TLCC	L54	16K x 4 SRAM w/OE
5962-86859 18LX	CY7C166A-35DMB	24.3 DIP	D14	16K x 4 SRAM w/OE
5962-86859 24YX	CY7C164A-35DMB	22.3 DIP	D10	16K x 4 SRAM
5962-86875 03XX	CY7C130-55DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962-86875 03ZX	CY7C131-55LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962-86875 04XX	CY7C130-45DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962-86875 04ZX	CY7C131-45LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962-86875 11XX	CY7C140-55DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962-86875 11ZX	CY7C141-55LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962-86875 12XX	CY7C140-45DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962-86875 12ZX	CY7C141-45LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962-86875 19XX	CY7C130-35DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962-86875 19ZX	CY7C131-35LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962-86875 20XX	CY7C140-35DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962-86875 20ZX	CY7C141-35LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962-87515 05KX	CY7C261-45TMB	24 CP	T73	8K x 8 UV EPROM
5962-87515 05LX	CY7C261-45WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962-87515 053X	CY7C261-45QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962-87515 06KX	CY7C261-55TMB	24 CP	T73	8K x 8 UV EPROM
5962-87515 06LX	CY7C261-55WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962-87515 063X	CY7C261-55QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962-87515 07KX	CY7C261-35TMB	24 CP	T73	8K x 8 UV EPROM
5962-87515 07LX	CY7C261-35WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962-87515 073X	CY7C261-35QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962-87515 08JX	CY7C264-35WMB	24.6 DIP	W12	8K x 8 UV EPROM
5962-87515 08KX	CY7C263-35TMB	24 CP	T73	8K x 8 UV EPROM
5962-87515 08LX	CY7C263-35WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962-87515 083X	CY7C263-35QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962-87515 09JX	CY7C264-45WMB	24.6 DIP	W12	8K x 8 UV EPROM
5962-87515 09KX	CY7C263-45TMB	24 CP	T73	8K x 8 UV EPROM
5962-87515 09LX	CY7C263-45WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962-87515 093X	CY7C263-45QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962-87515 10JX	CY7C264-55WMB	24.6 DIP	W12	8K x 8 UV EPROM
5962-87515 10KX	CY7C263-55TMB	24 CP	T73	8K x 8 UV EPROM
5962-87515 10LX	CY7C263-55WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962-87515 103X	CY7C263-55QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962-87515 11JX	CY7C264-25WMB	24.6 DIP	W12	8K x 8 UV EPROM
5962-87515 11KX	CY7C263-25TMB	24 CP	T73	8K x 8 UV EPROM
5962-87515 11LX	CY7C263-25WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962-87515 113X	CY7C263-25QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962-87515 12KX	CY7C261-25TMB	24 CP	T73	8K x 8 UV EPROM
5962-87515 12LX	CY7C261-25WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962-87515 123X	CY7C261-25QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962-87529 01LX	CY7C245-45WMB	24.3 DIP	W14	2K x 8 Registered UV PROM
5962-87529 013X	CY7C245-45QMB	28 S LCC	Q64	2K x 8 Registered UV PROM
5962-87529 02LX	CY7C245-35WMB	24.3 DIP	W14	2K x 8 Registered UV PROM
5962-87529 023X	CY7C245-35QMB	28 S LCC	Q64	2K x 8 Registered UV PROM
5962-87539 01LX	PALC22V10-25WMB	24.3 DIP	W14	24-Pin CMOS UV EPLD
5962-87539 013X	PALC22V10-25QMB	28 S LCC	Q64	24-Pin CMOS UV EPLD
5962-87539 02LX	PALC22V10-30WMB	24.3 DIP	W14	24-Pin CMOS UV EPLD
5962-87539 023X	PALC22V10-30QMB	28 S LCC	Q64	24-Pin CMOS UV EPLD
5962-87539 03LX	PALC22V10-40WMB	24.3 DIP	W14	24-Pin CMOS UV EPLD
5962-87539 04LX	PALC22V10B-20WMB	24.3 DIP	W14	24-Pin CMOS UV EPLD
5962-87539 043X	PALC22V10B-20QMB	28 S LCC	Q64	24-Pin CMOS UV EPLD



Military Ordering Information

DESC SMD (Standardized Military Drawing) Approvals^[1] (continued)

SMD Number	Cypress ^[2] Part Number	Package ^[3]		Product Description
		Description	Type	
5962-88636 03KX	CY7C235A-40KMB	24 CP	K73	1K x 8 Registered PROM
5962-88636 03LX	CY7C235A-40DMB	24.3 DIP	D14	1K x 8 Registered PROM
5962-88636 033X	CY7C235A-40LMB	28 S LCC	L64	1K x 8 Registered PROM
5962-88636 04KX	CY7C235A-30KMB	24 CP	K73	1K x 8 Registered PROM
5962-88636 04LX	CY7C235A-30DMB	24.3 DIP	D14	1K x 8 Registered PROM
5962-88636 043X	CY7C235A-30LMB	28 S LCC	L64	1K x 8 Registered PROM
5962-88636 05KX	CY7C235A-25KMB	24 CP	K73	1K x 8 Registered PROM
5962-88636 05LX	CY7C235A-25DMB	24.3 DIP	D14	1K x 8 Registered PROM
5962-88636 053X	CY7C235A-25LMB	28 S LCC	L64	1K x 8 Registered PROM
5962-88637 01KX	PLDC20G10-40KMB	24 CP	K73	Generic CMOS PLD
5962-88637 01LX	PLDC20G10-40DMB	24.3 DIP	D14	Generic CMOS PLD
5962-88637 02KX	PLDC20G10-30KMB	24 CP	K73	Generic CMOS PLD
5962-88637 02LX	PLDC20G10-30DMB	24.3 DIP	D14	Generic CMOS PLD
5962-88637 023X	PLDC20G10-30LMB	28 S LCC	L64	Generic CMOS PLD
5962-88662 03MX	CY7C199-55KMB	28 CP	K74	32K x 8 SRAM
5962-88662 03NX	CY7C199-55DMB	28.3 DIP	D22	32K x 8 SRAM
5962-88662 03UX	CY7C199-55LMB	28 R LCC	L54	32K x 8 SRAM
5962-88662 03XX	CY7C198-55DMB	28.6 DIP	D16	32K x 8 SRAM
5962-88662 03YX	CY7C198-55LMB	32 R LCC	L55	32K x 8 SRAM
5962-88662 04MX	CY7C199-45KMB	28 CP	K74	32K x 8 SRAM
5962-88662 04NX	CY7C199-45DMB	28.3 DIP	D22	32K x 8 SRAM
5962-88662 04UX	CY7C199-45LMB	28 R LCC	L54	32K x 8 SRAM
5962-88662 04XX	CY7C198-45DMB	28.6 DIP	D16	32K x 8 SRAM
5962-88662 04YX	CY7C198-45LMB	32 R LCC	L55	32K x 8 SRAM
5962-88662 05MX	CY7C199-35KMB	28 CP	K74	32K x 8 SRAM
5962-88662 05NX	CY7C199-35DMB	28.3 DIP	D22	32K x 8 SRAM
5962-88662 05UX	CY7C199-35LMB	28 R LCC	L54	32K x 8 SRAM
5962-88662 05XX	CY7C198-35DMB	28.6 DIP	D16	32K x 8 SRAM
5962-88662 05YX	CY7C198-35LMB	32 R LCC	L55	32K x 8 SRAM
5962-88662 06MX	CY7C199-25KMB	28 CP	K74	32K x 8 SRAM
5962-88662 06NX	CY7C199-25DMB	28.3 DIP	D22	32K x 8 SRAM
5962-88662 06UX	CY7C199-25LMB	28 R LCC	L54	32K x 8 SRAM
5962-88662 06XX	CY7C198-25DMB	28.6 DIP	D16	32K x 8 SRAM
5962-88662 06YX	CY7C198-25LMB	32 R LCC	L55	32K x 8 SRAM
5962-88662 07NX	CY7C199-20DMB	28.3 DIP	D22	32K x 8 SRAM
5962-88662 07MX	CY7C199-20KMB	28 CP	K74	32K x 8 SRAM
5962-88662 07UX	CY7C199-20LMB	28 R LCC	L54	32K x 8 SRAM
5962-88662 07YX	CY7C198-20LMB	32 R LCC	L55	32K x 8 SRAM
5962-88662 08NX	CY7C199-15DMB	28.3 DIP	D22	32K x 8 SRAM
5962-88662 08MX	CY7C199-15KMB	28 CP	K74	32K x 8 SRAM
5962-88662 08UX	CY7C199-15LMB	28 R LCC	L54	32K x 8 SRAM
5962-88662 08YX	CY7C198-15LMB	32 R LCC	L55	32K x 8 SRAM
5962-88669 02XX	CY7C428-65DMB	28.6 DIP	D16	2K x 9 FIFO
5962-88669 02YX	CY7C429-65DMB	28.3 DIP	D22	2K x 9 FIFO
5962-88669 02ZX	CY7C429-65LMB	32 R LCC	L55	2K x 9 FIFO
5962-88669 03XX	CY7C428-50DMB	28.6 DIP	D16	2K x 9 FIFO
5962-88669 03YX	CY7C429-50DMB	28.3 DIP	D22	2K x 9 FIFO
5962-88669 03ZX	CY7C429-50LMB	32 R LCC	L55	2K x 9 FIFO
5962-88669 04XX	CY7C428-40DMB	28.6 DIP	D16	2K x 9 FIFO
5962-88669 04YX	CY7C429-40DMB	28.3 DIP	D22	2K x 9 FIFO
5962-88669 04ZX	CY7C429-40LMB	32 R LCC	L55	2K x 9 FIFO
5962-88669 05XX	CY7C428-30DMB	28.6 DIP	D16	2K x 9 FIFO
5962-88669 05YX	CY7C429-30DMB	28.3 DIP	D22	2K x 9 FIFO
5962-88669 05ZX	CY7C429-30LMB	32 R LCC	L55	2K x 9 FIFO
5962-88670 01KX	PALC22V10-25KMB	24 CP	K73	24-Pin CMOS PLD
5962-88670 01LX	PALC22V10-25DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962-88670 013X	PALC22V10-25LMB	28 S LCC	L64	24-Pin CMOS PLD
5962-88670 02KX	PALC22V10-30KMB	24 CP	K73	24-Pin CMOS PLD
5962-88670 02LX	PALC22V10-30DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962-88670 023X	PALC22V10-30LMB	28 S LCC	L64	24-Pin CMOS PLD



Military Ordering Information

DESC SMD (Standardized Military Drawing) Approvals^[1] (continued)

SMD Number	Cypress ^[2] Part Number	Package ^[3]		Product Description
		Description	Type	
5962-88735 01KX	CY7C245-45KMB	24 CP	K73	2K x 8 Registered PROM
5962-88735 01LX	CY7C245-45DMB	24.3 DIP	D14	2K x 8 Registered PROM
5962-88735 013X	CY7C245-45LMB	28 S LCC	L64	2K x 8 Registered PROM
5962-88735 02KX	CY7C245-35KMB	24 CP	K73	2K x 8 Registered PROM
5962-88735 02LX	CY7C245-35DMB	24.3 DIP	D14	2K x 8 Registered PROM
5962-88735 023X	CY7C245-35LMB	28 S LCC	L64	2K x 8 Registered PROM
5962-88735 03KX	CY7C245A-35KMB	24 CP	K73	2K x 8 Registered PROM
5962-88735 03LX	CY7C245A-35DMB	24.3 DIP	D14	2K x 8 Registered PROM
5962-88735 033X	CY7C245A-35LMB	28 S LCC	L64	2K x 8 Registered PROM
5962-88735 04KX	CY7C245A-25KMB	24 CP	K73	2K x 8 Registered PROM
5962-88735 04LX	CY7C245A-25DMB	24.3 DIP	D14	2K x 8 Registered PROM
5962-88735 043X	CY7C245A-25LMB	28 S LCC	L64	2K x 8 Registered PROM
5962-89468 01XX	CY7C342-35RMB	68 PGA	R68	128-Macrocell UV EPLD
5962-89468 01YX	CY7C342-35HMB	68 SOJ	H81	128-Macrocell UV EPLD
5962-89468 01ZX	CY7C342-35TMB	68 QFP	T91	128-Macrocell UV EPLD
5962-89468 02XX	CY7C342-30RMB	68 PGA	R68	128-Macrocell UV EPLD
5962-89468 02YX	CY7C342-30HMB	68 SOJ	H81	128-Macrocell UV EPLD
5962-89468 02ZX	CY7C342-30TMB	68 QFP	T91	128-Macrocell UV EPLD
5962-89468 03XX	CY7C342B-25RMB	68 PGA	R68	128-Macrocell UV EPLD
5962-89468 03YX	CY7C342B-25HMB	68 SOJ	H81	128-Macrocell UV EPLD
5962-89468 03ZX	CY7C342B-25TMB	68 QFP	T91	128-Macrocell UV EPLD
5962-89468 04XX	CY7C342B-20RMB	68 PGA	R68	128-Macrocell UV EPLD
5962-89468 04YX	CY7C342B-20HMB	68 SOJ	H81	128-Macrocell UV EPLD
5962-89468 04ZX	CY7C342B-20TMB	68 QFP	T91	128-Macrocell UV EPLD
5962-89484 01MXX	CY7C265-50WMB	28 CP	W22	8K x 8 Registered UV PROM
5962-89484 01M3X	CY7C265-50QMB	28 S LCC	Q64	8K x 8 Registered UV PROM
5962-89484 02MXX	CY7C265-25WMB	28 CP	W22	8K x 8 Registered UV PROM
5962-89484 02M3X	CY7C265-25QMB	28 S LCC	Q64	8K x 8 Registered UV PROM
5962-89484 03MXX	CY7C265-15WMB	28 CP	W22	8K x 8 Registered UV PROM
5962-89484 03M3X	CY7C265-15QMB	28 S LCC	Q64	8K x 8 Registered UV PROM
5962-89517 01YX	CY7C9101-45LMB	68 S LCC	L81	16-Bit Slice
5962-89517 02YX	CY7C9101-35LMB	68 S LCC	L81	16-Bit Slice
5962-89523 01EX	CY7C403-10DMB	16.3 DIP	D2	64 x 4 FIFO
5962-89523 012X	CY7C403-10LMB	20 S LCC	L61	64 x 4 FIFO
5962-89523 02EX	CY7C403-15DMB	16.3 DIP	D2	64 x 4 FIFO
5962-89523 022X	CY7C403-15LMB	20 S LCC	L61	64 x 4 FIFO
5962-89523 05EX	CY7C401-10DMB	16.3 DIP	D2	64 x 4 FIFO
5962-89523 052X	CY7C401-10LMB	20 S LCC	L61	64 x 4 FIFO
5962-89523 06EX	CY7C401-15DMB	16.3 DIP	D2	64 x 4 FIFO
5962-89523 062X	CY7C401-15LMB	20 S LCC	L61	64 x 4 FIFO
5962-89524 03XX	CY7C195L-45DMB	28.3 DIP	D22	64K x 4 SRAM
5962-89524 04XX	CY7C195L-35DMB	28.3 DIP	D22	64K x 4 SRAM
5962-89524 05XX	CY7C195L-25DMB	28.3 DIP	D22	64K x 4 SRAM
5962-89537 01UX	CY7C251-65QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962-89537 01YX	CY7C251-65WMB	28.3 DIP	W22	16K x 8 UV EPROM
5962-89537 01ZX	CY7C251-65TMB	28 CP	T74	16K x 8 UV EPROM
5962-89537 02UX	CY7C251-55QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962-89537 02YX	CY7C251-55WMB	28.3 DIP	W22	16K x 8 UV EPROM
5962-89537 02ZX	CY7C251-55TMB	28 CP	T74	16K x 8 UV EPROM
5962-89537 03UX	CY7C251-45QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962-89537 03YX	CY7C251-45WMB	28.3 DIP	W22	16K x 8 UV EPROM
5962-89537 03ZX	CY7C251-45TMB	28 CP	T74	16K x 8 UV EPROM
5962-89538 01XX	CY7C254-65WMB	28.6 DIP	W16	16K x 8 UV EPROM
5962-89538 02XX	CY7C254-55WMB	28.6 DIP	W16	16K x 8 UV EPROM
5962-89538 03UX	CY7C254-45QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962-89538 03XX	CY7C254-45WMB	28.3 DIP	W16	16K x 8 UV EPROM
5962-89538 03ZX	CY7C254-45TMB	28 CP	T74	16K x 8 UV EPROM



Military Ordering Information

DESC SMD (Standardized Military Drawing) Approvals^[1] (continued)

SMD Number	Cypress ^[2] Part Number	Package ^[3]		Product Description
		Description	Type	
5962-89815 03LX	CY7C245A-18WMB	24.3 DIP	W14	2K x 8 Registered UV EPROM
5962-89815 03KX	CY7C245A-18TMB	24 CP	T73	2K x 8 Registered UV EPROM
5962-89815 033X	CY7C245A-18QMB	28 S LCC	Q64	2K x 8 Registered UV EPROM
5962-89817 01XX	CY7C271-55WMB	28.3 DIP	W16	32K x 8 UV EPROM
5962-89817 01YX	CY7C271-55TMB	28 CP	T74	32K x 8 UV EPROM
5962-89817 01ZX	CY7C271-55QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962-89817 02XX	CY7C271-45WMB	28.3 DIP	W16	32K x 8 UV EPROM
5962-89817 02YX	CY7C271-45TMB	28 CP	T74	32K x 8 UV EPROM
5962-89817 02ZX	CY7C271-45QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962-89817 03XX	CY7C271-35WMB	28.3 DIP	W22	32K x 8 UV EPROM
5962-89817 03YX	CY7C271-35TMB	28 CP	T74	32K x 8 UV EPROM
5962-89817 03ZX	CY7C271-35QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962-89817 04UX	CY7C274-55WMB	28.6 DIP	W16	32K x 8 UV EPROM
5962-89817 04ZX	CY7C274-55QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962-89817 05UX	CY7C274-45WMB	28.6 DIP	W16	32K x 8 UV EPROM
5962-89817 05ZX	CY7C274-45QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962-89817 06UX	CY7C274-35WMB	28.6 DIP	W16	32K x 8 UV EPROM
5962-89817 06ZX	CY7C274-35QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962-89841 01KX	PALC22V10D-30KMB	24 CP	K73	CMOS EE PLD
5962-89841 01LX	PALC22V10D-30DMB	24.3 DIP	D14	CMOS EE PLD
5962-89841 013X	PALC22V10D-30LMB	28 S LCC	L64	CMOS EE PLD
5962-89841 02KX	PALC22V10D-20KMB	24 CP	K73	CMOS EE PLD
5962-89841 02LX	PALC22V10D-20DMB	24.3 DIP	D14	CMOS EE PLD
5962-89841 023X	PALC22V10D-20LMB	28 S LCC	L64	CMOS EE PLD
5962-89841 03KX	PALC22V10D-15KMB	24 CP	K73	CMOS EE PLD
5962-89841 03LX	PALC22V10D-15DMB	24.3 DIP	D14	CMOS EE PLD
5962-89841 033X	PALC22V10D-15LMB	28 S LCC	L64	CMOS EE PLD
5962-89841 04KX	PALC22V10D-25KMB	24 CP	K73	CMOS EE PLD
5962-89841 04LX	PALC22V10D-25DMB	24.3 DIP	D14	CMOS EE PLD
5962-89841 043X	PALC22V10D-25LMB	28 S LCC	L64	CMOS EE PLD
5962-89841 05KX	PALC22V10D-15KMB	24 CP	K73	CMOS EE PLD
5962-89841 05LX	PALC22V10D-15DMB	24.3 DIP	D14	CMOS EE PLD
5962-89841 053X	PALC22V10D-15LMB	28 S LCC	L64	CMOS EE PLD
5962-89841 06KX	PALC22V10D-10KMB	24 CP	K73	CMOS EE PLD
5962-89841 06LX	PALC22V10D-10DMB	24.3 DIP	D14	CMOS EE PLD
5962-89841 063X	PALC22V10D-10LMB	28 S LCC	L64	CMOS EE PLD
5962-89855 01MYX	CY7C331-40KMB	28 CP	K74	Asynchronous PLD
5962-89855 01MZX	CY7C331-40YMB	28 S JCQ	Y64	Asynchronous PLD
5962-89855 01M3X	CY7C331-40LMB	28 S LCC	L64	Asynchronous PLD
5962-89855 02MXX	CY7C331-30DMB	28.3 DIP	D22	Asynchronous PLD
5962-89855 02MYX	CY7C331-30KMB	28 CP	K74	Asynchronous PLD
5962-89855 02MZX	CY7C331-30YMB	28 S JCQ	Y64	Asynchronous PLD
5962-89855 03MXX	CY7C331-25DMB	28.3 DIP	D22	Asynchronous PLD
5962-89855 03MYX	CY7C331-25KMB	28 CP	K74	Asynchronous PLD
5962-89855 03MZX	CY7C331-25YMB	28 S JCQ	Y64	Asynchronous PLD
5962-89855 03M3X	CY7C331-25LMB	28 S LCC	L64	Asynchronous PLD
5962-89863 02XX	CY7C420-65DMB	28.6 DIP	D16	512 x 9 FIFO
5962-89863 02YX	CY7C421-65DMB	28.3 DIP	D22	512 x 9 FIFO
5962-89863 02ZX	CY7C421-65LMB	32 R LCC	L55	512 x 9 FIFO
5962-89863 03XX	CY7C420-50DMB	28.6 DIP	D16	512 x 9 FIFO
5962-89863 03YX	CY7C421-50DMB	28.3 DIP	D22	512 x 9 FIFO
5962-89863 03ZX	CY7C421-50LMB	32 R LCC	L55	512 x 9 FIFO
5962-89863 04XX	CY7C420-40DMB	28.6 DIP	D16	512 x 9 FIFO
5962-89863 04YX	CY7C421-40DMB	28.3 DIP	D22	512 x 9 FIFO
5962-89863 04ZX	CY7C421-40LMB	32 R LCC	L55	512 x 9 FIFO
5962-89863 05XX	CY7C420-30DMB	28.6 DIP	D16	512 x 9 FIFO
5962-89863 05YX	CY7C421-30DMB	28.3 DIP	D22	512 x 9 FIFO
5962-89863 05ZX	CY7C421-30LMB	32 R LCC	L55	512 x 9 FIFO
5962-89863 06XX	CY7C420-25DMB	28.6 DIP	D16	512 x 9 FIFO
5962-89863 06YX	CY7C421-25DMB	28.3 DIP	D22	512 x 9 FIFO
5962-89863 06ZX	CY7C421-25LMB	32 R LCC	L55	512 x 9 FIFO



Military Ordering Information

DESC SMD (Standardized Military Drawing) Approvals^[1] (continued)

SMD Number	Cypress ^[2] Part Number	Package ^[3]		Product Description	
		Description	Type		
5962-90715	06MUX	CY7C433-30DMB	28.3 DIP	D22	4K x 9 FIFO
5962-90715	06MXX	CY7C432-30DMB	28.6 DIP	D16	4K x 9 FIFO
5962-90715	06MZX	CY7C433-30LMB	32 R LCC	L55	4K x 9 FIFO
5962-90754	01MYX	CY7C331-40TMB	28 CP	T74	Asynchronous UV PLD
5962-90754	01MZX	CY7C331-40HMB	28 S JCO	H64	Asynchronous UV PLD
5962-90754	02MYX	CY7C331-30TMB	28 CP	T74	Asynchronous UV PLD
5962-90754	02MZX	CY7C331-30HMB	28 S JCO	H64	Asynchronous UV PLD
5962-90754	02M3X	CY7C331-30QMB	28 S LCC	Q64	Asynchronous UV PLD
5962-90754	03MXX	CY7C331-25WMB	28.3 DIP	W22	Asynchronous UV PLD
5962-90754	03MYX	CY7C331-25TMB	28 CP	T74	Asynchronous UV PLD
5962-90754	03MZX	CY7C331-25HMB	28 S JCO	H64	Asynchronous UV PLD
5962-90754	03M3X	CY7C331-25QMB	28 S LCC	Q64	Asynchronous UV PLD
5962-90803	01MLX	CY7C261-55DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962-90803	01M3X	CY7C261-55LMB	28 S LCC	L64	8K x 8 OTP PROM
5962-90803	02MLX	CY7C261-45DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962-90803	02M3X	CY7C261-45LMB	28 S LCC	L64	8K x 8 OTP PROM
5962-90803	03MLX	CY7C261-35DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962-90803	03M3X	CY7C261-35LMB	28 S LCC	L64	8K x 8 OTP PROM
5962-90803	04MLX	CY7C261-25DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962-90803	04M3X	CY7C261-25LMB	28 S LCC	L64	8K x 8 OTP PROM
5962-90803	05MJX	CY7C264-55DMB	24.6 DIP	D12	8K x 8 OTP PROM
5962-90803	05MLX	CY7C263-55DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962-90803	05M3X	CY7C263-55LMB	28 S LCC	L64	8K x 8 OTP PROM
5962-90803	06MJX	CY7C264-45DMB	24.6 DIP	D12	8K x 8 OTP PROM
5962-90803	06MLX	CY7C263-45DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962-90803	06M3X	CY7C263-45LMB	28 S LCC	L64	8K x 8 OTP PROM
5962-90803	07MJX	CY7C264-35DMB	24.6 DIP	D12	8K x 8 OTP PROM
5962-90803	07MLX	CY7C263-35DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962-90803	07M3X	CY7C263-35LMB	28 S LCC	L64	8K x 8 OTP PROM
5962-90803	08MJX	CY7C264-25DMB	24.6 DIP	D12	8K x 8 OTP PROM
5962-90803	08MLX	CY7C263-25DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962-90803	08M3X	CY7C263-25LMB	28 S LCC	L64	8K x 8 OTP PROM
5962-90831	01MXX	CY7C269-60DMB	28.3 DIP	D22	8K x 8 REG OTP PROM
5962-90831	02MXX	CY7C269-50DMB	28.3 DIP	D22	8K x 8 REG OTP PROM
5962-90831	03MXX	CY7C269-25DMB	28.3 DIP	D22	8K x 8 REG OTP PROM
5962-90831	04MXX	CY7C269-18DMB	28.3 DIP	D22	8K x 8 REG OTP PROM
5962-90913	01MXX	CY7C287-65WMB	28.3 DIP	W22	64K x 8 Registered UV PROM
5962-90913	01MYX	CY7C287-65QMB	32 R LCC	Q55	64K x 8 Registered UV PROM
5962-90913	02MXX	CY7C287-55WMB	28.3 DIP	W22	64K x 8 Registered UV PROM
5962-90913	02MYX	CY7C287-55QMB	32 R LCC	Q55	64K x 8 Registered UV PROM
5962-90930	01MXX	CY7C269-50WMB	28.3 DIP	W22	8K x 8 Registered UV PROM
5962-90930	01MYX	CY7C269-50TMB	28 CP	T74	8K x 8 Registered UV PROM
5962-90930	01M3X	CY7C269-50QMB	28 S LCC	Q64	8K x 8 Registered UV PROM
5962-90930	02MXX	CY7C269-25WMB	28.3 DIP	W22	8K x 8 Registered UV PROM
5962-90930	02MYX	CY7C269-25TMB	28 CP	T74	8K x 8 Registered UV PROM
5962-90930	02M3X	CY7C269-25QMB	28 S LCC	Q64	8K x 8 Registered UV PROM
5962-90930	03MXX	CY7C269-15WMB	28.3 DIP	W22	8K x 8 Registered UV PROM
5962-90930	03MYX	CY7C269-15TMB	28 CP	T74	8K x 8 Registered UV PROM
5962-90930	03M3X	CY7C269-15QMB	28 S LCC	Q64	8K x 8 Registered UV PROM
5962-90989	01MLX	PLDC20RA10-35WMB	24.3 DIP	W14	Asynchronous CMOS UV EPLD
5962-90989	02MLX	PLDC20RA10-25WMB	24.3 DIP	W14	Asynchronous CMOS UV EPLD
5962-90989	02M3X	PLDC20RA10-25QMB	28 S LCC	Q64	Asynchronous CMOS UV EPLD
5962-90989	03MLX	PLDC20RA10-20WMB	24.3 DIP	W14	Asynchronous CMOS UV EPLD
5962-90989	03M3X	PLDC20RA10-20QMB	28 S LCC	Q64	Asynchronous CMOS UV EPLD
5962-91518	01MZX	CY10E474L-7KMB	24 CP	K63	1K x 4 ECL SRAM
5962-91518	02MZX	CY10E474L-5KMB	24 CP	K63	1K x 4 ECL SRAM
5962-91584	01MYX	CY7C332-25TMB	28 CP	T74	Registered Combinatorial UV EPLD
5962-91584	01MZX	CY7C332-25HMB	28 S JCO	H64	Registered Combinatorial UV EPLD
5962-91584	02MYX	CY7C332-20TMB	28 CP	T74	Registered Combinatorial UV EPLD
5962-91584	02MZX	CY7C332-20HMB	28 S JCO	H64	Registered Combinatorial UV EPLD
5962-91584	02M3X	CY7C332-20QMB	28 S LCC	Q64	Registered Combinatorial UV EPLD



Military Ordering Information

DESC SMD (Standardized Military Drawing) Approvals^[1] (continued)

SMD Number	Cypress ^[2] Part Number	Package ^[3]		Product Description	
		Description	Type		
5962-92213	03MRX	CY54FCT240ATDMB	20.3 DIP	D6	Octal Buffer/Driver I
5962-92213	03M2X	CY54FCT240ATLMB	20 S LCC	L61	Octal Buffer/Driver I
5962-92213	05MRX	CY54FCT240CTDMB	20.3 DIP	D6	Octal Buffer/Driver I
5962-92213	05M2X	CY54FCT240CTLMB	20 S LCC	L61	Octal Buffer/Driver I
5962-92214	01MRX	CY54FCT245TDMB	20.3 DIP	D6	Octal Tranceiver
5962-92214	01M2X	CY54FCT245TLMB	20 S LCC	L61	Octal Tranceiver
5962-92214	03MRX	CY54FCT245ATDMB	20.3 DIP	D6	Octal Tranceiver
5962-92214	03M2X	CY54FCT245ATLMB	20 S LCC	L61	Octal Tranceiver
5962-92214	05MRX	CY54FCT245CTDMB	20.3 DIP	D6	Octal Tranceiver
5962-92214	05M2X	CY54FCT245CTLMB	20 S LCC	L61	Octal Tranceiver
5962-92215	01MRX	CY54FCT273TDMB	20.3 DIP	D6	Octal D Flip-Flops
5962-92215	01M2X	CY54FCT273TLMB	20 S LCC	L61	Octal D Flip-Flops
5962-92215	03MRX	CY54FCT273ATDMB	20.3 DIP	D6	Octal D Flip-Flops
5962-92215	03M2X	CY54FCT273ATLMB	20 S LCC	L61	Octal D Flip-Flops
5962-92215	05MRX	CY54FCT273CTDMB	20.3 DIP	D6	Octal D Flip-Flops
5962-92215	05M2X	CY54FCT273CTLMB	20 S LCC	L61	Octal D Flip-Flops
5962-92217	01MRX	CY54FCT373TDMB	20.3 DIP	D6	Octal Transparent Latch
5962-92217	01M2X	CY54FCT373TLMB	20 S LCC	L61	Octal Transparent Latch
5962-92217	02MRX	CY54FCT373ATDMB	20.3 DIP	D6	Octal Transparent Latch
5962-92217	02M2X	CY54FCT373ATLMB	20 S LCC	L61	Octal Transparent Latch
5962-92217	03MRX	CY54FCT373CTDMB	20.3 DIP	D6	Octal Transparent Latch
5962-92217	03M2X	CY54FCT373CTLMB	20 S LCC	L61	Octal Transparent Latch
5962-92218	02MRX	CY54FCT374TDMB	20.3 DIP	D6	Octal D Flip-Flop W/OE
5962-92218	02M2X	CY54FCT374TLMB	20 S LCC	L61	Octal D Flip-Flop W/OE
5962-92218	04MRX	CY54FCT374ATDMB	20.3 DIP	D6	Octal D Flip-Flop W/OE
5962-92218	04M2X	CY54FCT374ATLMB	20 S LCC	L61	Octal D Flip-Flop W/OE
5962-92218	06MRX	CY54FCT374CTDMB	20.3 DIP	D6	Octal D Flip-Flop W/OE
5962-92218	06M2X	CY54FCT374CTLMB	20 S LCC	L61	Octal D Flip-Flop W/OE
5962-92219	01MRX	CY54FCT377TDMB	20.3 DIP	D6	Octal D Flip-Flop W/CE
5962-92219	01M2X	CY54FCT377TLMB	20 S LCC	L61	Octal D Flip-Flop W/CE
5962-92219	02MRX	CY54FCT377ATDMB	20.3 DIP	D6	Octal D Flip-Flop W/CE
5962-92219	02M2X	CY54FCT377ATLMB	20 S LCC	L61	Octal D Flip-Flop W/CE
5962-92219	03MRX	CY54FCT377CTDMB	20.3 DIP	D6	Octal D Flip-Flop W/CE
5962-92219	03M2X	CY54FCT377CTLMB	20 S LCC	L61	Octal D Flip-Flop W/CE
5962-92221	01MLX	CY54FCT543TDMB	24.3 DIP	D14	Octal Tranceiver/Reg
5962-92221	01M3X	CY54FCT543TLMB	28 S LCC	L64	Octal Tranceiver/Reg
5962-92221	02MLX	CY54FCT543ATDMB	24.3 DIP	D14	Octal Tranceiver/Reg
5962-92221	02M3X	CY54FCT543ATLMB	28 S LCC	L41	Octal Tranceiver/Reg
5962-92221	03MLX	CY54FCT543CTDMB	24.3 DIP	D14	Octal Tranceiver/Reg
5969-92221	03M3X	CY54FCT543CTLMB	28 S LCC	L64	Octal Tranceiver/Reg
5962-92222	01MRX	CY54FCT574TDMB	20.3 DIP	D6	Octal D Register
5962-92222	01M2X	CY54FCT574TLMB	20 S LCC	L61	Octal D Register
5962-92222	03MRX	CY54FCT574ATDMB	20.3 DIP	D6	Octal D Register
5962-92222	03M2X	CY54FCT574ATLMB	20 S LCC	L61	Octal D Register
5962-92222	05MRX	CY54FCT574CTDMB	20.3 DIP	D6	Octal D Register
5962-92222	05M2X	CY54FCT574CTLMB	20 S LCC	L61	Octal D Register
5962-92223	01MLX	CY54FCT646TDMB	24.3 DIP	D14	Octal Reg Tranceiver
5962-92223	01M3X	CY54FCT646TLMB	28 S LCC	L64	Octal Reg Tranceiver
5962-92223	03MLX	CY54FCT646ATDMB	24.3 DIP	D14	Octal Reg Tranceiver
5962-92223	03M3X	CY54FCT646ATLMB	28 S LCC	L41	Octal Reg Tranceiver
5962-92223	05MLX	CY54FCT646CTDMB	24.3 DIP	D14	Octal Reg Tranceiver
5969-92223	05M3X	CY54FCT646CTLMB	28 S LCC	L64	Octal Reg Tranceiver
5962-92230	01MLX	CY54FCT825ATDMB	24.3 DIP	D14	Octal Register W/OE
5962-92230	01M3X	CY54FCT825ATLMB	28 S LCC	L64	Octal Register W/OE
5962-92230	03MLX	CY54FCT825BTDMB	24.3 DIP	D14	Octal Register W/OE
5962-92230	03M3X	CY54FCT825BTLMB	28 S LCC	L41	Octal Register W/OE
5962-92230	05MLX	CY54FCT825CTDMB	24.3 DIP	D14	Octal Register W/OE
5969-92230	05M3X	CY54FCT825CTLMB	28 S LCC	L64	Octal Register W/OE
5962-92233	02MEX	CY54FCT138TDMB	16.3 DIP	D2	1-of-8 Decoder
5962-92233	02M2X	CY54FCT138TLMB	20 S LCC	L61	1-of-8 Decoder



Military Ordering Information

DESC SMD (Standardized Military Drawing) Approvals^[1] (continued)

SMD Number	Cypress ^[2] Part Number	Package ^[3]		Product Description
		Description	Type	
5962-93112 01MXX	CY7B992-7LMB	32 R LCC	D2	Prog Skew Clock Buffer
5962-93124 01MXX	CY7C453-30DMB	32.3 DIP	D32	2K x 9 Clocked FIFO
5962-93124 01MYX	CY7C453-30LMB	32 R LCC	L55	2K x 9 Clocked FIFO
5962-93124 02MXX	CY7C453-20DMB	32.3 DIP	D32	2K x 9 Clocked FIFO
5962-93124 02MYX	CY7C453-20LMB	32 R LCC	L55	2K x 9 Clocked FIFO
5962-93124 03MXX	CY7C453-14DMB	32.3 DIP	D32	2K x 9 Clocked FIFO
5962-93124 03MYX	CY7C453-14LMB	32 R LCC	L55	2K x 9 Clocked FIFO
5962-93144 01MZX	CY7C346-35RMB	100 PGA	R100	128-Macrocell UV EPLD
5962-93144 01MUX	CY7C346-35HMB	84 S JCO	H84	128-Macrocell UV EPLD
5962-93144 02MZX	CY7C346-30RMB	100 PGA	R100	128-Macrocell UV EPLD
5962-93144 02MUX	CY7C346-30HMB	84 S JCO	H84	128-Macrocell UV EPLD
5962-93152 01MXX	CY7C464-40DMB	28.6 DIP	TBD	32K X 9 FIFO
5962-93152 01MYX	CY7C464-40LMB	32 R LCC	L55	32K X 9 FIFO
5962-93152 02MXX	CY7C464-25DMB	28.6 DIP	TBD	32K X 9 FIFO
5962-93152 02MYX	CY7C464-25LMB	32 R LCC	L55	32K X 9 FIFO
5962-93152 03MXX	CY7C464-20DMB	28.6 DIP	TBD	32K X 9 FIFO
5962-93152 03MYX	CY7C464-20LMB	32 R LCC	L55	32K X 9 FIFO
5962-93166 01MXX	CY7C271-55DMB	28.3 DIP	D22	32K x 8 OTP PROM
5962-93166 02MXX	CY7C271-45DMB	28.3 DIP	D22	32K x 8 OTP PROM
5962-93166 03MXX	CY7C271-35DMB	28.3 DIP	D22	32K x 8 OTP PROM
5962-93173 01MXX	CY7C451-30DMB	32.3 DIP	D32	512 x 9 Clocked FIFO
5962-93173 01MYX	CY7C451-30LMB	32 R LCC	L55	512 x 9 Clocked FIFO
5962-93173 02MXX	CY7C451-20DMB	32.3 DIP	D32	512 x 9 Clocked FIFO
5962-93173 02MYX	CY7C451-20LMB	32 R LCC	L55	512 x 9 Clocked FIFO
5962-93173 03MXX	CY7C451-14DMB	32.3 DIP	D32	512 x 9 Clocked FIFO
5962-93173 03MYX	CY7C451-14LMB	32 R LCC	L55	512 x 9 Clocked FIFO
5962-93225 01MXX	CY7C196-45DMB	28.3 DIP	D22	64K x 4 SRAM w/OE
5962-93225 01MYX	CY7C196-45LMB	28 R LCC	L54	64K x 4 SRAM w/OE
5962-93225 02MXX	CY7C196-35DMB	28.3 DIP	D22	64K x 4 SRAM w/OE
5962-93225 02MYX	CY7C196-35LMB	28 R LCC	L54	64K x 4 SRAM w/OE
5962-93225 03MXX	CY7C196-25DMB	28.3 DIP	D22	64K x 4 SRAM w/OE
5962-93225 03MYX	CY7C196-25LMB	28 R LCC	L54	64K x 4 SRAM w/OE
5962-93225 04MXX	CY7C196-20DMB	28.3 DIP	D22	64K x 4 SRAM w/OE
5962-93225 04MYX	CY7C196-20LMB	28 R LCC	L54	64K x 4 SRAM w/OE
5962-94510 01MXX	CY7C335-50WMB	28.3 DIP	W22	Synchronous UV EPLD
5962-94510 01MYX	CY7C335-50HMB	28 S JCO	H64	Synchronous UV EPLD
5962-94510 01MZX	CY7C335-50QMB	28 S LCC	Q64	Synchronous UV EPLD
5962-94510 02MXX	CY7C335-66WMB	28.3 DIP	W22	Synchronous UV EPLD
5962-94510 02MYX	CY7C335-66HMB	28 S JCO	H64	Synchronous UV EPLD
5962-94510 02MZX	CY7C335-66QMB	28 S LCC	Q64	Synchronous UV EPLD
5962-94510 03MXX	CY7C335-83WMB	28.3 DIP	W22	Synchronous UV EPLD
5962-94510 03MYX	CY7C335-83HMB	28 S JCO	H64	Synchronous UV EPLD
5962-94510 03MZX	CY7C335-83QMB	28 S LCC	Q64	Synchronous UV EPLD
5962-94522 01MXX	CY7B991-7LMB	32 R LCC	L55	Prog Skew Clock Buffer

Notes:

1. Devices listed have been approved by DESC for the SMD indicated as of the date of publication. Contact your local Cypress representative, or the Cypress SMD Hotline at 408/943-2716, for the latest update.
2. Use the SMD part number as the ordering code.
3. Package: 24.3 DIP = 24-pin 0.300" DIP;
24.6 DIP = 24-pin 0.600" DIP;
28 R LCC = 28 terminal rectangular LCC,
S = Square LCC, TLCC = Thin LCC
24 CP = 24-pin ceramic flatpack (Configuration 1);
FP = brazed flatpack;
PGA = Pin Grid Array.

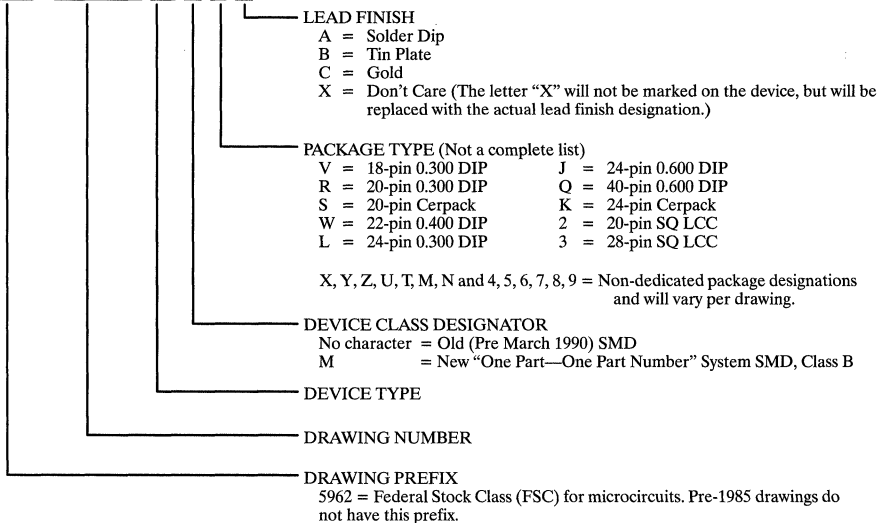
SMD Hotline: 408/943-2716



Military Ordering Information

SMD Ordering Information

5962-XXXXX 01 L X



Cypress Military Marking Information

Manufacturer's identification:

Cypress Logo, CYPRESS, CYP, and CY are trademarks of Cypress Semiconductor Corporation.

Manufacturer's designating symbol or CAGE CODE:

Designating symbol = CETK or ETK

CAGE CODE/FSCM Number = 65786

Country of origin:

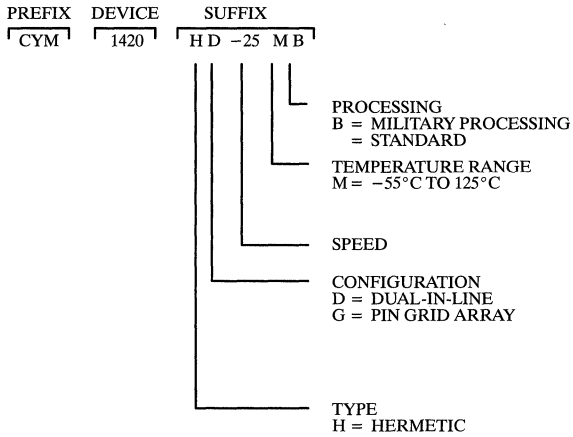
USA = United States of America

THA = Thailand



Military Ordering Information

The codes for module products follow the the format below.



Cypress FSCM #65786



Section Contents

Quality and Reliability

Page Number

Quality, Reliability, and Process Flows	13-1
Tape and Reel Specifications	13-16

Table 1. Cypress Commercial and Industrial Product Screening Flows—Components

Screen	MIL-STD-883 Method	Product Temperature Ranges			
		Commercial 0° C to +70° C; Industrial -40° C to +85° C			
		Level 1		Level 2	
		Plastic	Hermetic	Plastic	Hermetic
Visual/Mechanical					
• Internal Visual	2010	0.4% AQL	100%	0.4% AQL	100%
• Hermeticity – Fine Leak – Gross Leak	1014, Cond A or B (sample) 1014, Cond C	Does Not Apply Does Not Apply	LTPD = 5 100%	Does Not Apply Does Not Apply	LTPD = 5 100%
Burn-in					
• Pre-Burn-in Electrical	Per Device Specification	Does Not Apply	Does Not Apply	100%	100%
• Burn-in	Per Cypress Specification	Does Not Apply	Does Not Apply	100% ^[1]	100% ^[1]
• Post-Burn-in Electrical	Per Device Specification	Does Not Apply	Does Not Apply	100%	100%
• Percent Defective Allowable (PDA)		Does Not Apply	Does Not Apply	5% (max) ^[2]	5% (max) ^[2]
Final Electrical					
• Static (DC), Functional, and Switching (AC) Tests	Per Device Specification 1. At 25° C and Power Supplies Extremes 2. At Hot Temperature and Power Supply Extremes	Not Performed 100%	Not Performed 100%	100% ^[1] 100%	100% ^[1] 100%
Cypress Quality Lot Acceptance					
• External Visual	2009	Note 3	Note 3	Note 3	Note 3
• Final Electrical Conformance	Cypress Method 17-00064	Note 3	Note 3	Note 3	Note 3

Table 2. Cypress Commercial and Industrial Product Screening Flows—Modules

Screen	MIL-STD-883 Method	Product Temperature Ranges	
		Commercial 0° C to +70° C; Industrial -40° C to +85° C	
		Level 1	Level 2
Burn-in			
• Pre-Burn-in Electrical	Per Device Specification	Does Not Apply	100%
• Burn-in	1015	Does Not Apply	100%
• Post-Burn-in Electrical	Per Device Specification	Does Not Apply	100%
• Percent Defective Allowable (PDA)		Does Not Apply	15%
Final Electrical			
• Static (DC), Functional, and Switching (AC) Tests	Per Device Specification 1. At 25° C and Power Supply Extremes 2. At Hot Temperature and Power Supply Extremes	Not Performed 100%	100% 100%
Cypress Quality Lot Acceptance			
• External Visual	2009	Per Cypress Module Specification	Per Cypress Module Specification
• Final Electrical Conformance	Cypress Method 17-00064	Note 3	Note 3

Notes:

- Burn-in is performed as a standard for 12 hours at 150° C.
- Electrical Test is performed after burn-in. Results of this are used to determine PDA percentage.
- Lot acceptance testing is performed on every lot. AOQL (the Average Outgoing Quality Level) for 1994 was <100 PPM.

Table 4. Group A Test Descriptions

Sub-group	Description	Sample Size/Accept No.	
		Components	Modules ^[7]
1	Static Tests at 25°C	116/0	116/0
2	Static Tests at Maximum Rated Operating Temperature	116/0	116/0
3	Static Tests at Minimum Rated Operating Temperature	116/0	116/0
4	Dynamic Tests at 25°C	116/0	116/0
5	Dynamic Tests at Maximum Rated Operating Temperature	116/0	116/0
6	Dynamic Tests at Minimum Rated Operating Temperature	116/0	116/0
7	Functional Tests at 25°C	116/0	116/0
8A	Functional Tests at Maximum Temperature	116/0	116/0
8B	Functional Tests at Minimum Temperature	116/0	116/0
9	Switching Tests at 25°C	116/0	116/0
10	Switching Tests at Maximum Temperature	116/0	116/0
11	Switching Tests at Minimum Temperature	116/0	116/0

Cypress uses an LTPD sampling plan that was developed by the Military to assure product quality. Testing is performed to the sub-groups found to be appropriate for the particular device type. All Military Grade component products have a Group A sample test performed on each inspection lot per MIL-I-38535/MIL-STD-883 and the applicable device specification.

Table 5. Group B Quality Tests

Sub-group	Description	Quantity/Accept # or LTPD	
		Components	Modules ^[7]
2	Resistance to Solvents, Method 2015	3/0	3/0
3	Solderability, Method 2003 ^[8]	22/0	10
5	Bond Strength, Method 2011 ^[9]	15/0	NA

Notes:

7. Military Grade Modules are processed to proposed JEDEC standard flows for MIL-STD-883 compliant modules.
8. Sample size is based upon leads taken from a minimum of 3 devices.
9. Sample size is based upon leads taken from a minimum of 4 devices.

Group B testing is performed for each inspection lot. An inspection lot is defined as a group of material of the same device type, package type and lead finish built within a six week seal period and submitted to Group B testing at the same time.

Table 6. Group C Quality Tests

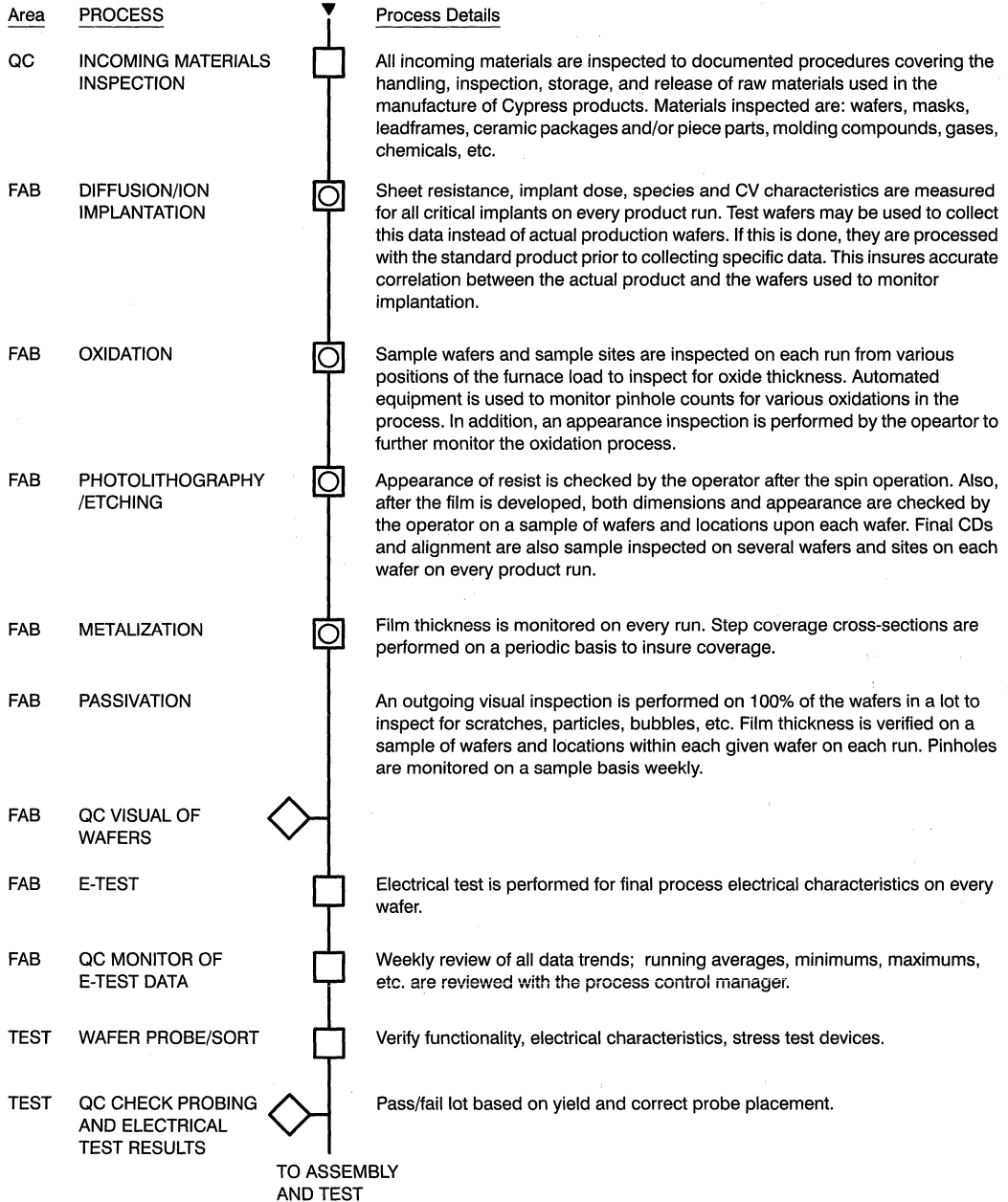
Sub-group	Description	LTPD	
		Components	Modules ^[7]
1	Steady State Life Test, End-Point Electricals, Method 1005, Cond D	45/0	15/0

Group C tests for all Military Grade products are performed on one device type from one inspection lot representing each technology. Sample tests are performed per MIL-I-38535/MIL-STD-883 from each four calendar quarters production of devices, which is based upon the die fabrication date code.

End-point electrical tests and parameters are performed per the applicable device specification.

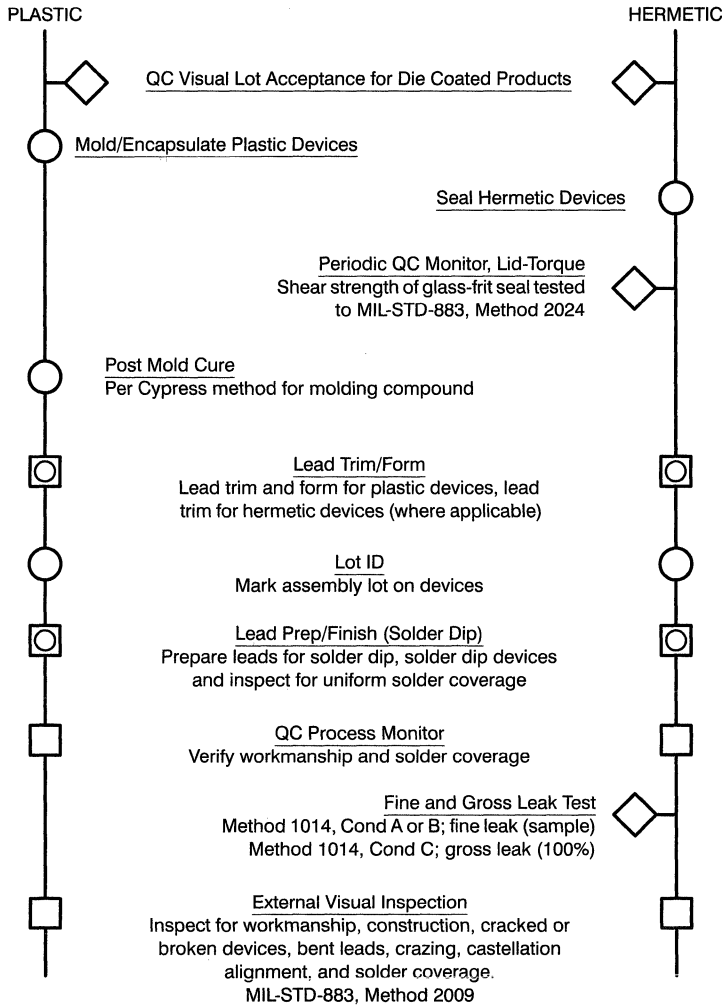
Table 7. Group D Quality Tests (Package Related)

Sub-group	Description	Quantity/Accept # or LTPD	
		Components	Modules ^[7]
1	Physical Dimensions, Method 2016	15/0	15/0
2	Lead Integrity, Seal: Fine and Gross Leak, Method 2004 and 1014	45/0 ^[8]	15/0
3	Thermal Shock, Temp Cycling, Moisture Resistance, Seal: Fine and Gross Leak, Visual Examination, End-Point, Electricals, Methods 1011, 1010, 1004 and 1014	15/0	15/0
4	Mechanical Shock, Vibration - Variable Frequency, Constant Acceleration, Seal: Fine and Gross Leak, Visual Examination, End-Point Electricals, Methods 2002, 2007, 2001 and 1014	15/0	15/0

Product Quality Assurance Flow—Components


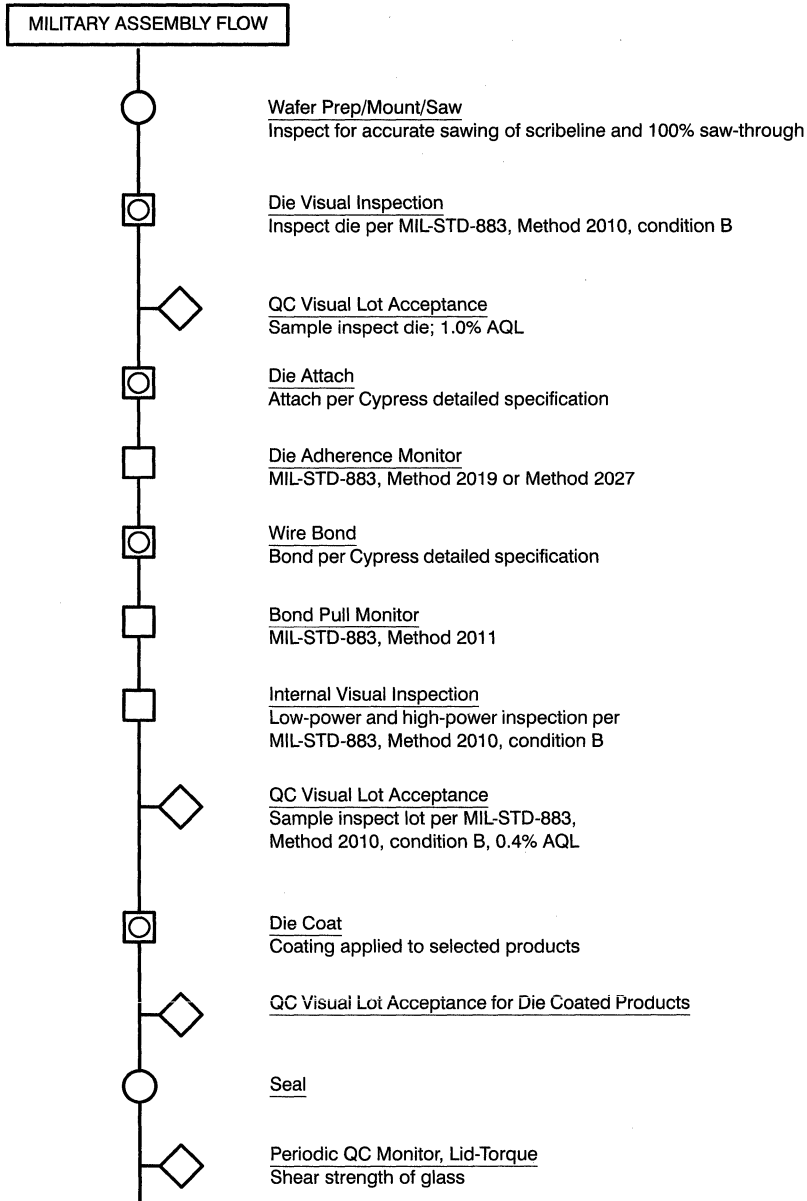
(continued)

Product Quality Assurance Flow—Components (continued)
Commercial and Industrial Product



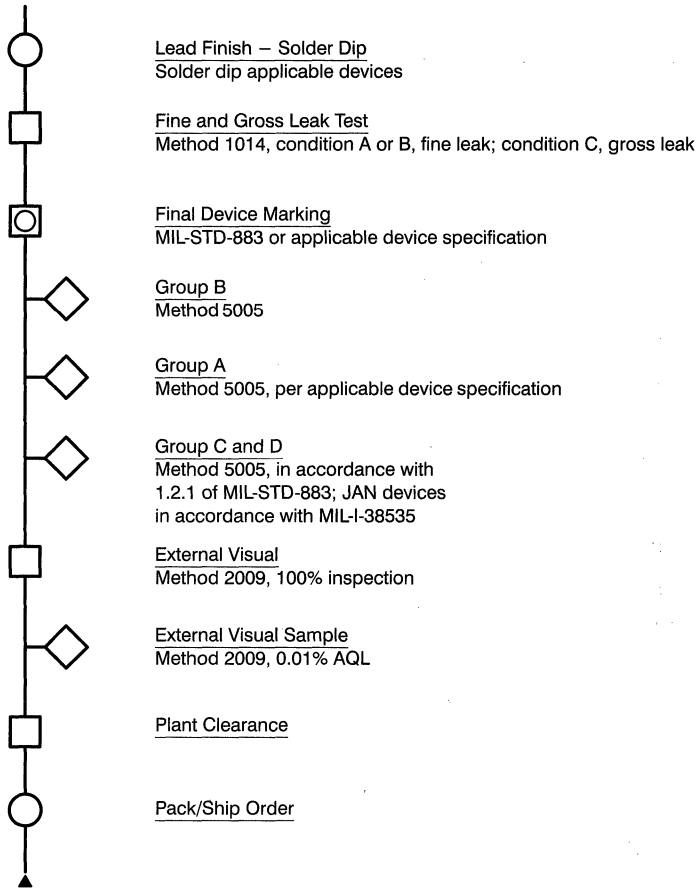
(continued)

Product Quality Assurance Flow—Components
Military Components







(continued)

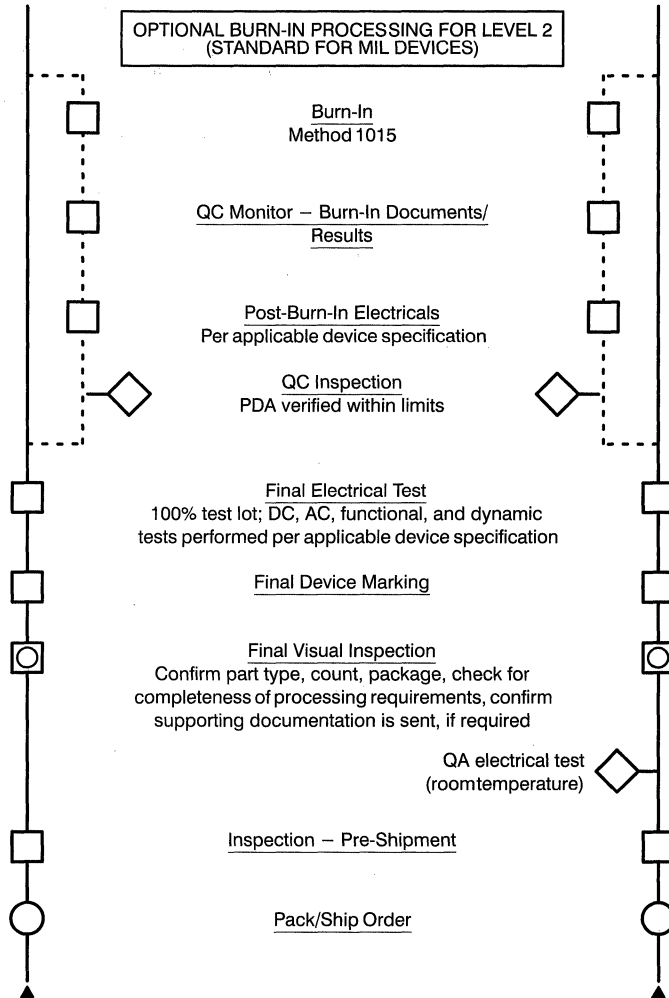
Product Quality Assurance Flow—Components (continued)
Military Components







Key

-  Production Process
-  Test/Inspection
-  Production Process and Test Inspection
-  QC Sample Gate and Inspection

Product Quality Assurance Flow—Modules (continued)



Key

-  Production Process
-  Test/Inspection
-  Production Process and Test Inspection
-  QC Sample gate and inspection



Tape and Reel Specifications

Description

Surface-mounted devices are packaged in embossed tape and wound onto reels for shipment in compliance with Electronics Industries Association Standard EIA-481 Rev. A.

Specifications

Cover Tape

- The cover tape may not extend past the edge of the carrier tapes
- The cover tape shall not cover any part of any sprocket hole.
- The seal of the cover tape to the carrier tape is uniform, with the seal extending over 100% of the length of each pocket, on each side.

- The force to peel back the cover tape from the carrier tape shall be: 20 gms minimal, 70 gms nominal, 100 gms maximal, at a pull-back speed of 300 ± 10 mm/min.

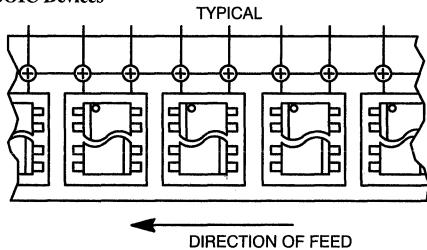
Loading the Reel

Empty pockets between the first and last filled pockets on the tape are permitted within the following requirements:

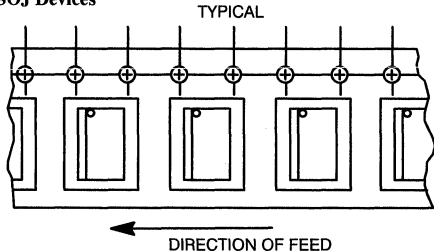
- No two consecutive pockets may be left empty
- No more than a total of ten (10) empty pockets may be on a reel

The surface-mount devices are placed in the carrier tape with the leads down, as shown in *Figure 1*.

SOIC Devices



SOJ Devices



PLCC and LCC Devices

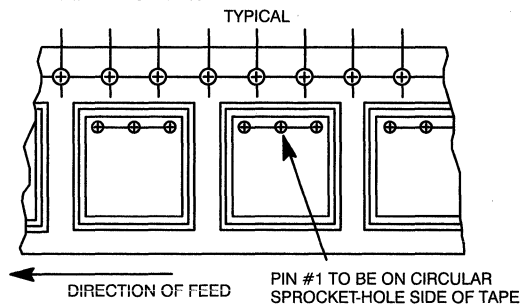


Figure 1. Part Orientation in Carrier Tape

Table 1. Parts Per Reel and Tape Specifications

Package Type	Terminals	Carrier Width (mm)	Part Pitch (mm)	Parts Per Full Reel
PLCC	20	16	12	750
	28	24	16	500
	32R	24	16	500
	44	32	24	400
	52	32	24	400
	68	44	32	250
	84	44	32	250
SOIC	20	24	12	1,000
	24	24	12	1,000
	28	24	12	1,000
SOJ	20	24	3	1,000
	24	24	3	1,000
	28	24	3	1,000
	32 (400 mil)	32	3	1,000
TSOP	32	32	3	1,750
SSOP	20 (150 mil)	16	8	2,000
	24 (150 mil)	16	8	2,000
	48 (300 mil)	32	16	1,000
	56 (300 mil)	32	16	1,000
TSSOP	48	24	12	2,000
	56	24	12	2,000





Section Contents

Packages	Page Number
Thermal Management and Component Reliability	14-1
Package Diagrams	14-11
Module Package Diagrams	14-92

Sales Representatives and Distributors

- Direct Sales Offices
- North American Sales Representatives
- International Sales Representatives
- Distributors

Table 1. Failure Mechanisms and Activation Energies in CMOS Devices

Failure Mode	Approximate Activation Energy (Eq)
Oxide Defects	0.3 eV
Silicon Defects	0.3 eV
Electromigration	0.6 eV
Contact Metallurgy	0.9 eV
Surface Charge	0.5–1.0 eV
Slow Trapping	1.0 eV
Plastic Chemistry	1.0 eV
Polarization	1.0 eV
Microcracks	1.3 eV
Contamination	1.4 eV

To reduce thermally activated reliability failures, Cypress Semiconductor has optimized both their low-power-generating CMOS device fabrication process and their high-heat-dissipation packaging capabilities. Table 2 demonstrates this optimized thermal performance by comparing bipolar, NMOS, and Cypress high-speed 1K SRAM CMOS devices in their respective plastic packaging environments under standard operating conditions.

Table 2. Thermal Performance of Fast 1K SRAMs in Plastic Packages

Technology	Bipolar	NMOS	Cypress CMOS
Device Number	93422	9122	7C122
Speed (ns)	30	25	25
I _{CC} (mA)	150	110	60
V _{CC} (V)	5.0	5.0	5.0
P _{MAX} (mW)	750	550	300
Package RTH (JA) (°C/W)	120	120	70
Junction Temperature (°C) at Datasheet P _{MAX} ^[1]	160	136	91

During its normal operation, the Cypress 7C122 device experiences a 91°C junction temperature, whereas competitive devices in their respective packaging environments see a 45°C and 69°C higher junction temperature. In terms of relative reliability life expectancy, assuming a 1.0-eV activation energy failure mechanism, this translates into an improvement in excess of two orders of magnitude (100x) over the bipolar 93422 device, and more than one order of magnitude (30x) over the NMOS 9122 device.

Thermal Performance Data of Cypress Component Packages

The thermal performance of a semiconductor device in its package is determined by many factors, including package design and construction, packaging materials, chip size, chip thickness, chip attachment process and materials, package size, etc.

Notes:

1. T_{ambient} = 70°C
2. ANSYS Finite Element Software User Guides
3. SDR-IDEAS Pre and Post Processor User Guide

Thermal Resistance (θ_{JA}, θ_{JC})

Thermal resistance is a measure of the ability of a package to transfer the heat generated by the device inside it to the ambient.

For a packaged semiconductor device, heat generated near the junction of the powered chip causes the junction temperature to rise above the ambient temperature. The total thermal resistance is defined as

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

and θ_{JA} physically represents the temperature differential between the die junction and the surrounding ambient at a power dissipation of 1 watt.

The junction temperature is given by the equation

$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JC} + \theta_{CA}]$$

where

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad \text{and} \quad \theta_{CA} = \frac{T_C - T_A}{P}$$

T_A = Ambient temperature at which the device is operated; Most common standard temperature of operation is room temperature to 70°C.

T_J = Junction temperature of the IC chip.

T_C = Temperature of the case (package).

P = Power at which the device operates.

θ_{JC} = Junction-to-case thermal resistance. This is mainly a function of the thermal properties of the materials constituting the package.

θ_{JA} = Junction-to-ambient thermal resistance. The junction-to-ambient environment is a still-air environment.

θ_{CA} = Case-to-ambient thermal resistance. This is mainly dependent on the surface area available for convection and radiation and the ambient conditions among other factors. This can be controlled at the user end by using heat sinks providing greater surface area and better conduction path or by air or liquid cooling.

Thermal Resistance: Finite Element Model

θ_{JC} and θ_{JA} values given in the following figures and listed in the following tables have been obtained by simulation using the Finite element software ANSYS^[2]. SDR-IDEAS Pre and Post processor software^[3] was used to create the finite element model of the packages and the ANSYS input data required for analysis.

SEMI Standard (Semiconductor Equipment and Materials International) method SEMI G30-88^[4] states “heat sink” mounting technique to be the “reference” method for θ_{JC} estimation of ceramic packages. Accordingly, θ_{JC} of packages has been obtained by applying the boundary conditions that correspond to the heat sink mounted on the packages in the simulation.

For θ_{JA} evaluation, SEMI standard specification SEMI G38-87 suggests using a package-mounting arrangement that approximates the application environment. So, in evaluating the θ_{JA}, package on-board configuration is assumed.

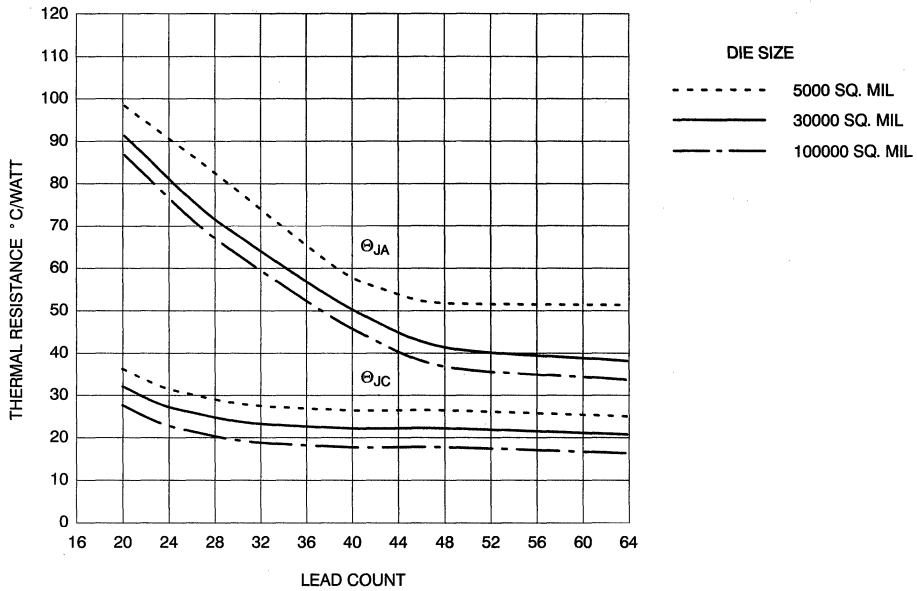


Figure 2. Thermal Resistance of Cypress Plastic DIPs (Package type "P")

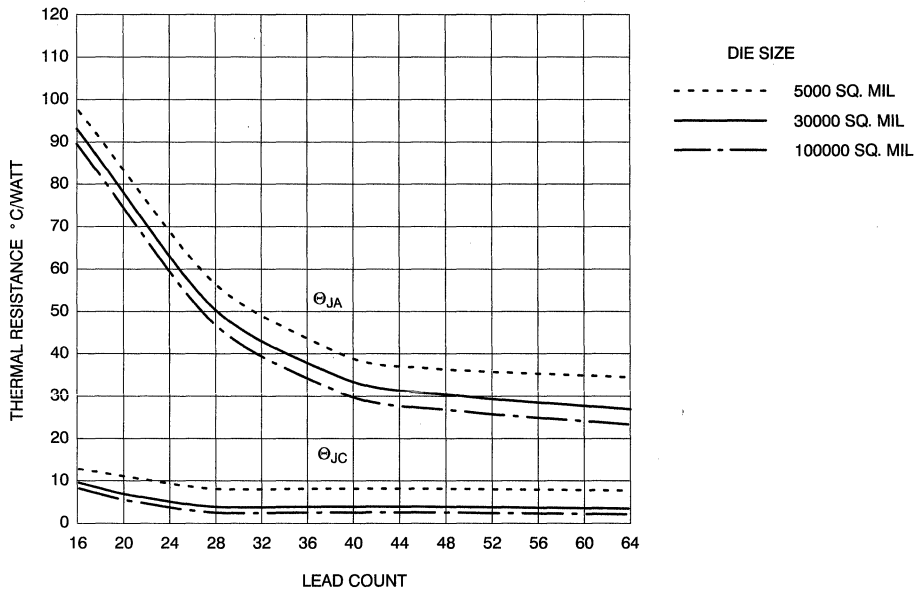
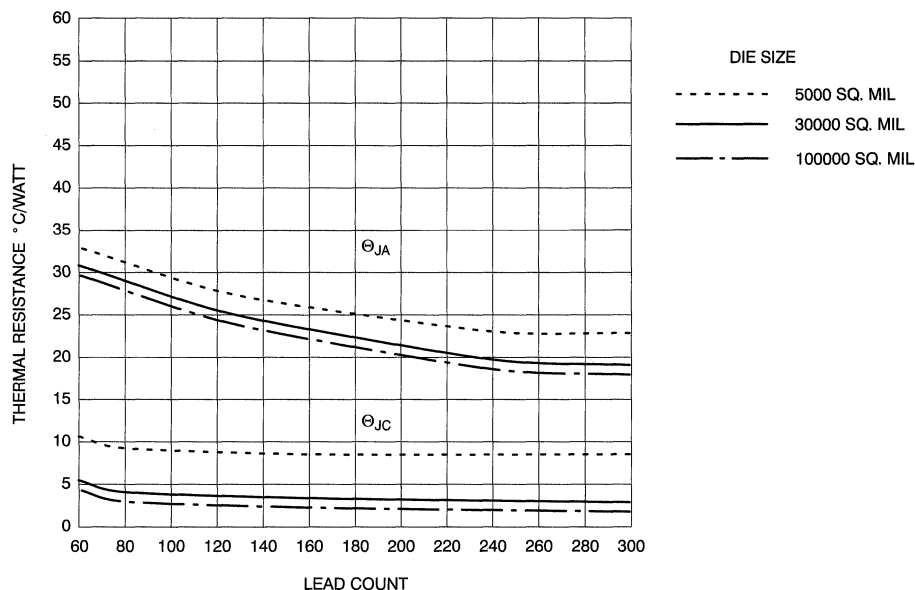


Figure 3. Thermal Resistance of Cypress Ceramic DIPs (Package type "D" and "W")


Figure 6. Thermal Resistance of Cypress Ceramic PGAs
Table 5. Plastic Surface Mount SOIC, SOJ^[8,9]

Package Type "S" and "V"	Paddle Size (mil)	LF Material	Die Size (mil)	Die Area (sq. mil)	θ_{JC} ($^{\circ}C/W$)	θ_{JA} ($^{\circ}C/W$ still air)
16	140 x 170	Copper	98 x 84	8,232	19.0	120
18	140 x 170	Copper	98 x 84	8,232	18.0	116
20	180 x 250	Copper	145 x 213	30,885	17.0	105
24	180 x 250	Copper	145 x 213	30,885	15.4	88
24	170 x 500	Copper	141 x 459	64,719	14.9	85
28	170 x 500	Copper	145 x 213	30,885	16.7	84
28	170 x 500	Copper	141 x 459	64,719	14.4	80

Table 6. Plastic Quad Flatpacks

Package Type "N"	LF Material	Paddle Size (mil)	Die Size (mil)	θ_{JC} ($^{\circ}C/W$)	θ_{JA} ($^{\circ}C/W$ still air)
100	Copper	310 x 310	235 x 235	17	51
144	Copper	310 x 310	235 x 235	18	41
160	Copper	310 x 310	230 x 230	18	40
184	Copper	460 x 460	322 x 311	15	38.5
208	Copper	400 x 400	290 x 320	16	39

Notes:

8. The data in *Table 6* was simulated for SOIC packaging.
9. SOICs and SOJs have very similar thermal resistance characteristics. The thermal resistance values given above apply to SOJ packages also.

Table 10. Die Sizes of Cypress Devices (continued)

Part Number	Size (mil ²)	Part Number	Size (mil ²)
CY7B173	102200	CY7C171A	21228
CY7B174	102200	CY7C172	21228
CY7B180	54600	CY7C172A	21228
CY7B181	54600	CY7C183	65636
CY7B185	27244	CY7C184	65636
CY7B186	27244	CY7C185	30885
CY7B191	73152	CY7C186	30885
CY7B192	73152	CY7C187	30885
CY7B194	73152	CY7C189	4130
CY7C122	6300	CY7C190	4130
CY7C123	6300	CY7C191	68150
CY7C128	20007	CY7C192	68150
CY7C128A	17400	CY7C194	68150
CY7C130	36636	CY7C196	68150
CY7C131	36636	CY7C197	68150
CY7C132	36636	CY7C198	68150
CY7C136	36636	CY7C199	68150
CY7C140	36636	CY7C191 (RAM2.5)	51590
CY7C141	36636	CY7C192 (RAM2.5)	51590
CY7C142	36636	CY7C194 (RAM2.5)	51590
CY7C146	36636	CY7C196 (RAM2.5)	51590
CY7C147	10132	CY7C197 (RAM2.5)	51590
CY7C148	9983	CY7C198 (RAM2.5)	51590
CY7C149	9983	CY7C199 (RAM2.5)	51590
CY7C150	6634	CY7C9122	6300
CY7C157	86460	CY93422A	6300
CY7C161A	30885	PROMs	
CY7C162A	30885	CY7C225	11815
CY7C164A	30885	CY7C235	13900
CY7C166A	30885	CY7C245	19321
CY7C167	21228	CY7C245A	9394
CY7C167A	21228	CY7C251	49536
CY7C168	21228	CY7C254	49536
CY7C168A	21228	CY7C261	28290
CY7C169	21228	CY7C263	28290
CY7C169A	21228	CY7C264	28290
CY7C170	21228	CY7C265	28290
CY7C170A	21228	CY7C266	28290
CY7C171	21228	CY7C268	29400

Table 10. Die Sizes of Cypress Devices (continued)

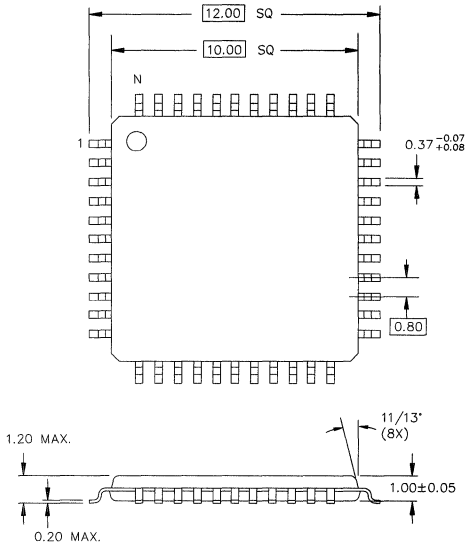
Part Number	Size (mil ²)
Logic	
CY2909A	7968
CY2910A	21750
CY2911A	7968
CY7C2901	11800
CY7C510	30704
CY7C516	29000
CY7C517	29000
CY7C901	11800
CY7C909	7968
CY7C910	21750
CY7C9101	36108
CY7C911	7968

Part Number	Size (mil ²)
ECL	
CY100E301L	14875
CY100E302L	14875
CY100E422	6960
CY100E474	10830
CY100E494	29575
CY10E301L	14875
CY10E302L	14875
CY10E422	6960
CY10E474	10830
CY10E494	29575
Bus Interface	
CY7C964	21460
VAC068	101060
VIC068A	103620
VIC64	103620

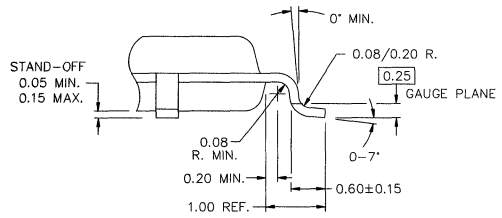
Document #: 38-00190

Thin Quad Flat Packs (continued)

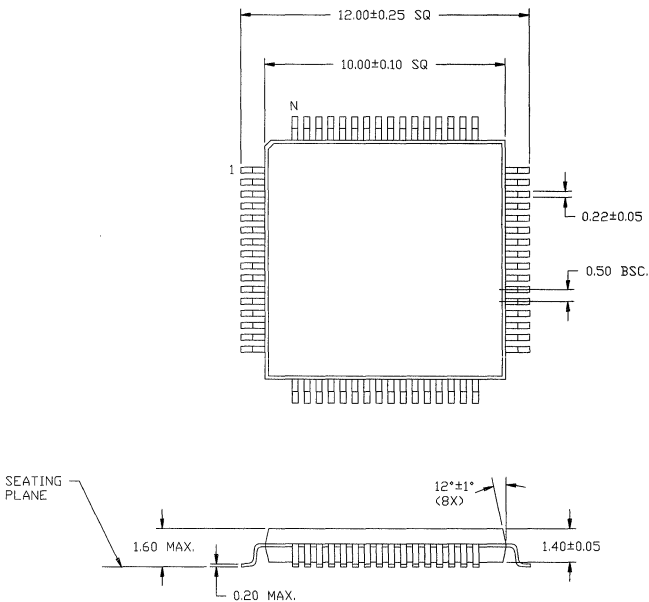
44-Lead Thin Plastic Quad Flat Pack A44



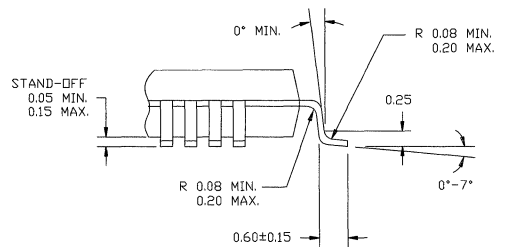
DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.080 MAX.



64-Pin Thin Quad Flat Pack A64

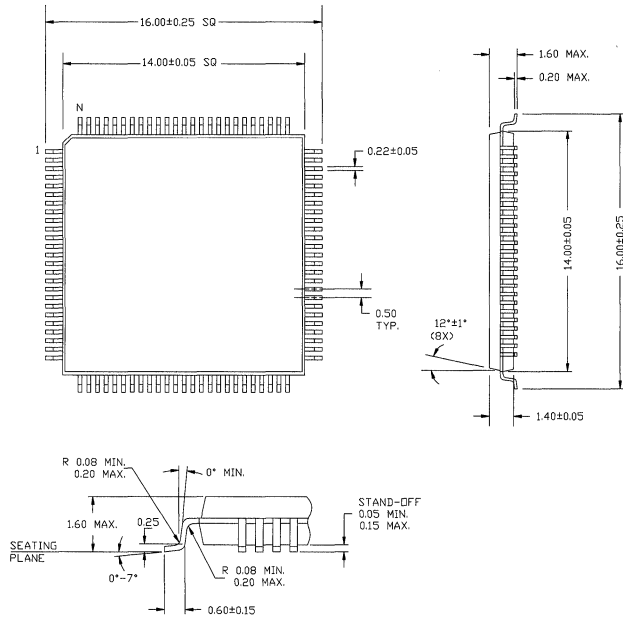


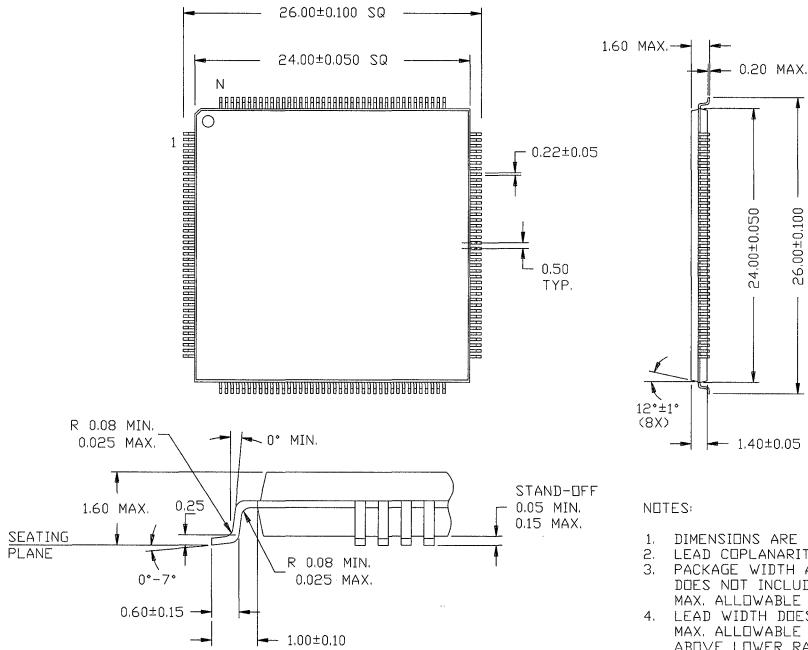
DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.080 MAX.



Thin Quad Flat Packs (continued)

100-Pin Thin Quad Flat Pack A100

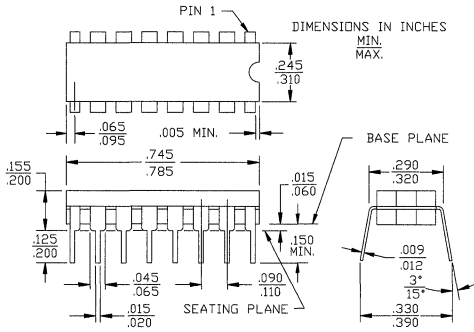


Thin Quad Flat Packs (continued)
160-Lead Thin Quad Flat Pack (TQFP) A160

NOTES:

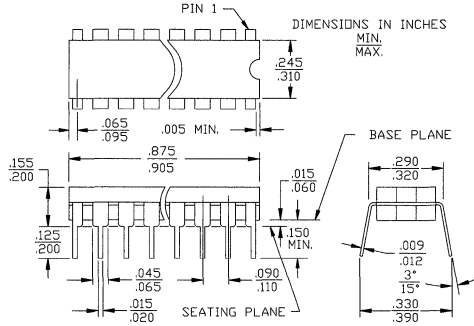
1. DIMENSIONS ARE IN MILLIMETERS.
2. LEAD COPLANARITY 0.100 MAX.
3. PACKAGE WIDTH AND LENGTH (24.00 ± 0.05) DOES NOT INCLUDE MOLD PROTRUSION. MAX. ALLOWABLE PROTRUSION IS 0.25 MM.
4. LEAD WIDTH DOES NOT INCLUDE DAMBAR PROTRUSION. MAX. ALLOWABLE DAMBAR PROTRUSION ABOVE LOWER RADIUS IS 0.08 MM.

Ceramic Dual-In-Line Packages

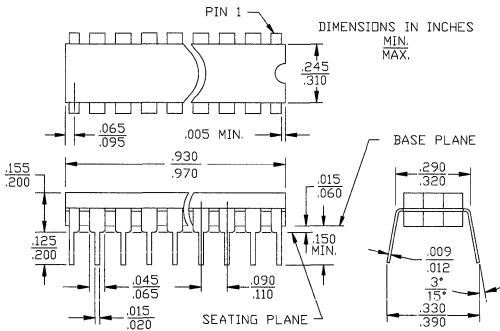
16-Lead (300-Mil) CerDIP D2
MIL-STD-1835 D-2 Config. A



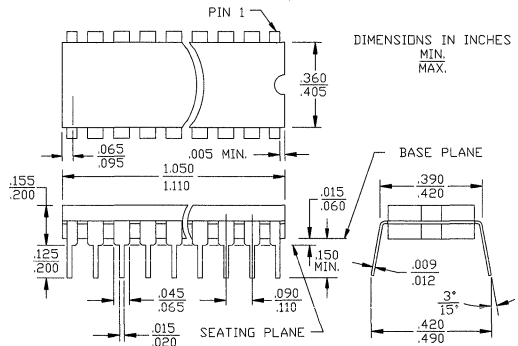
18-Lead (300-Mil) CerDIP D4
MIL-STD-1835 D-8 Config. A



20-Lead (300-Mil) CerDIP D6
MIL-STD-1835 D-8 Config. A

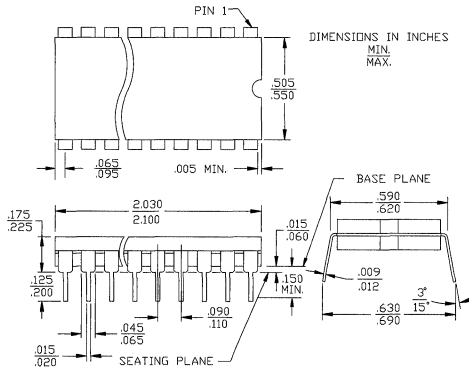


22-Lead (400-Mil) CerDIP D8
MIL-STD-1835 D-7 Config. A

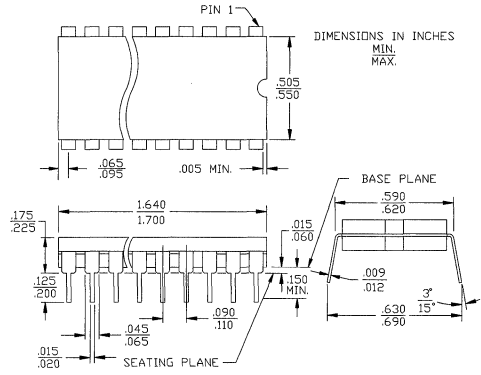


Ceramic Dual-In-Line Packages (continued)

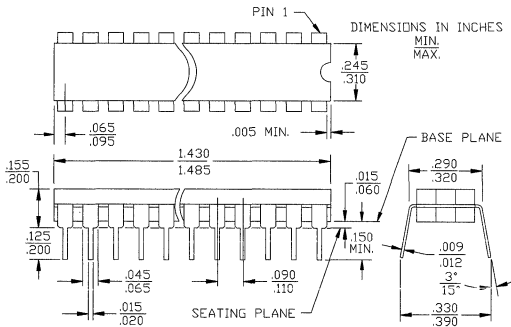
40-Lead (600-Mil) CerDIP D18
MIL-STD-1835 D-5 Config. A



32-Lead (600-Mil) CerDIP D20

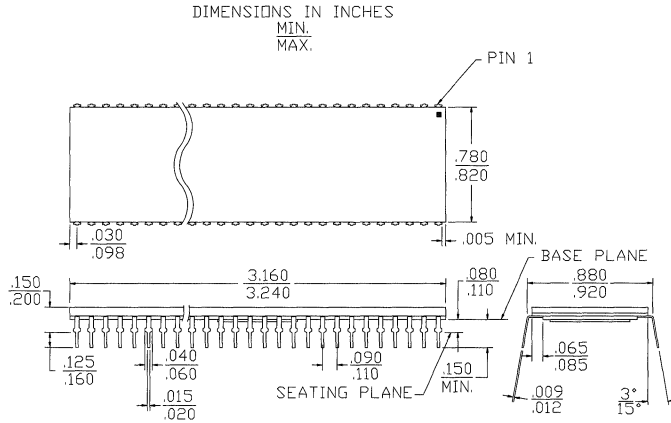


28-Lead (300-Mil) CerDIP D22
MIL-STD-1835 D-15 Config. A

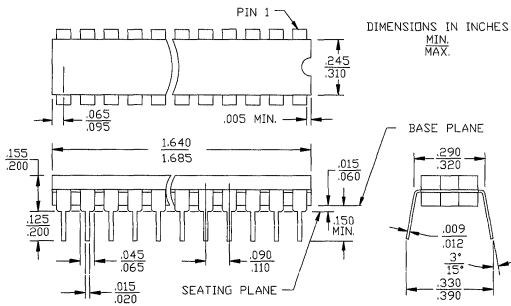


Ceramic Dual-In-Line Packages (continued)

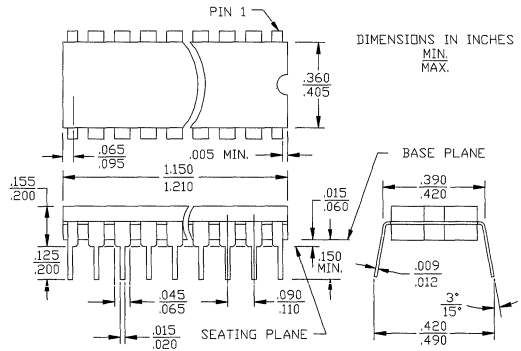
64-Lead (900-Mil) Bottombraze DIP D30

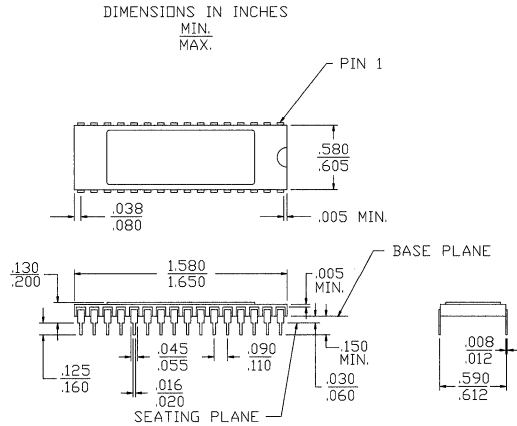
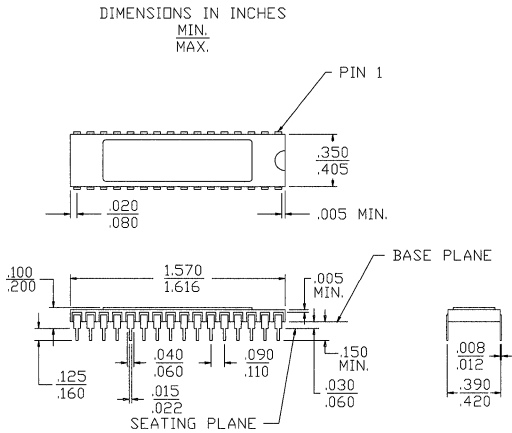


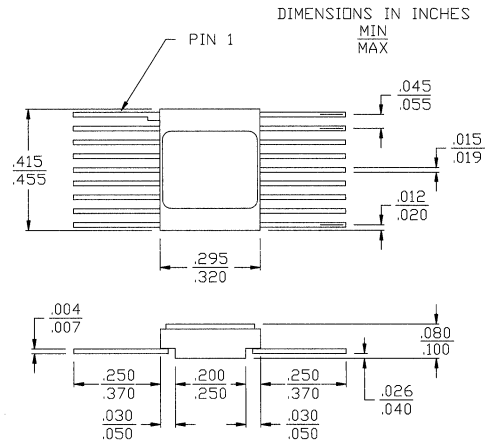
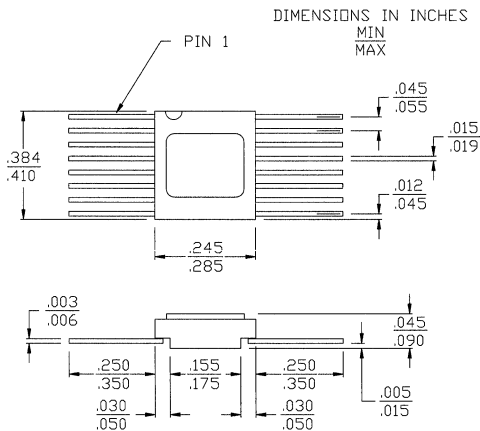
32-Lead (300-Mil) CerDIP D32



24-Lead (400-Mil) Sidebraze DIP D40
MIL-STD-1835 D-11 Config. A



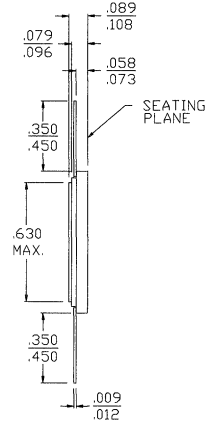
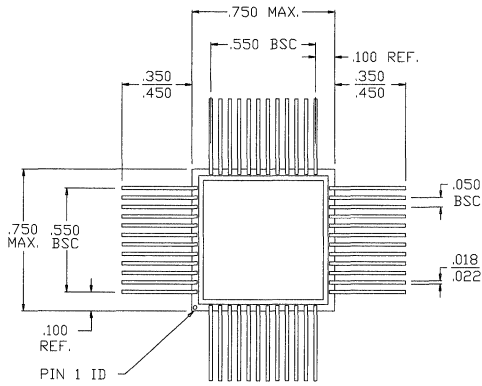
Ceramic Dual-In-Line Packages (continued)
32-Lead (400-Mil) Sidebraze DIP D46
32-Lead (600-Mil) Sidebraze DIP D50

Ceramic Flatpacks
16-Lead Rectangular Flatpack F69
MIL-STD-1835 F-5 Config. B

18-Lead Rectangular Flatpack F70


Ceramic Flatpacks (continued)

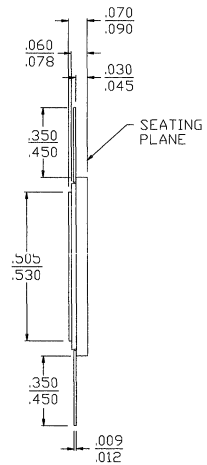
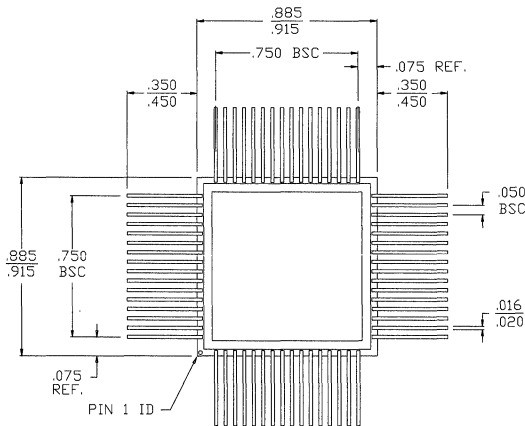
48-Lead Quad Flatpack F78

DIMENSIONS IN INCHES
MIN
MAX



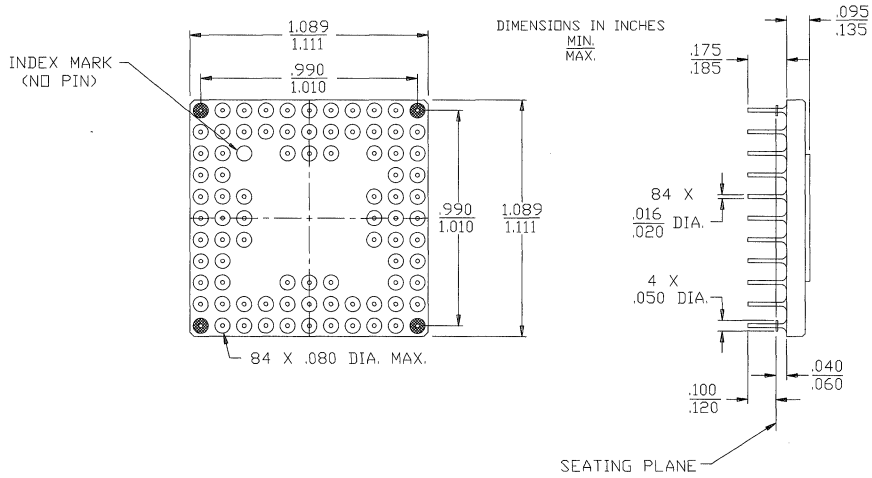
64-Lead Quad Flatpack F90

DIMENSIONS IN INCHES
MIN
MAX

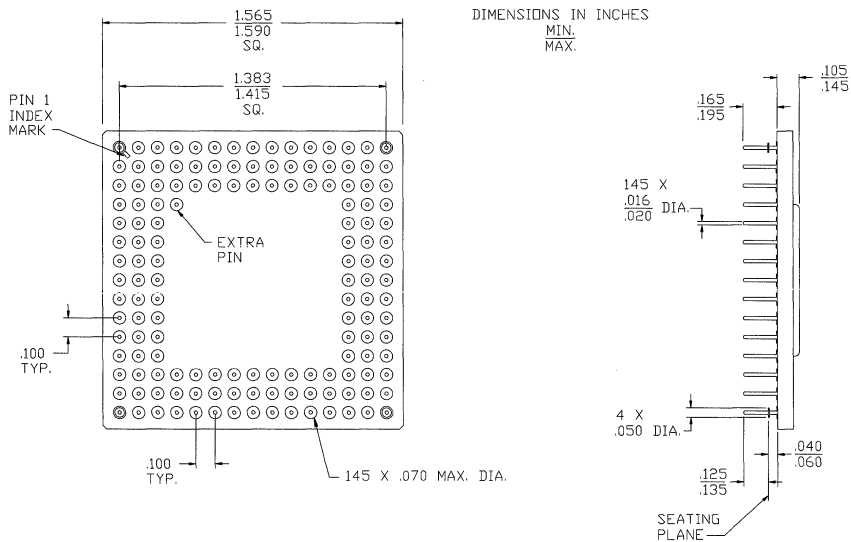


Ceramic Pin Grid Arrays (continued)

84-Pin Grid Array (Cavity Up) G84

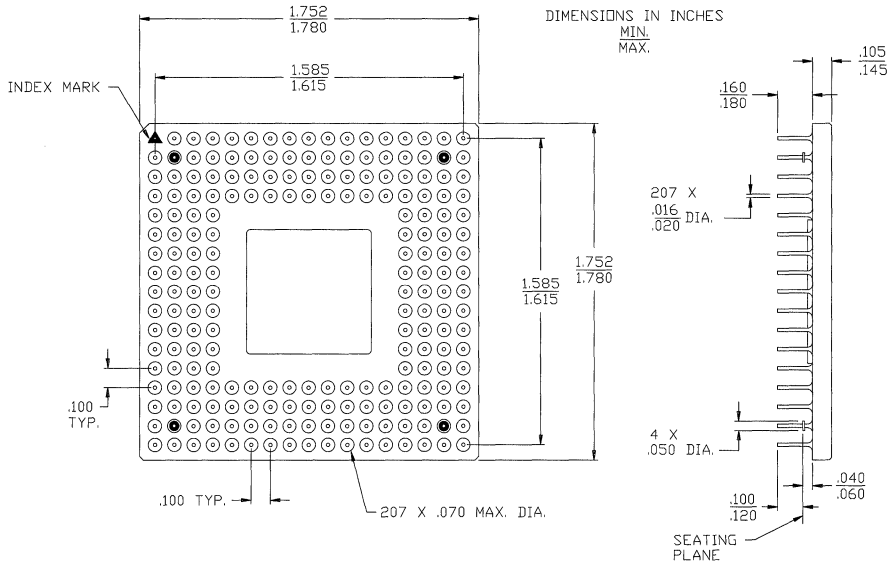


145-Pin Grid Array (Cavity Up) G145



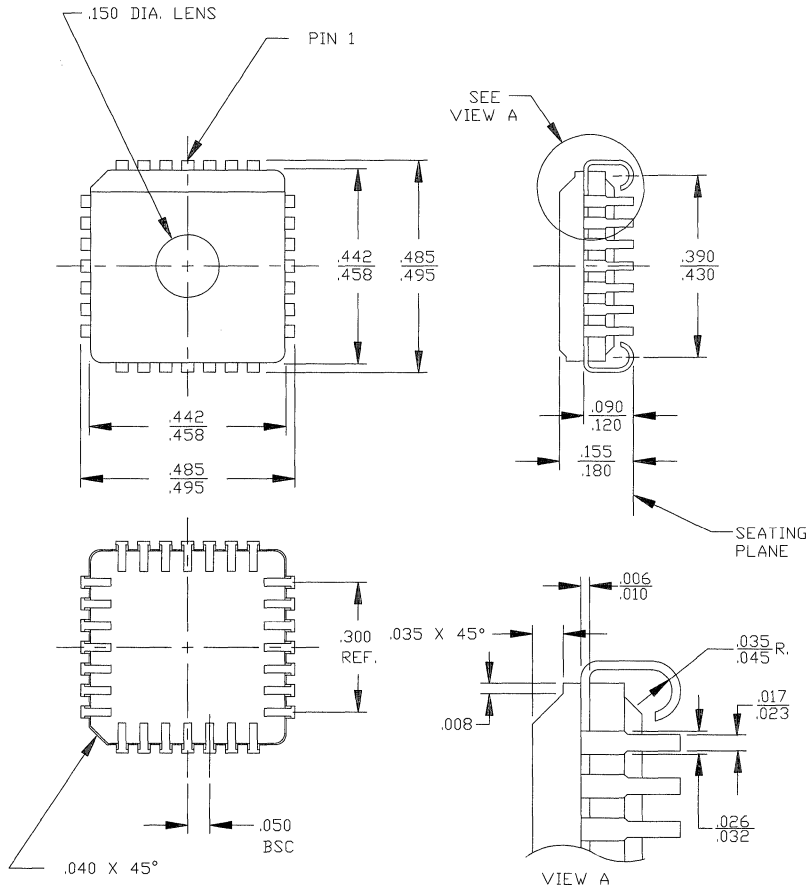
Ceramic Pin Grid Arrays (continued)

207-Pin Grid Array (Cavity Down) G207



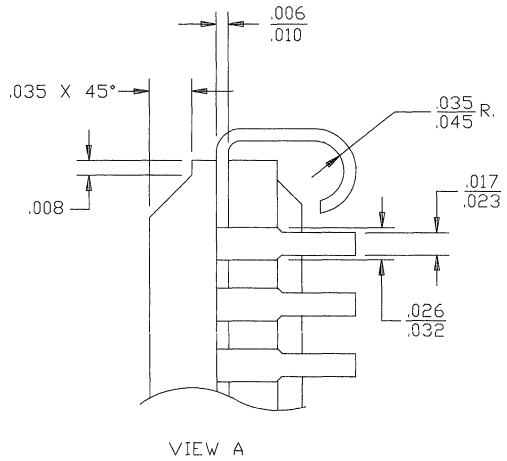
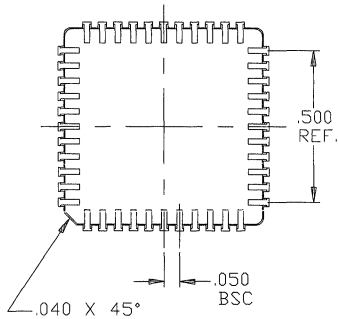
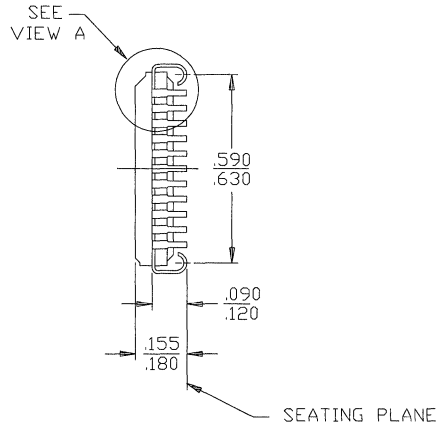
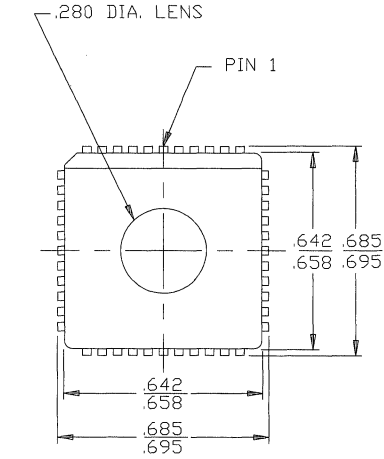
Ceramic Windowed J-Leaded Chip Carriers (continued)

28-Pin Windowed Leaded Chip Carrier H64



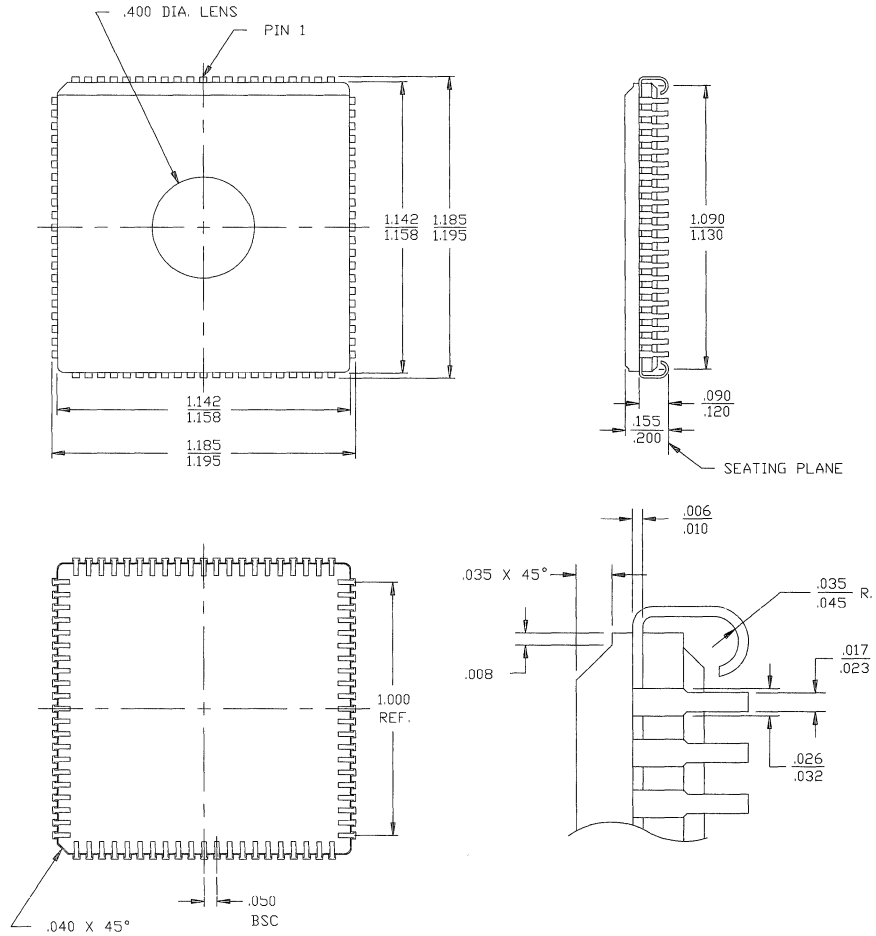
Ceramic Windowed J-Leaded Chip Carriers (continued)

44-Pin Windowed Leaded Chip Carrier H67



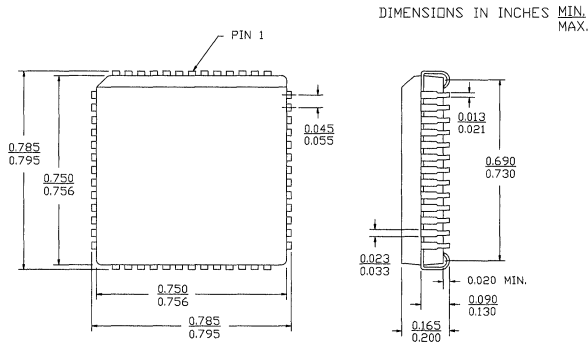
Ceramic Windowed J-Leaded Chip Carriers (continued)

84-Lead Windowed Leaded Chip Carrier H84

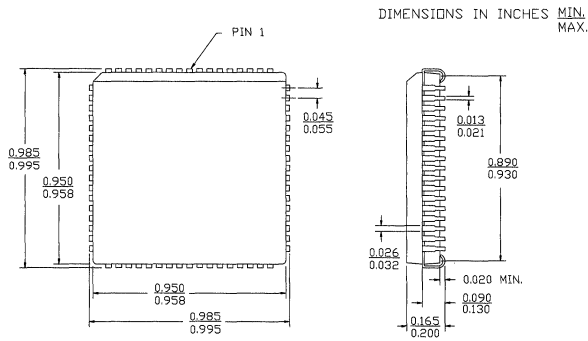


Plastic Leaded Chip Carriers (continued)

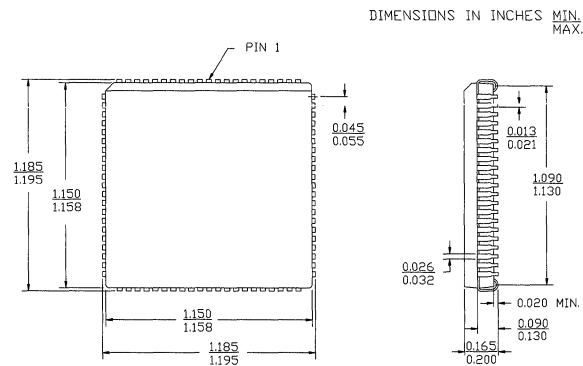
52-Lead Plastic Leaded Chip Carrier J69



68-Lead Plastic Leaded Chip Carrier J81

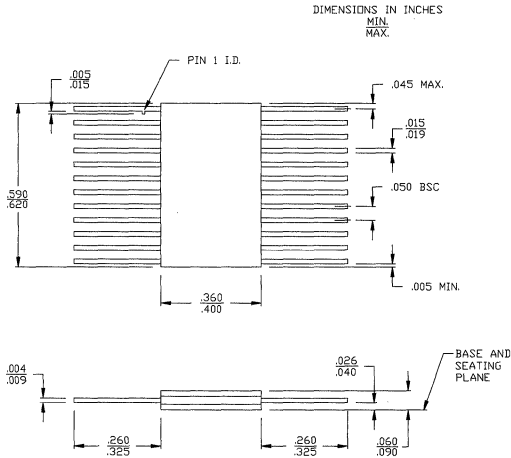


84-Lead Plastic Leaded Chip Carrier J83

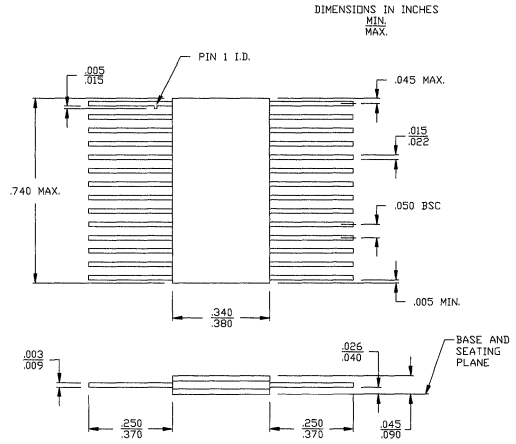


Cerpacks (continued)

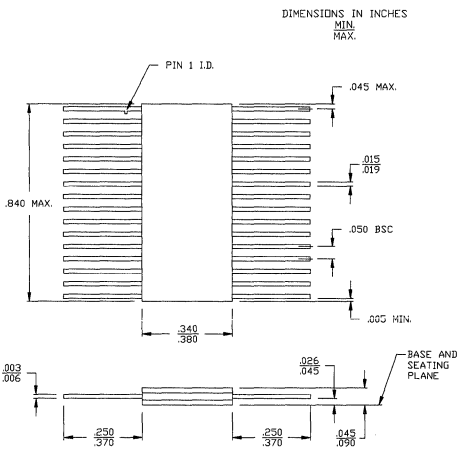
24-Lead Rectangular Cerpack K73
MIL-STD-1835 F-6 Config. A



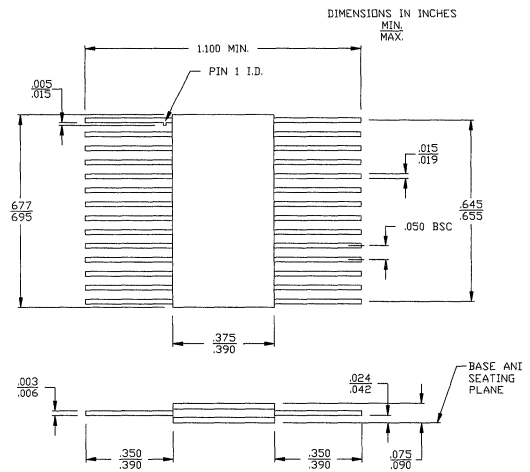
28-Lead Rectangular Cerpack K74
MIL-STD-1835 F-11 Config. A

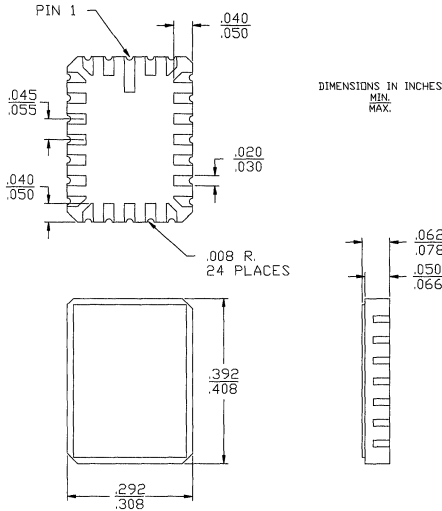
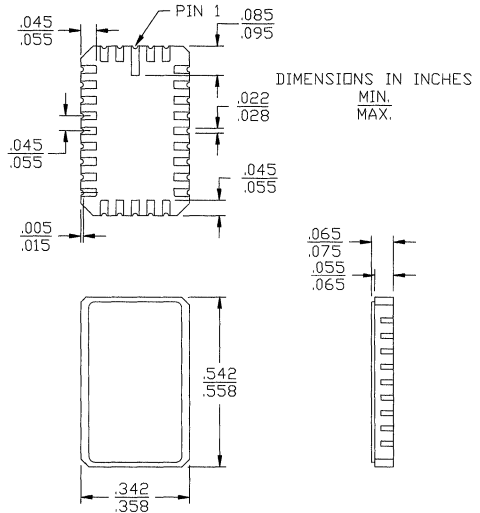
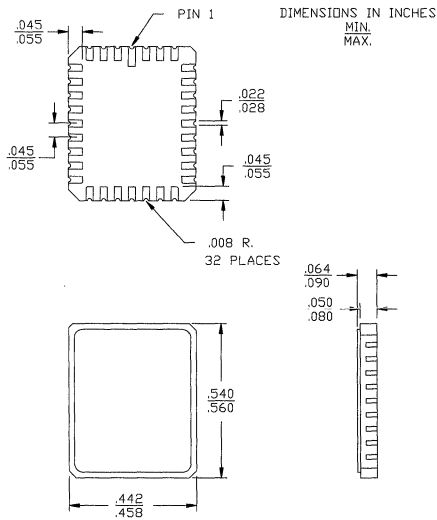
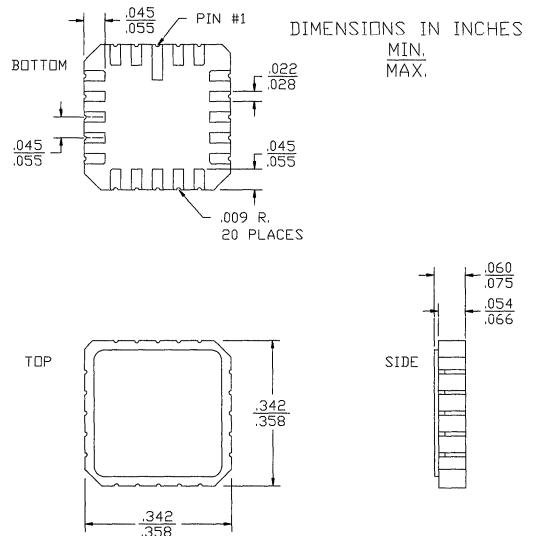


32-Lead Rectangular Cerpack K75



28-Lead Rectangular Cerpack K80

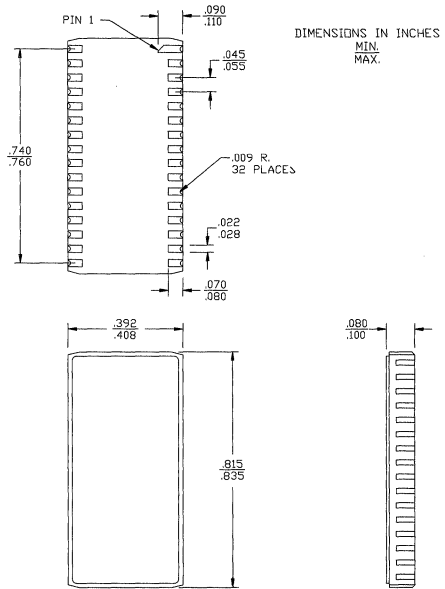
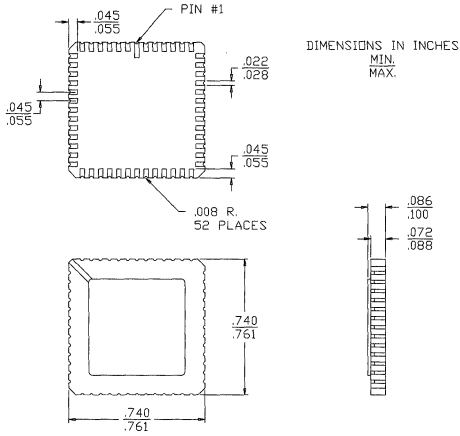


Ceramic Leadless Chip Carriers (continued)
24-Pin Rectangular Leadless Chip Carrier L53

28-Pin Rectangular Leadless Chip Carrier L54
MIL-STD-1835 C-11A

32-Pin Rectangular Leadless Chip Carrier L55
MIL-STD-1835 C-12

20-Pin Square Leadless Chip Carrier L61
MIL-STD-1835 C-2A


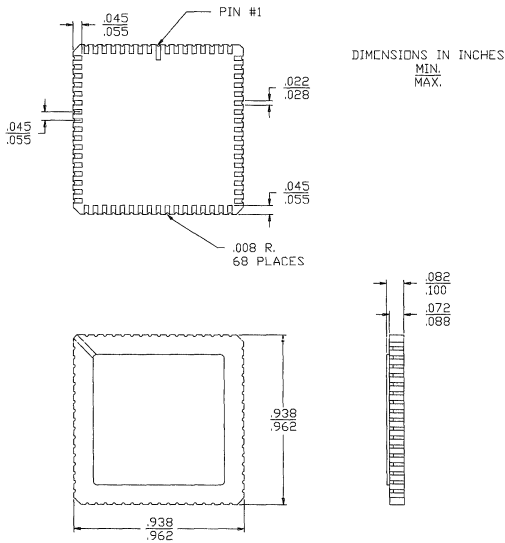
Ceramic Leadless Chip Carriers (continued)

52-Square Leadless Chip Carrier L69

32-Pin Leadless Chip Carrier L75

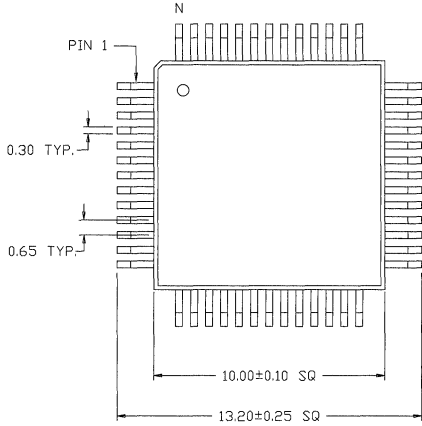


68-Square Leadless Chip Carrier L81
MIL-STD-1835 C-7

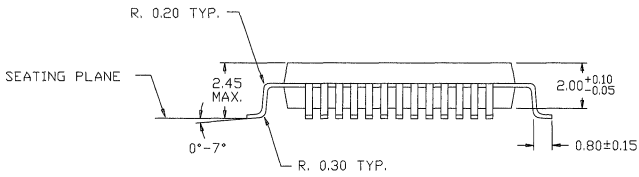


Plastic Quad Flatpacks (continued)

52-Lead Plastic Quad Flatpack N52

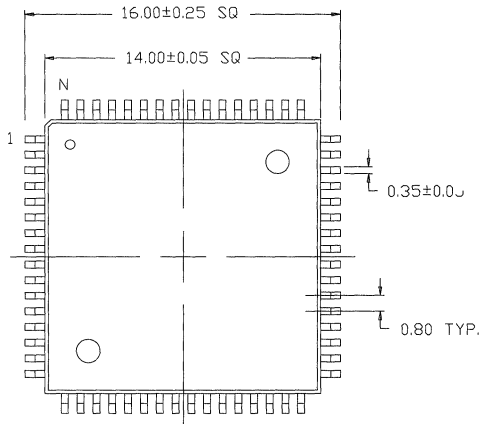


DIMENSIONS ARE IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.

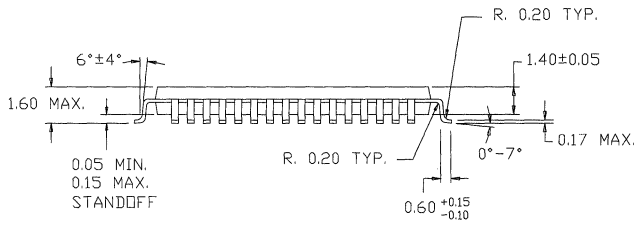


Plastic Quad Flatpacks (continued)

64-Lead Plastic Thin Quad Flatpack N65

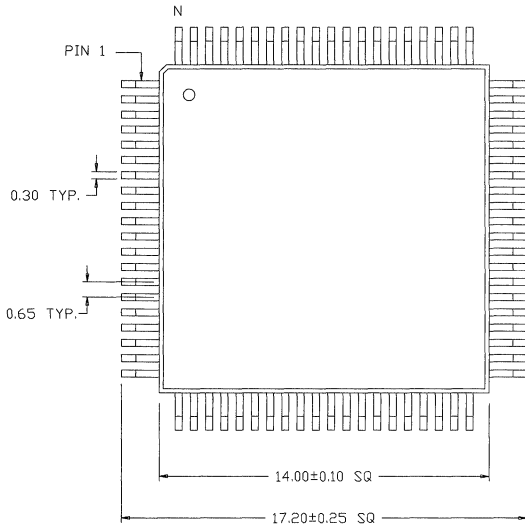


DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.100 MAX.

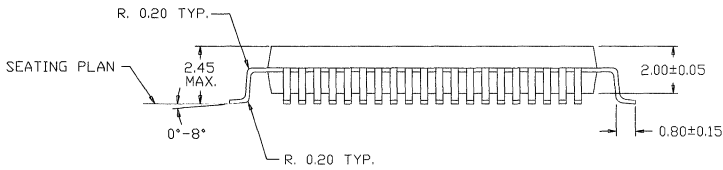


Plastic Quad Flatpacks (continued)

80-Lead Plastic Quad Flatpack N80

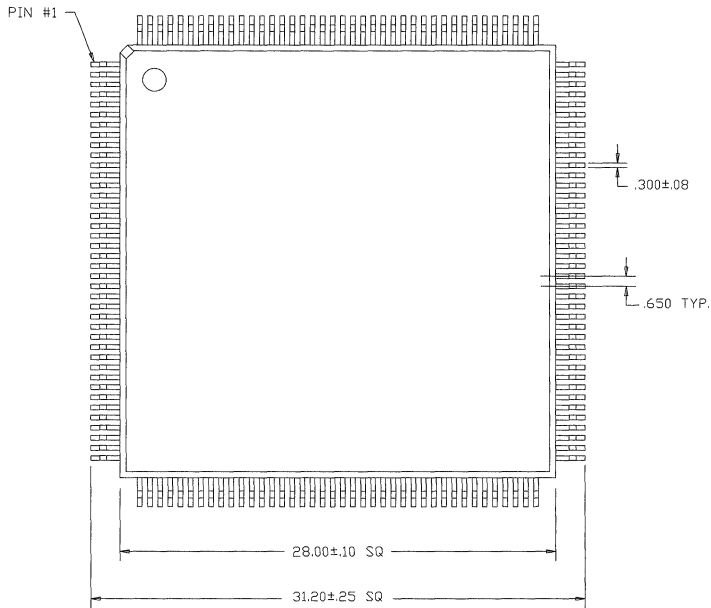


DIMENSIONS ARE IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.

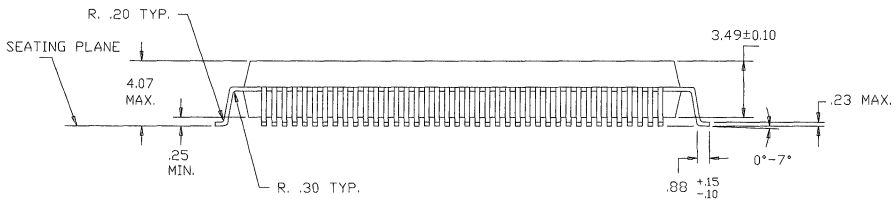


Plastic Quad Flatpacks (continued)

160-Lead Plastic Quad Flatpack N160

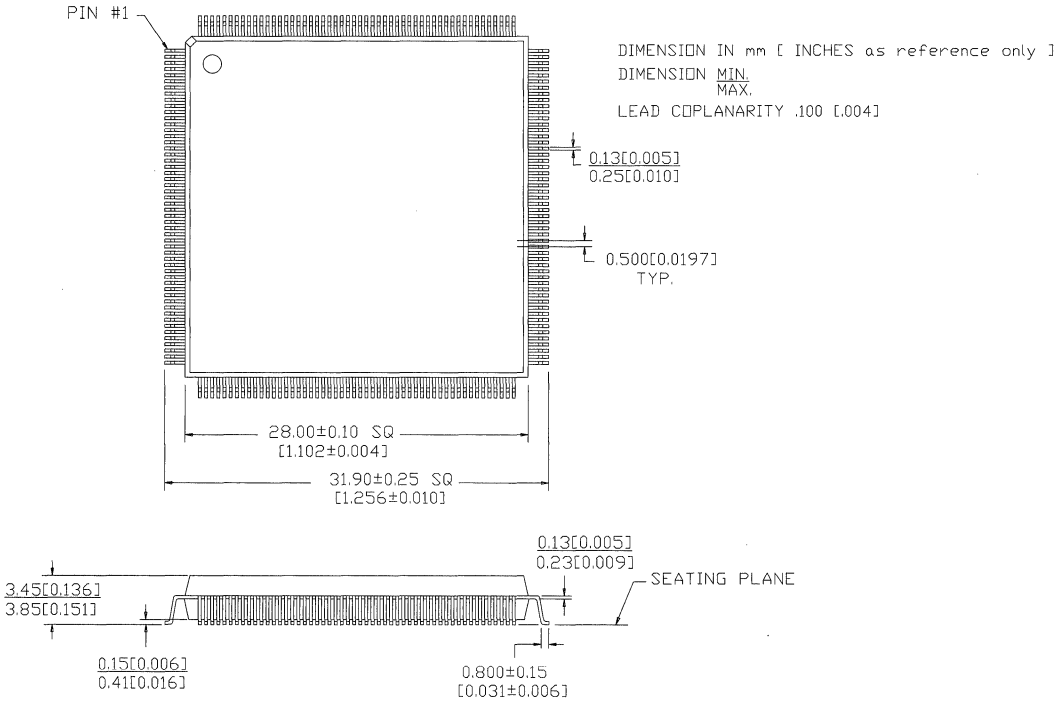


DIMENSION IN mm
LEAD COPLANARITY .100



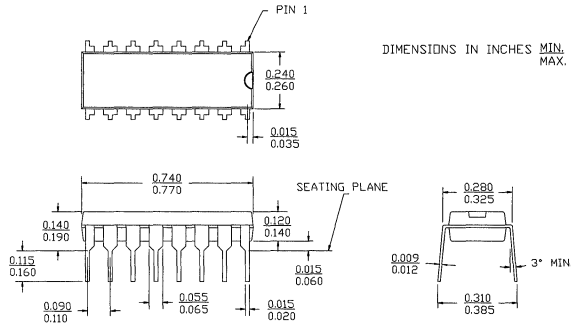
Plastic Quad Flatpacks (continued)

208-Lead Plastic Quad Flatpack N208

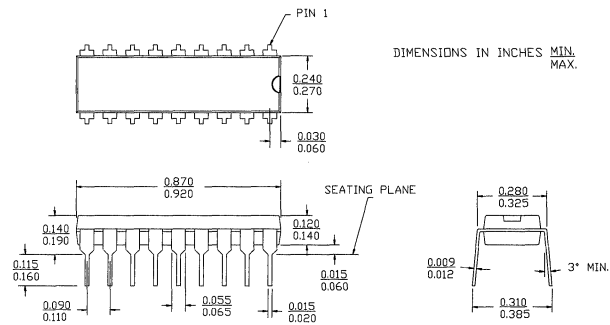


Plastic Dual-In-Line Packages

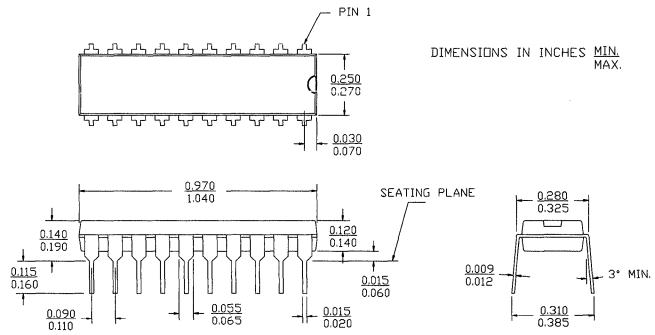
16-Lead (300-Mil) Molded DIP P1

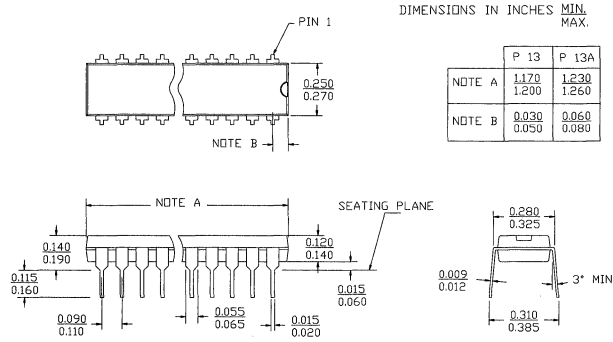
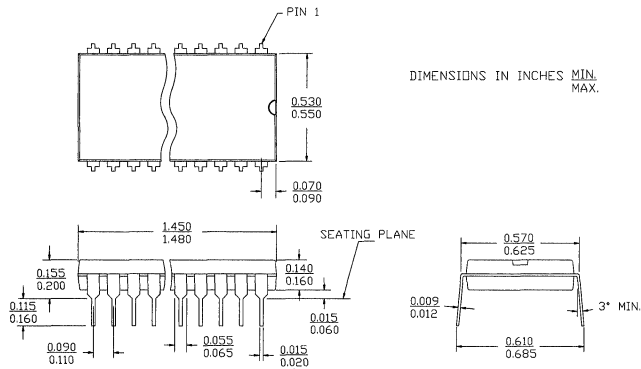
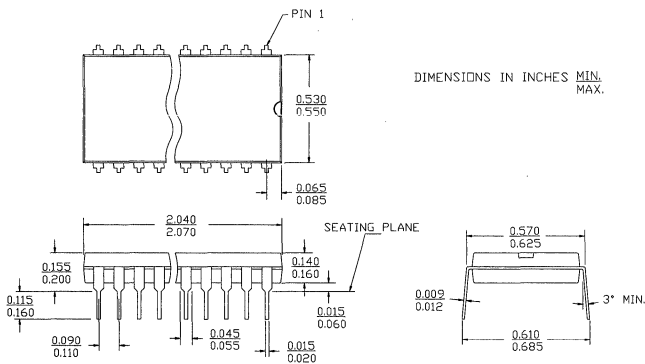


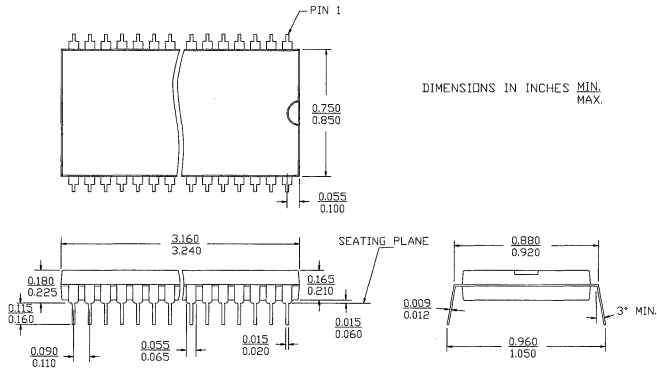
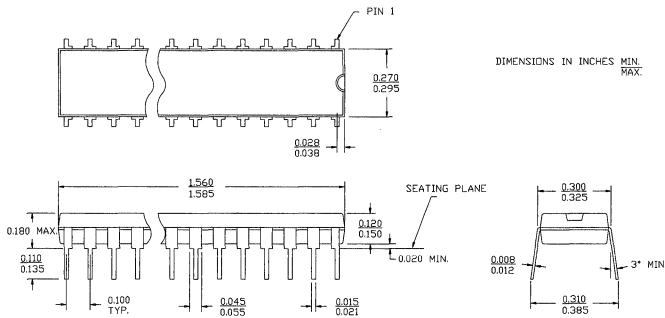
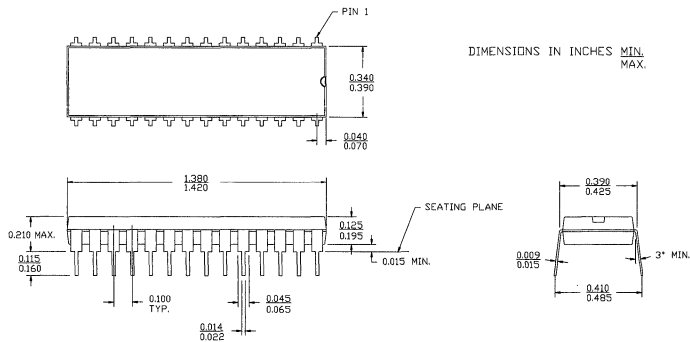
18-Lead (300-Mil) Molded DIP P3



20-Lead (300-Mil) Molded DIP P5

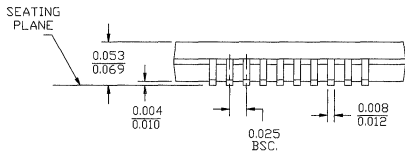
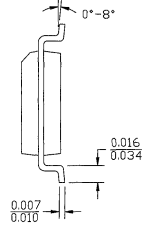
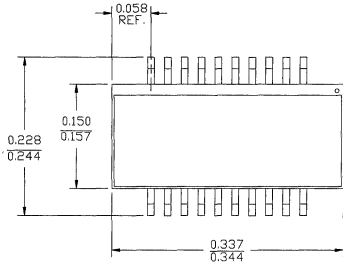


Plastic Dual-In-Line Packages (continued)
24-Lead (300-Mil) Molded DIP P13/P13A

28-Lead (600-Mil) Molded DIP P15

40-Lead (600-Mil) Molded DIP P17


Plastic Dual-In-Line Packages (continued)
64-Lead (900-Mil) Molded DIP P29

32-Lead (300-Mil) Molded DIP P31

28-Lead (400-Mil) Molded DIP P41


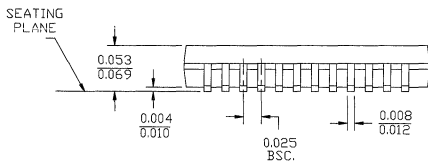
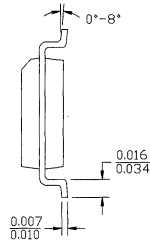
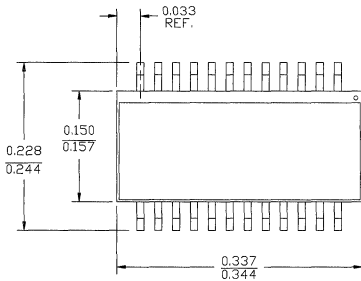
Quarter Size Outline Packages

20-Lead Quarter Size Outline Q5



DIMENSIONS IN INCHES MIN. MAX.
LEAD COPLANARITY 0.004 MAX.

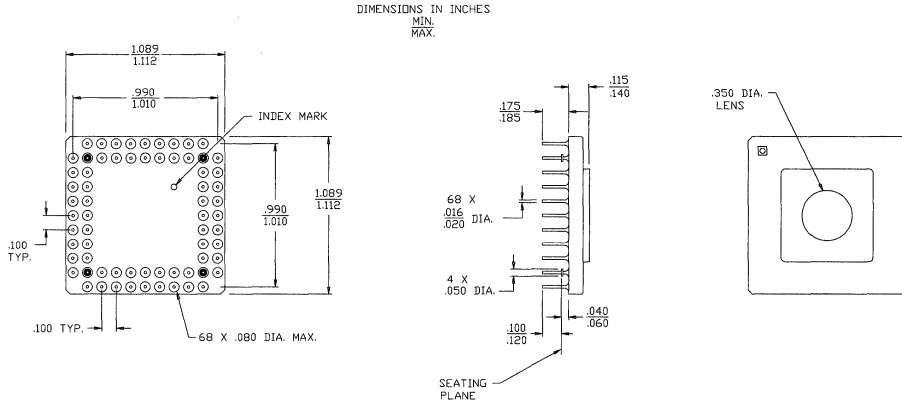
24-Lead Quarter Size Outline Q13



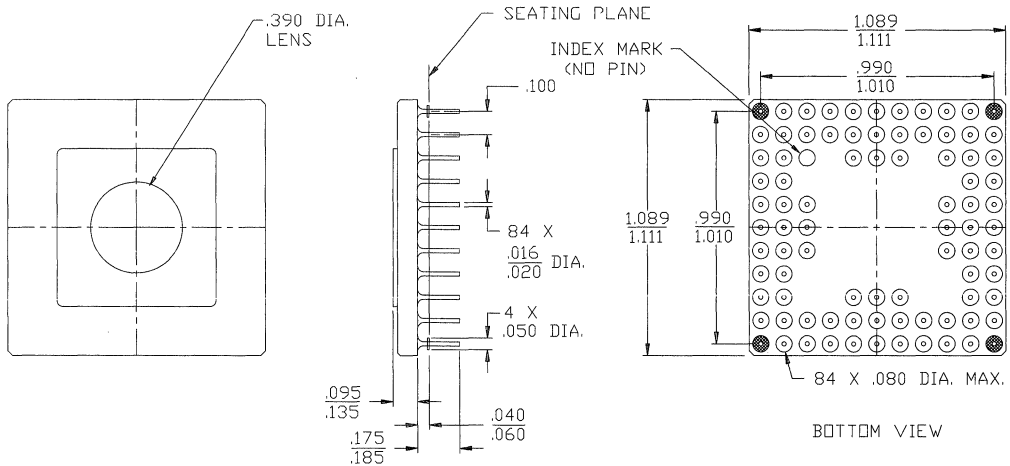
DIMENSIONS IN INCHES MIN. MAX.
LEAD COPLANARITY 0.004 MAX.

Ceramic Windowed Pin Grid Arrays

68-Pin Windowed PGA Ceramic R68

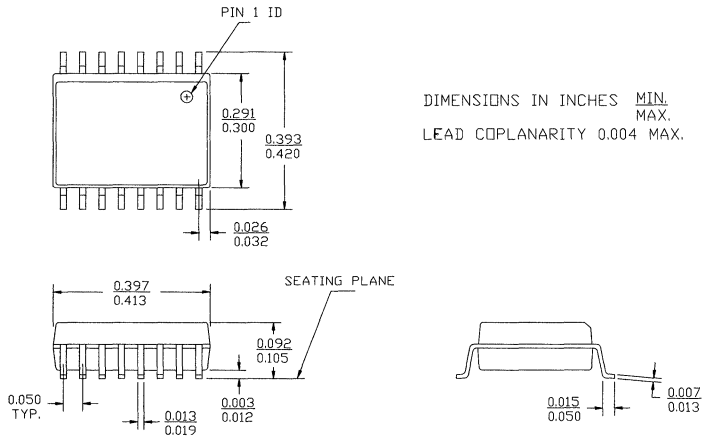


84-Lead Windowed Pin Grid Array R84

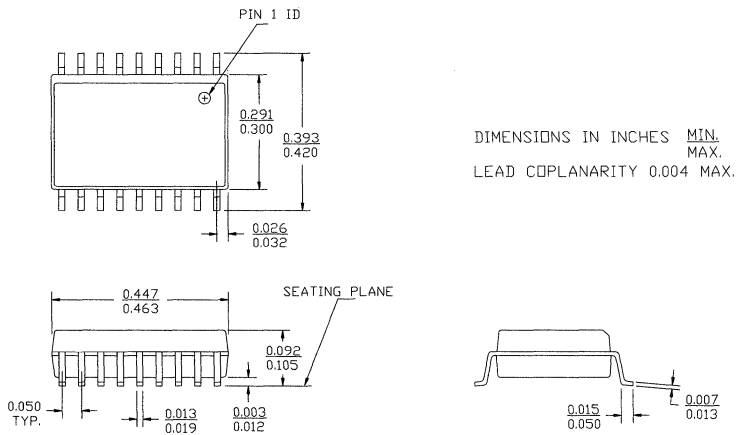


Plastic Small Outline ICs

16-Lead Molded SOIC S1

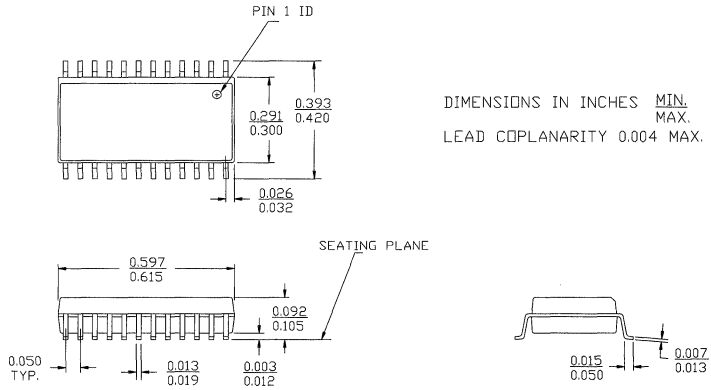


18-Lead (300-Mil) Molded SOIC S3

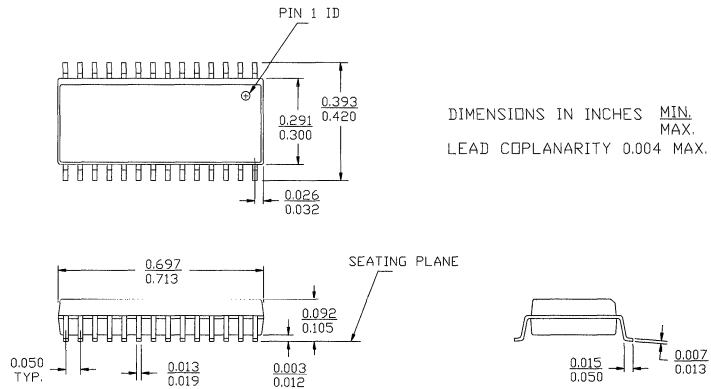


Plastic Small Outline ICs (continued)

24-Lead (300-Mil) Molded SOIC S13



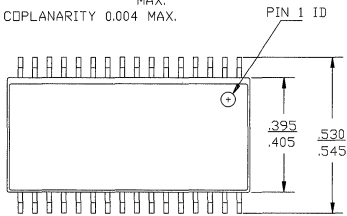
28-Lead (300-Mil) Molded SOIC S21



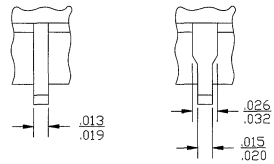
Plastic Small Outline ICs (continued)

32-Lead (400-Mil) Molded SOIC S33

DIMENSIONS IN INCHES MIN.
MAX.
LEAD COPLANARITY 0.004 MAX.

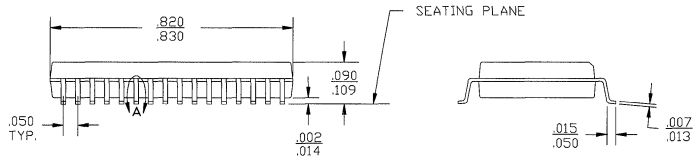


DETAIL A
EXTERNAL LEAD DESIGN



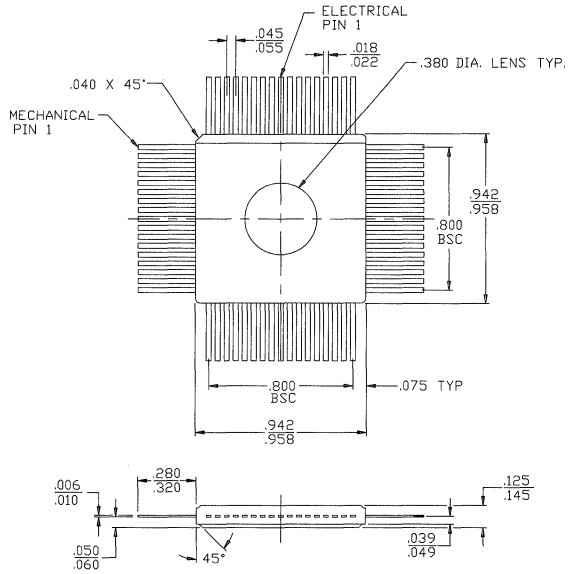
OPTION 1

OPTION 2



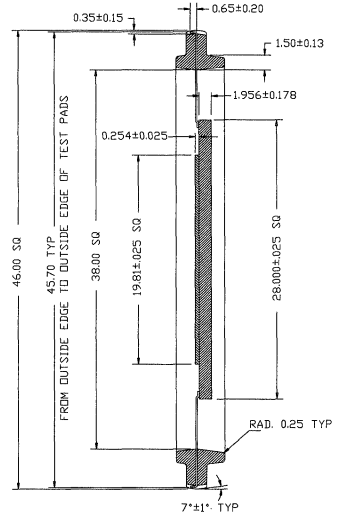
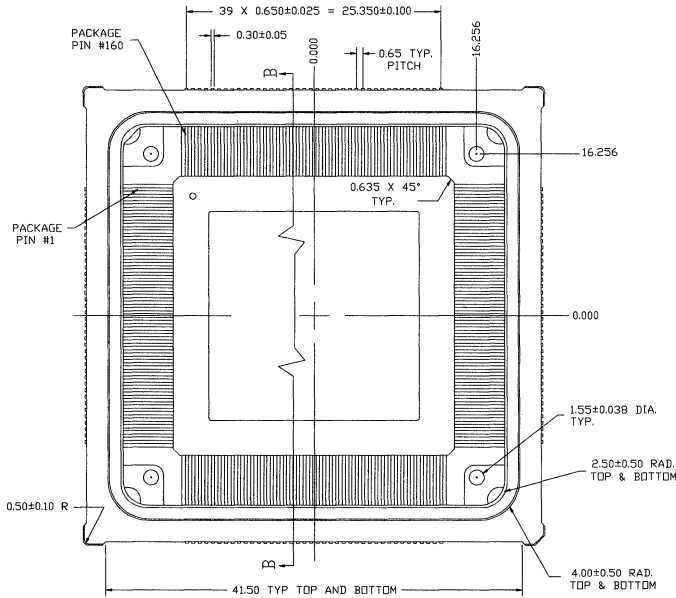
Windowed Cerpacks (continued)

68-Lead Windowed Cerquad Flatpack T91

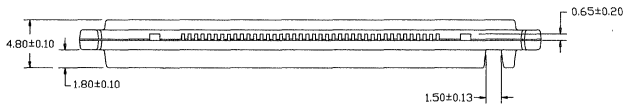


Ceramic Quad Flatpacks (continued)

160-Lead Ceramic Quad Flatpack In Ring U160

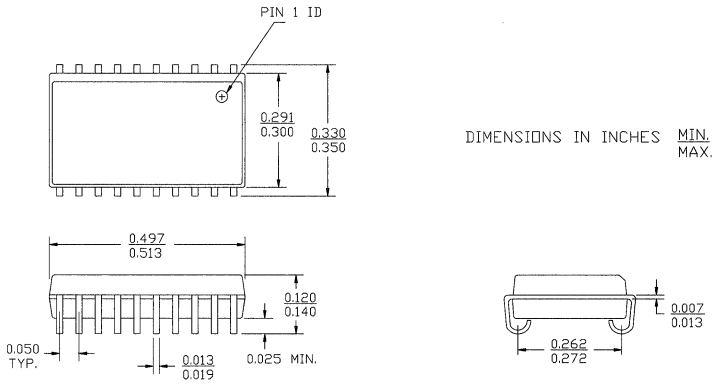


SECTION B-B

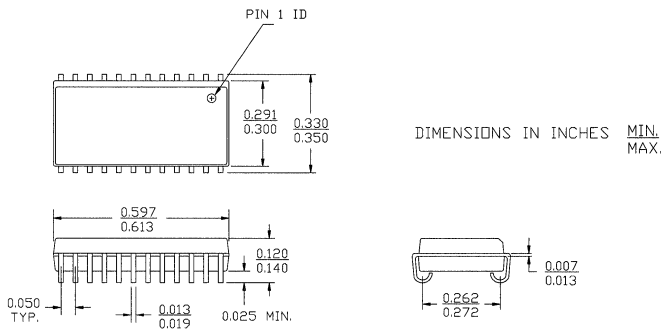


Plastic Small Outline J-Bend

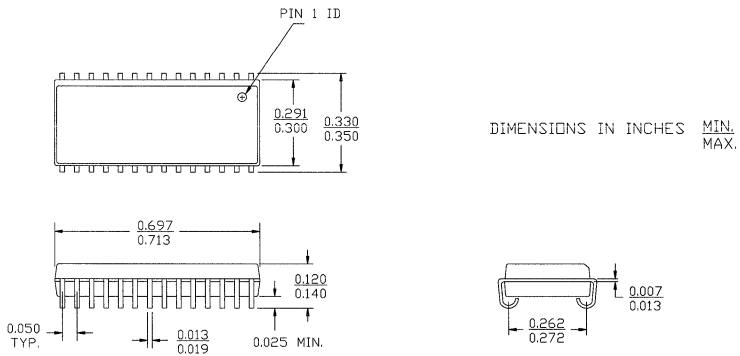
20-Lead (300-Mil) Molded SOJ V5



24-Lead (300-Mil) Molded SOJ V13



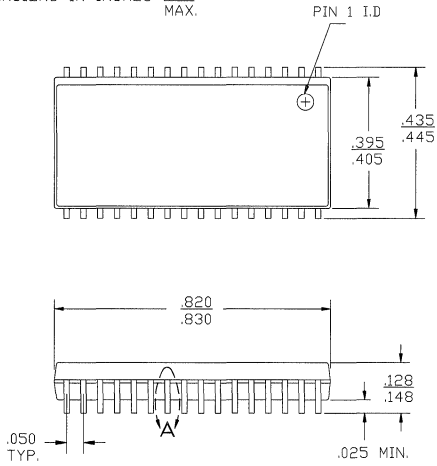
28-Lead (300-Mil) Molded SOJ V21



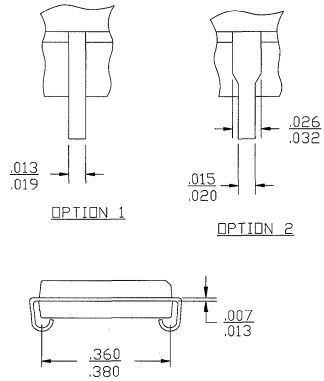
Plastic Small Outline J-Bend (continued)

32-Lead (400-Mil) Molded SOJ V33

DIMENSIONS IN INCHES MIN. MAX.

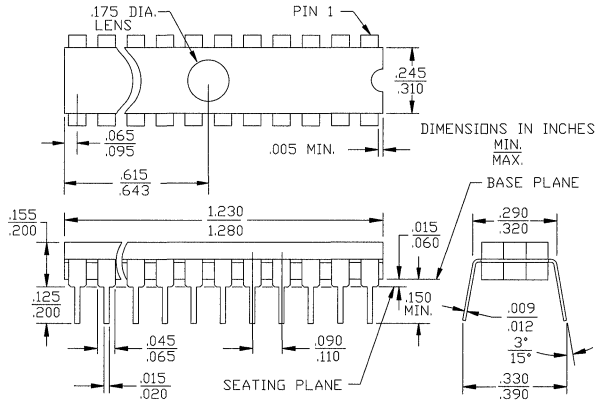


DETAIL A
EXTERNAL LEAD DESIGN

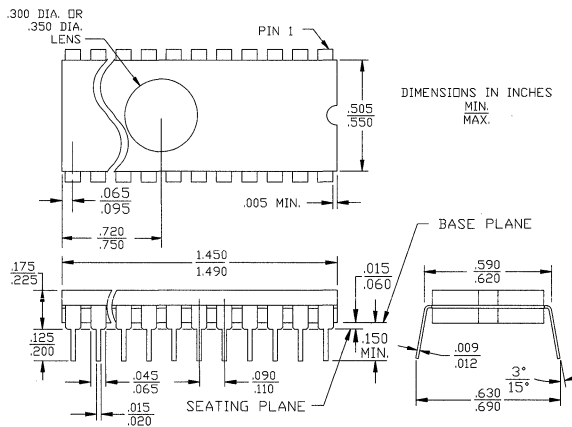


Ceramic Windowed Dual-In-Line Packages (continued)

24-Lead (300-Mil) Windowed CerDIP W14
MIL-STD-1835 D-9 Config. A

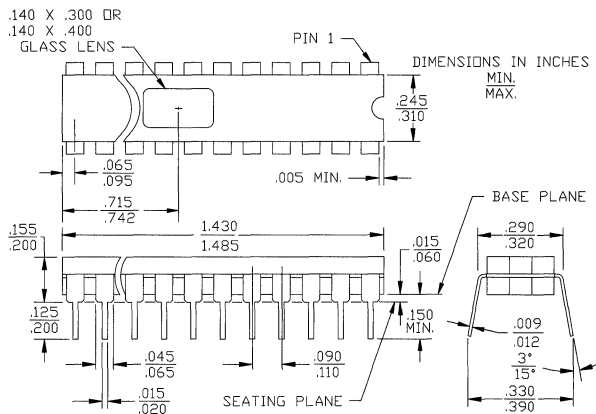


28-Lead (600-Mil) Windowed CerDIP W16
MIL-STD-1835 D-10 Config. A

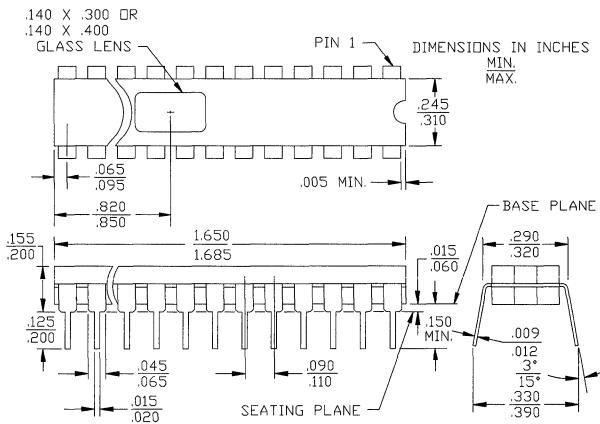


Ceramic Windowed Dual-In-Line Packages (continued)

28-Lead (300-Mil) Windowed CerDIP W22
MIL-STD-1835 D-15 Config. A

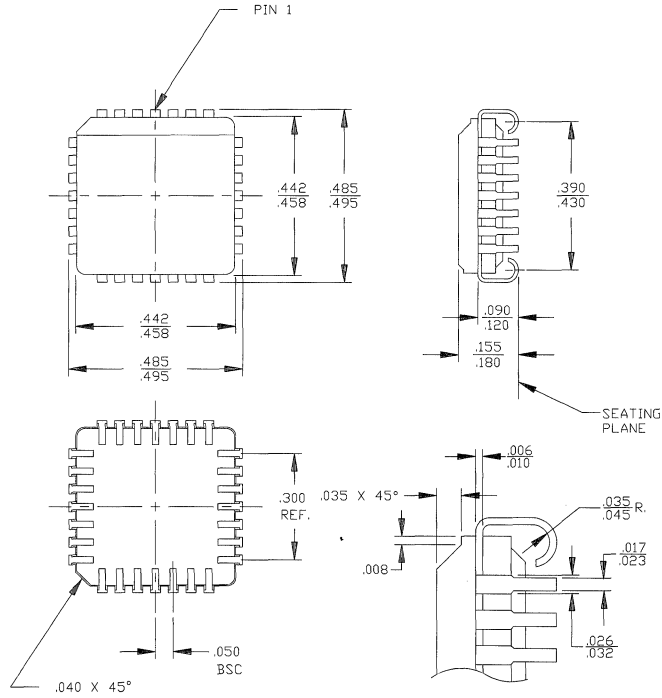


32-Lead (300-Mil) Windowed CerDIP W32



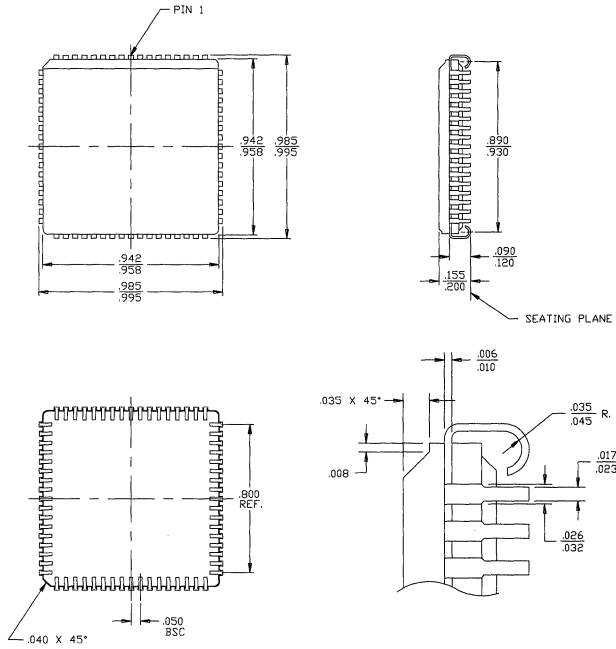
Ceramic J-Leaded Chip Carriers (continued)

28-Pin Ceramic Leaded Chip Carrier Y64



Ceramic J-Leaded Chip Carriers (continued)

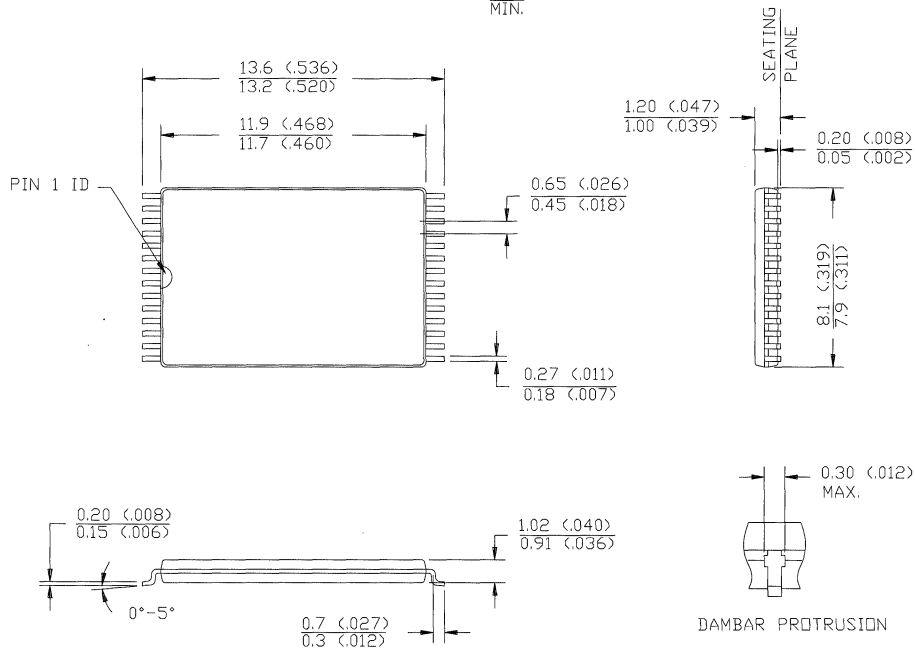
68-Pin Ceramic Leaded Chip Carrier Y68



Thin Small Outline Packages

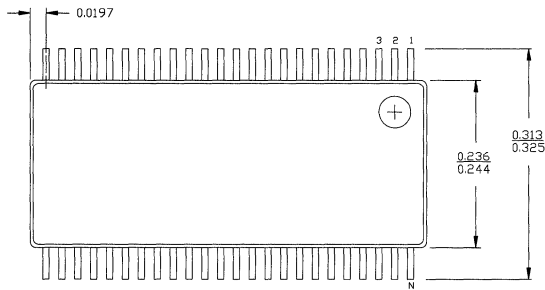
28-Lead Thin Small Outline Package Z28

DIMENSION IN MM (INCH)
MAX.
MIN.

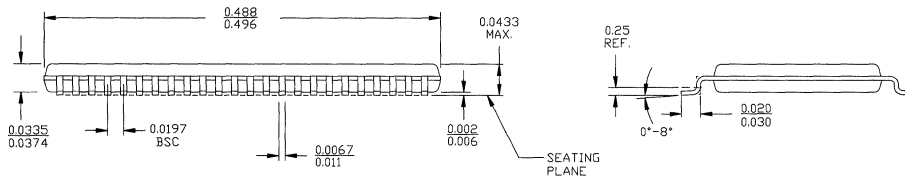


Thin Small Outline Packages (continued)

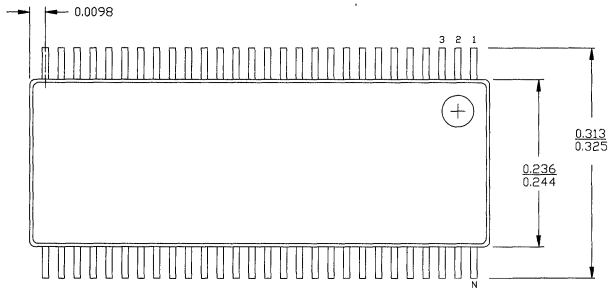
48-Lead Thin Shrunken Small Outline Package Z48



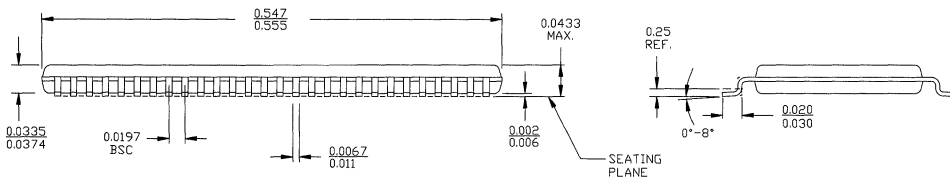
DIMENSIONS IN INCHES MIN.
MAX.



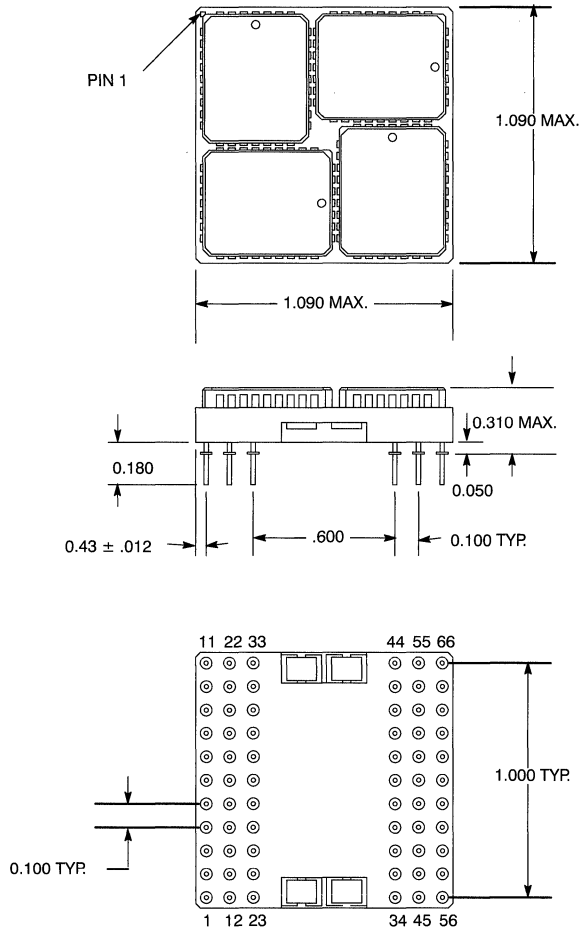
56-Lead Thin Shrunken Small Outline Package Z56



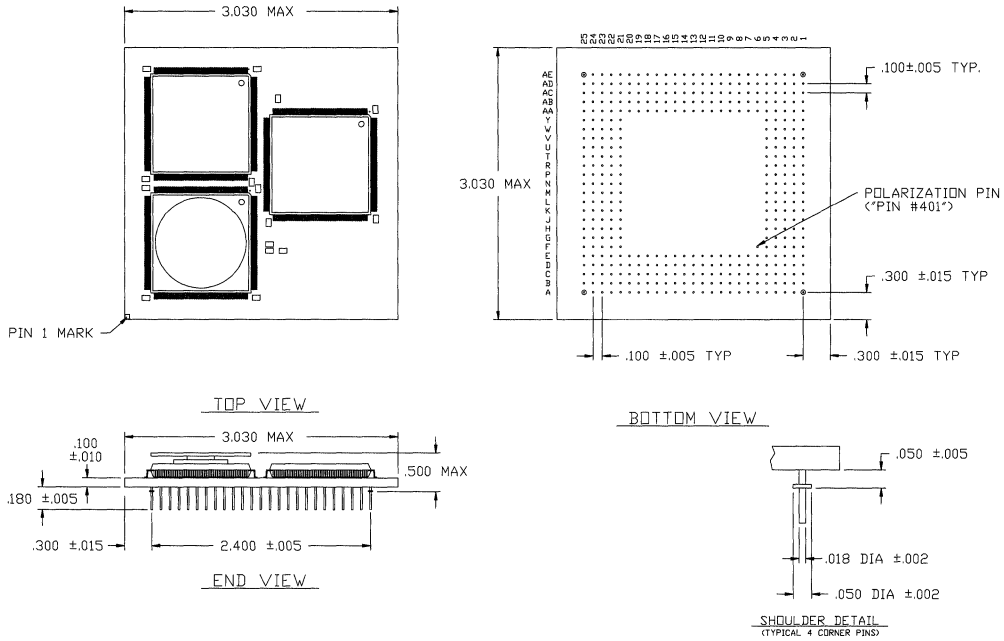
DIMENSIONS IN INCHES MIN.
MAX.



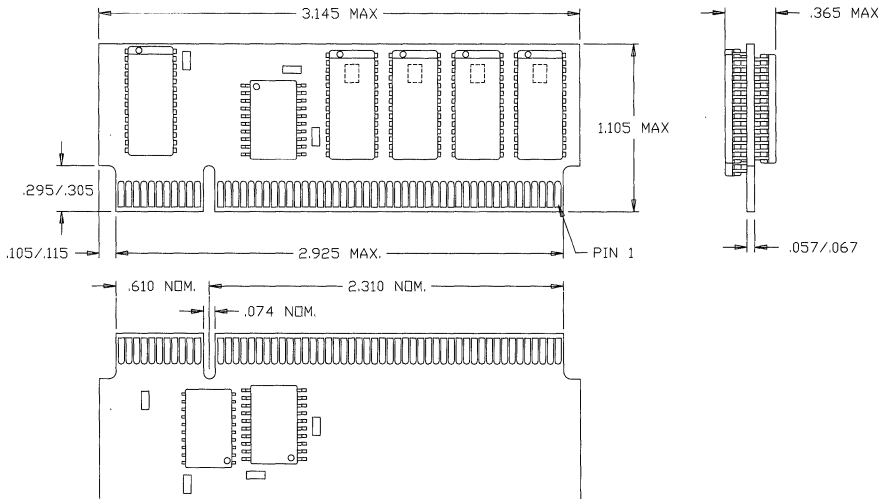
66-Pin PGA Module HG01



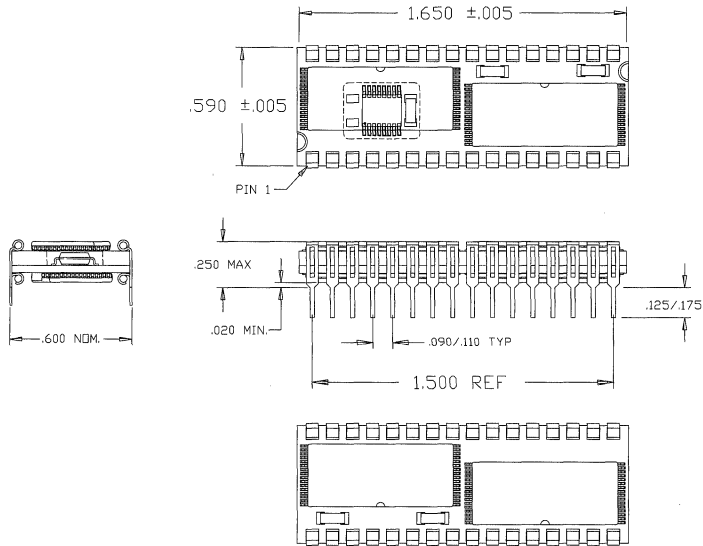
401-Pin PGA Module HG03



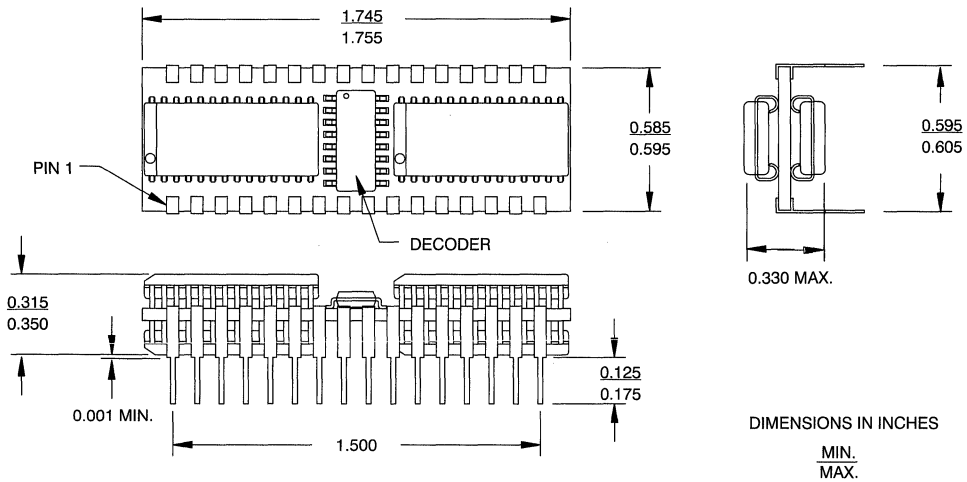
112-Pin Dual-Readout SIMM PB17



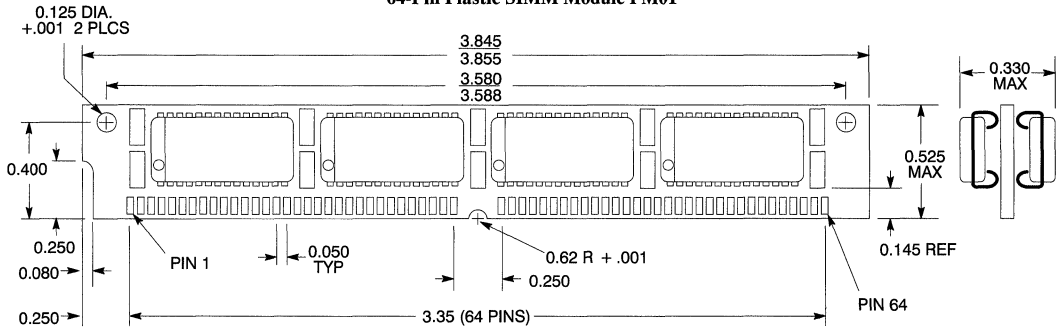
32-Pin DIP Module PD03



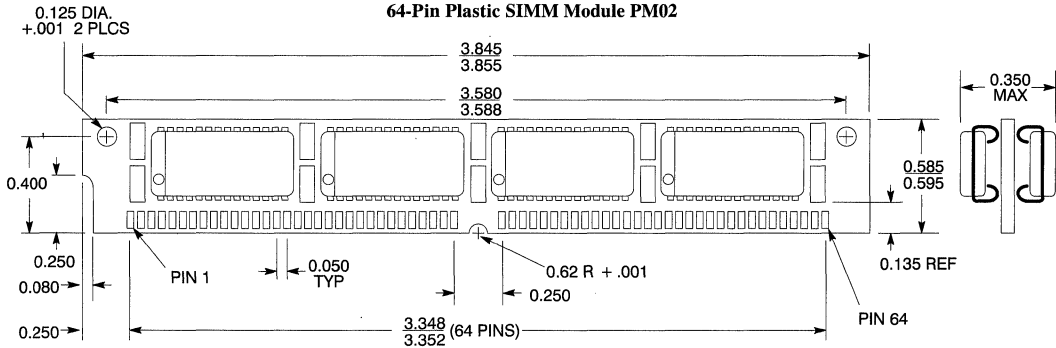
32-Pin DIP Module PD05



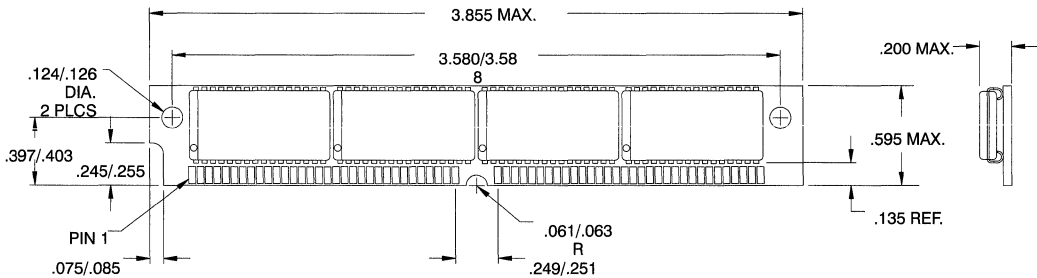
64-Pin Plastic SIMM Module PM01



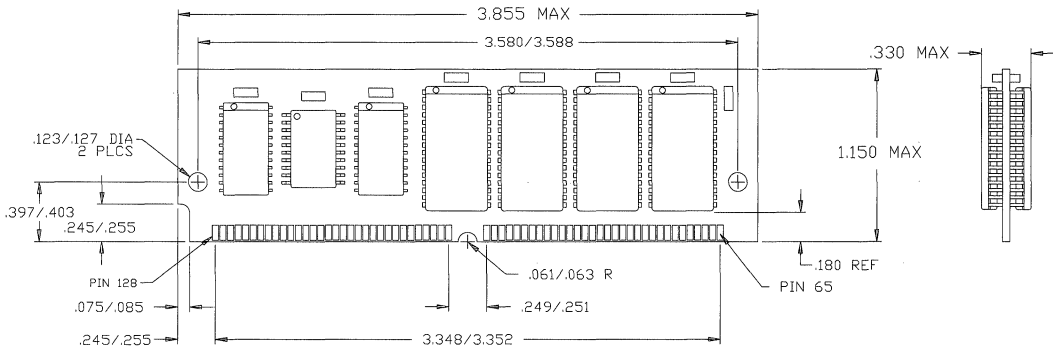
64-Pin Plastic SIMM Module PM02



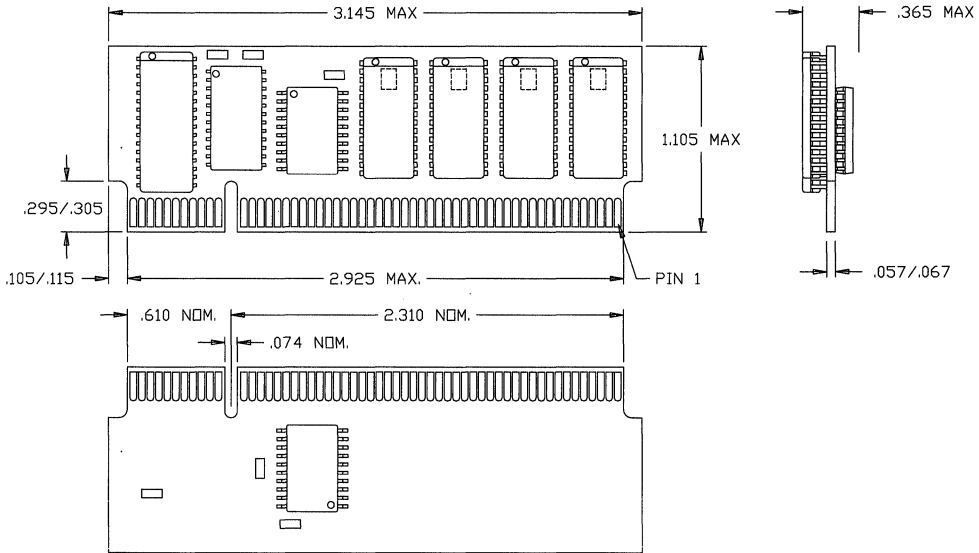
64-Pin SIMM Module PM03



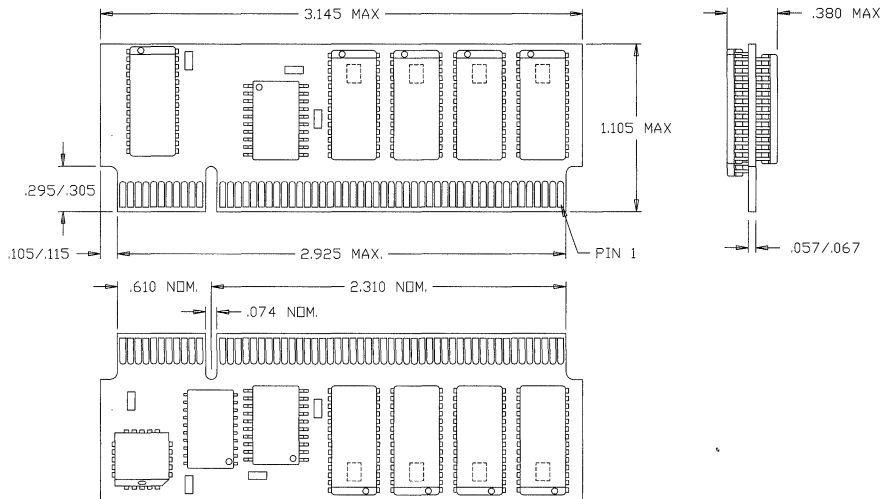
128-Pin Dual-Readout SIMM Module PM07



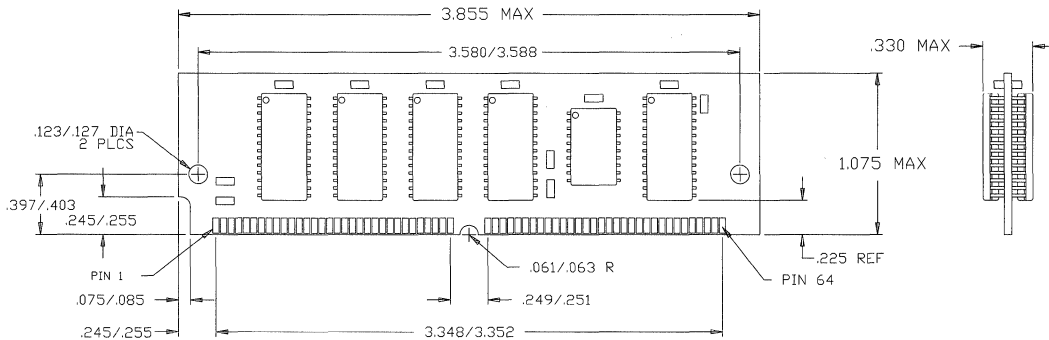
112-Pin Dual-Readout SIMM PM09



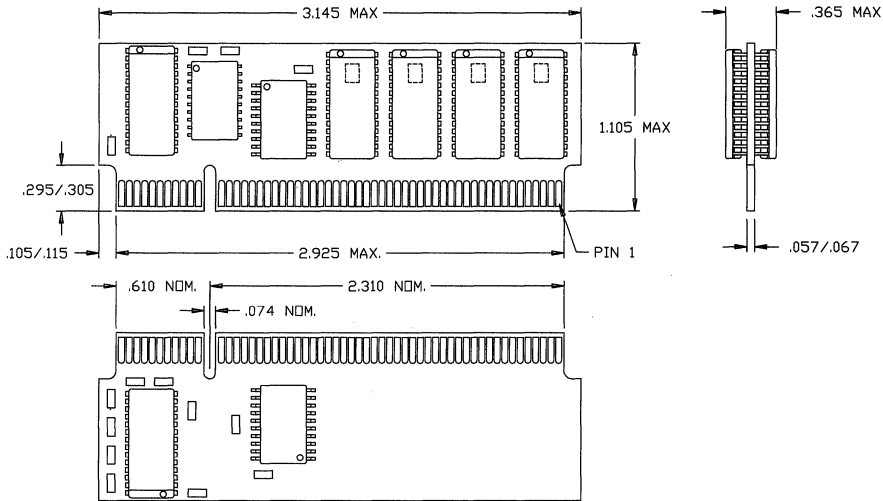
112-Pin Dual-Readout SIMM PM12



128-Pin Dual-Readout SIMM PM13

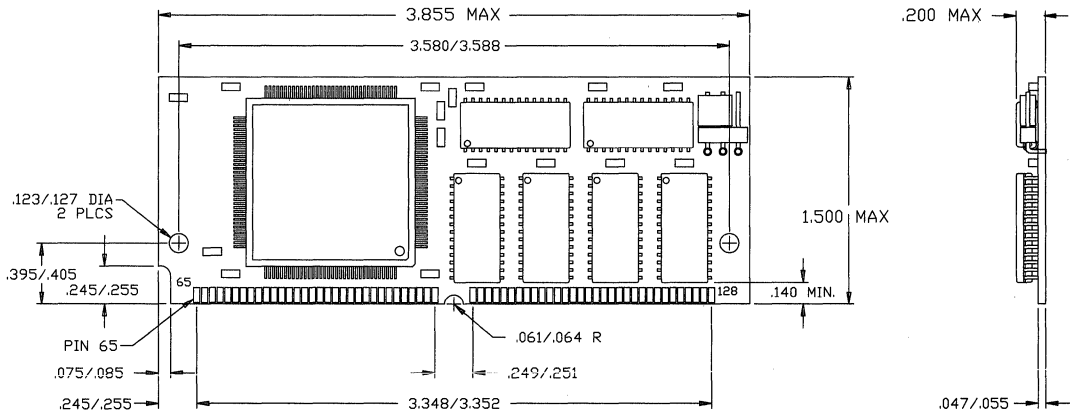


112-Pin Dual-Readout SIMM PM16

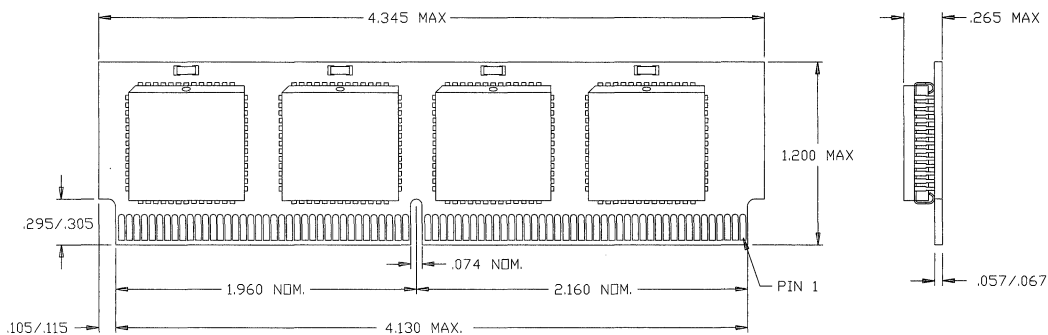


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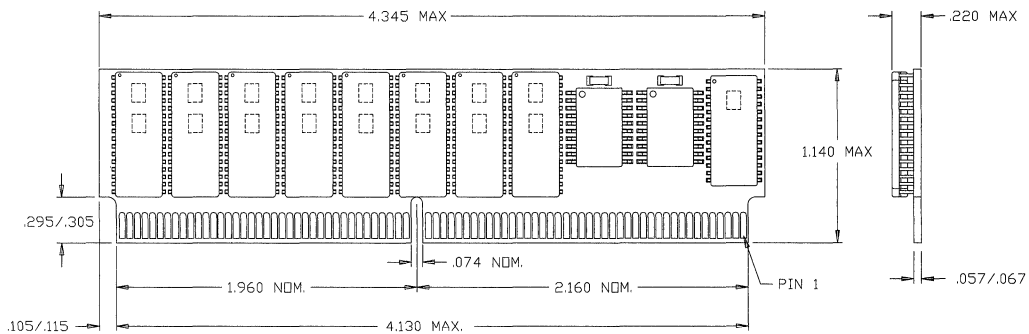
128-pin Dual-Readout SIMM PM19

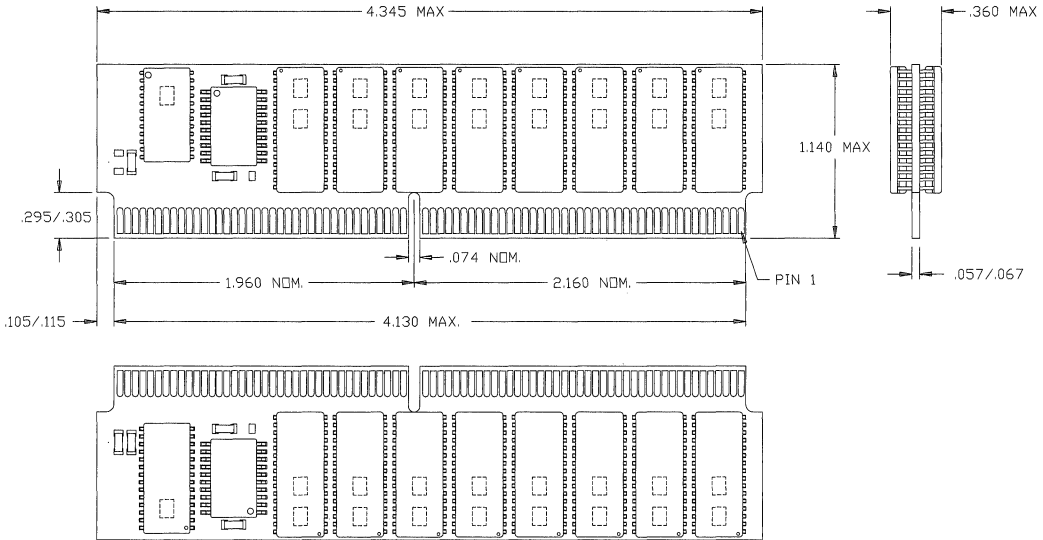
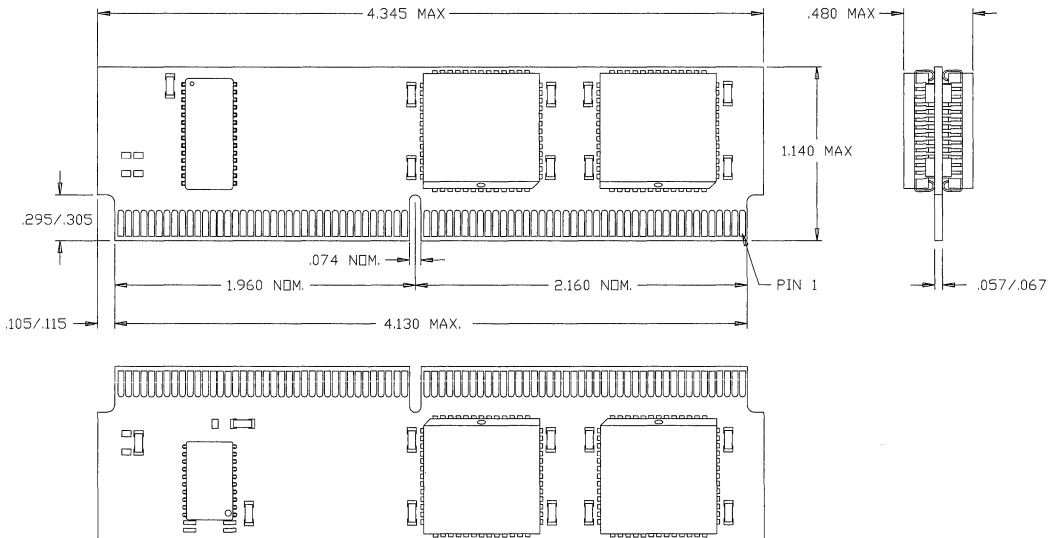


160-Pin Dual-Readout SIMM PM26

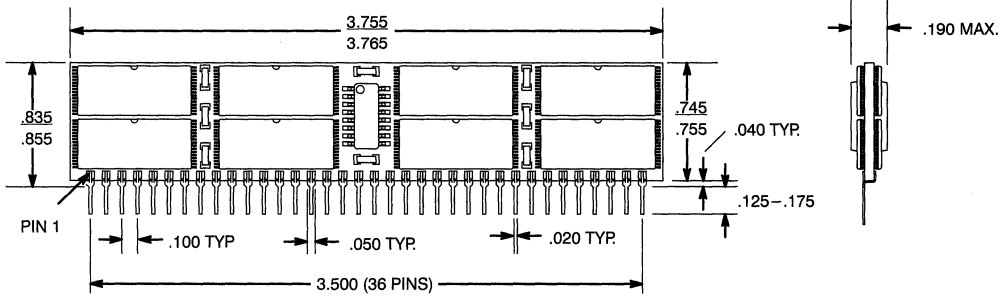


160-Pin Dual-Readout SIMM PM27

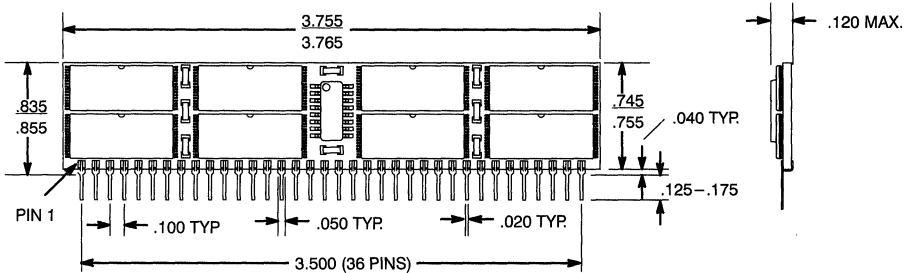


160-Pin Dual-Readout SIMM PM32

160-Pin Dual-Readout SIMM PM33


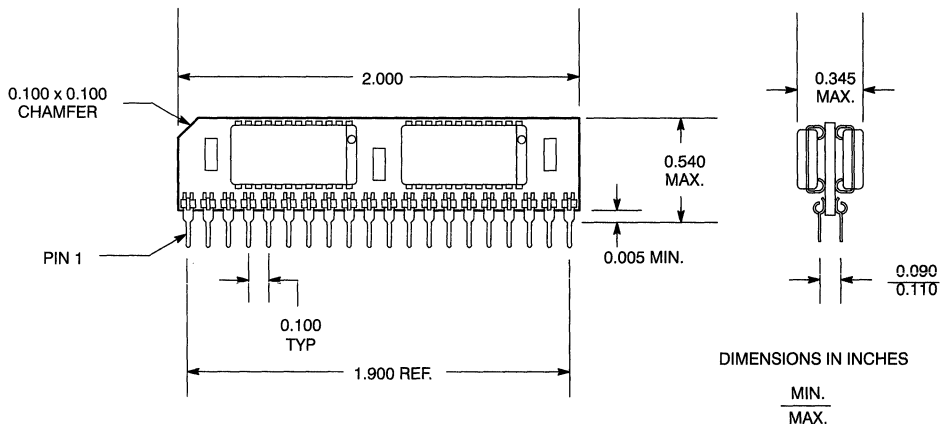
36-Pin SIP Module PS06



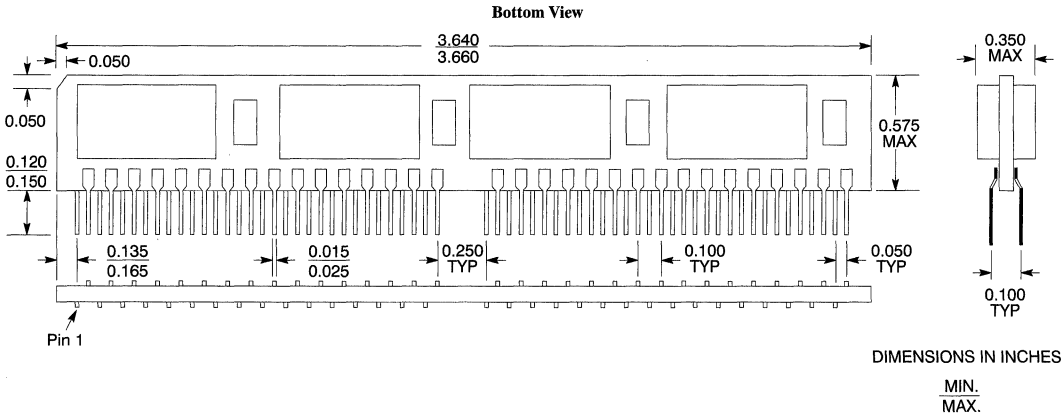
36-Pin SIP Module PS08



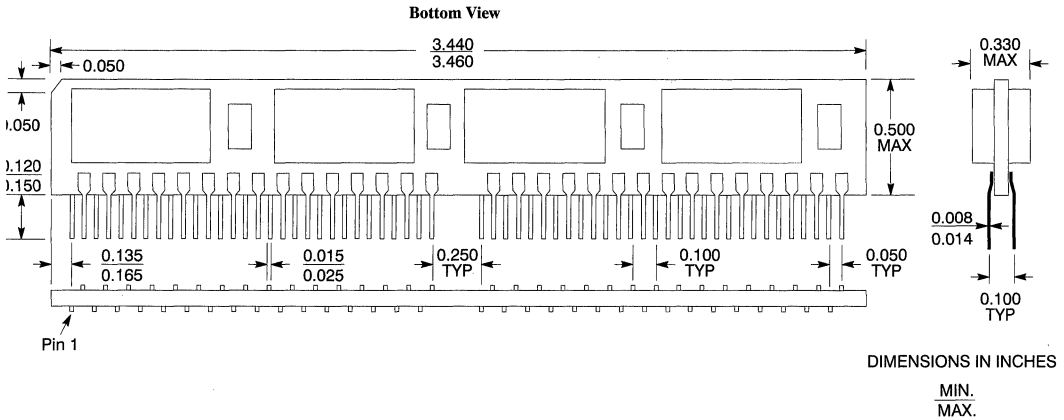
40-Pin Plastic VDIP Module PV04



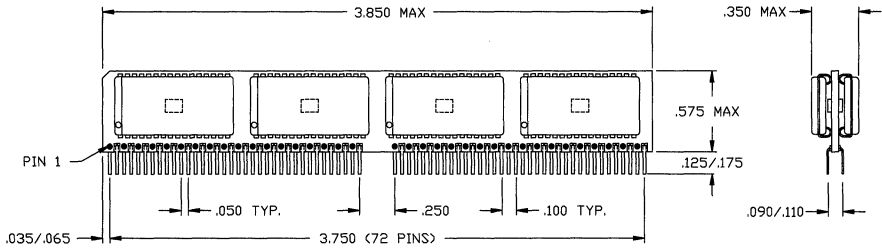
64-Pin Plastic ZIP Module PZ03



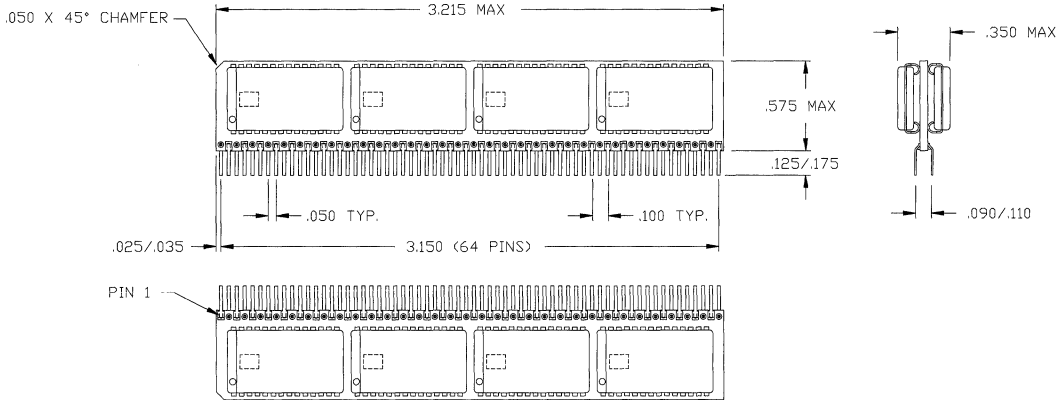
60-Pin Plastic ZIP Module PZ04



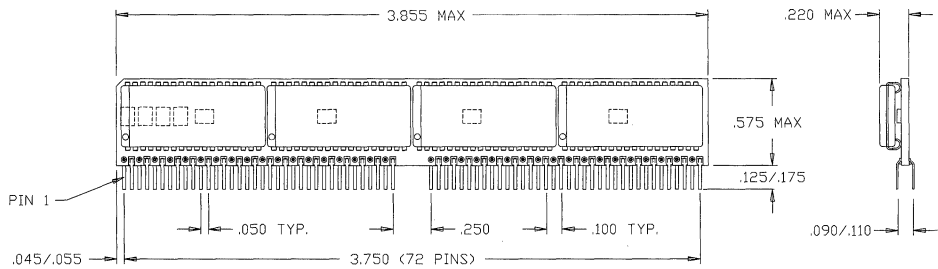
72-Pin Plastic ZIP Module PZ09



64-Pin Plastic ZIP Module PZ10



72-Pin Plastic ZIP Module PZ11





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Telex: 8954213 PRONTO G
FAX: (44) 81-518-32-22

Spectrum
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